Sample Proposal

Programmable Frequency Synthesizer

Note from BF: This was submitted by a student in EE413 in a previous semester. The proposal has some shortcomings, but it will give you a good idea of what to include.

Introduction

In the area of communications, the need of a clean, stable frequency source is desired and is required to meet stringent specifications for applications in today's developing market. The growing trend to use digital telecommunication technology has greatly emphasized the need for a cost effective self-contained frequency source with high spectral purity. The use of software to control a broadband synthesized frequency source would lower the overall cost of the manufacturing tasks since this one piece of hardware could, in theory, replace many older units that are not as versatile. The use of hardware based on current technologies allows for a design that can span a larger range of frequencies with fewer parts, which results in a low cost solution, especially in high volume areas. The concept of reducing cost is at the core of all companies. The final goal is to supply quality along with quantity. The programmable synthesized frequency source when designed will have the capability of covering the frequency range of 1.8 – 2.1 GHz and have the ability to tune to any single frequency within that range down to the XXXX Hz resolution.

(Note from BF: Summary should be included here)

Technical Discussion

The design of a frequency synthesizer, in the past, relied on the use of a fixed non-programmable PLL ASIC based on feedback control theory. This type of design usually synthesized a single frequency. To obtain a broader range of frequencies there was the need of switching circuits to switch in filters, multipliers, VCO's and prescalers which required a lot of initial NRE (Non-Recurring Engineering) and greatly increased the complexity of the circuits. Synergy offers a prepackaged synthesizer module with a broad range of programmable frequencies. The modules have a variety of frequency ranges, and the one that will be used in this design will be the SPLH-1470SA, which has a range of 1.8 – 2.1 GHz. Referring to the diagram in Figure 1.0 you will notice the overall signal flow and the final acceptance testing equipment setup. The datasheet for this module is located at the end of this document in Appendix A. The design will have multiple design phases – each phase schedule describing how tasks will be implemented as time availability permits. The first and most important phase will be thoroughly completed, while the others will be implemented depending on time available. The first phase will consist of the design/prototyping of the programmable software controlled synthesized frequency source hardware and the necessary LabVIEW software to control it. Manual measurements of phase noise, reference spur suppression and output power will be performed to demonstrate that the programmable synthesizer performs correctly and meets the specifications. The second phase will consist of software development to automate the final acceptance-testing showing how automation can speed up the process of proving that the design met the required specifications. The areas that will be automated and tested include phase noise measurement, reference spur measurement, output power level verification and the ability to program over the range of frequencies that have been specified in the original design.

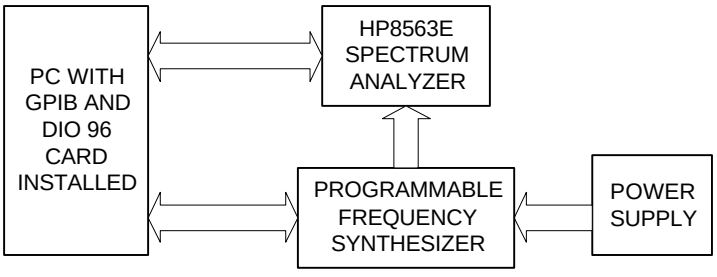


Figure 1.0 – Signal Flow Diagram

Phase One

Hardware Design

Phase one will consist of hardware and software design. To design the programmable frequency synthesizer hardware a few application specific chips will be used. The use of the Synergy synthesizer module will allow the design to be realized. Referring to Figure 1.1 the block diagram representation of the programmable frequency synthesizer is shown. Prototyping of the Synergy synthesizer module will be necessary to determine the extent of filtering and signal conditioning that will be required to produce a clean and stable source. The initial schematic will be created along with the necessary NETLIST file using OrCAD Capture 9.0. The PCB will be created in Protel PCB (Printed Circuit Board) using the NETLIST file generated from OrCAD Capture 9.0. When the circuit has been proven to work, the schematic and NETLIST will be updated to reflect the final design using OrCAD Capture 9.0. The PCB layout will be updated and Gerber files, which allow an outside source to do the manufacturing of the final PCB, will be created. The final EM (Engineering Model) will be fabricated on the PCB and installed into a chassis. The chassis will have a D-Sub connector and a SMA connector to interface with the computer and test equipment. The initial goal on chassis dimensions along with the location of the D-Sub and SMA connectors are depicted in Figure 1.2. The final test setup will consist of the equipment shown in Figure 1.0, unless major design issues come up during prototyping stages, and will be supplied by In-Phase Technologies and the student in charge for the final acceptance testing at NJIT. The user interface will look similar to that shown in Figure 1.3. This GUI (Graphical User Interface) is shown as a sample screen; the final may be more complex, depending on whether phase two of the design is completed. Test procedures will be created along with a data sheet, which will be filled out during the final testing at the college. Depending on the time available, phase two will be implemented and the test procedures and data sheet will become unnecessary. To minimize the final project demonstration, these items will be eliminated.

Software Design

The initial LabVIEW code will consist of the bare essentials to get the synthesizer to lock on frequency. When the design is experimentally proven to work, the code will be upgraded. The updating will add the functionality necessary to produce the final programmable software controlled synthesized frequency source having a friendly GUI. Phase two, if pursued, will add additional functionality to the GUI and automate the testing procedure.

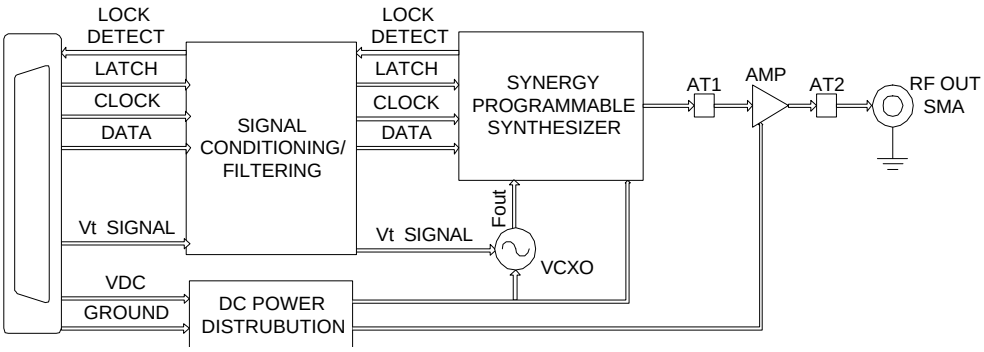


Figure 1.1 – Proposed Circuit

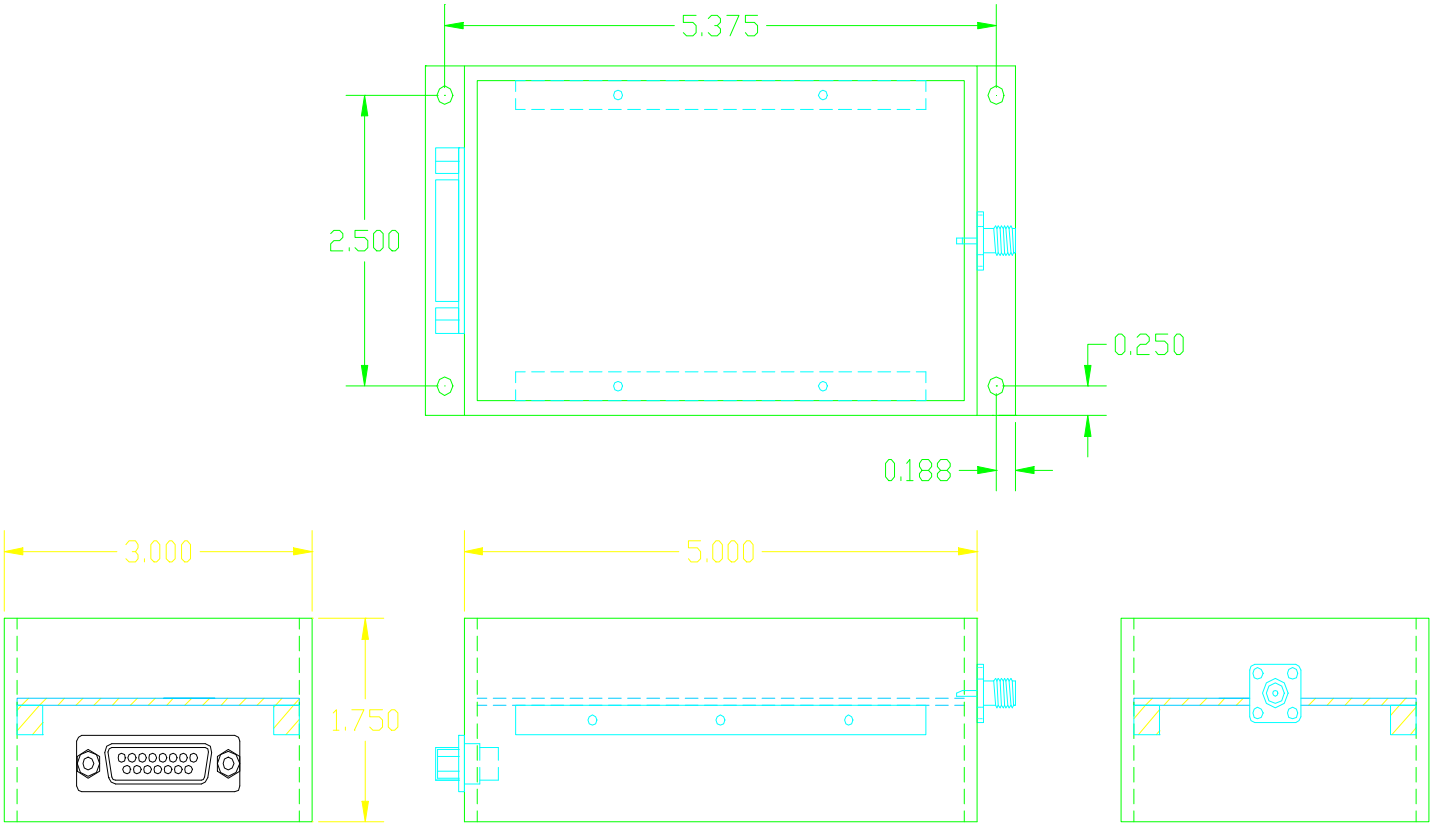


Figure 1.2 – Proposed Chassis

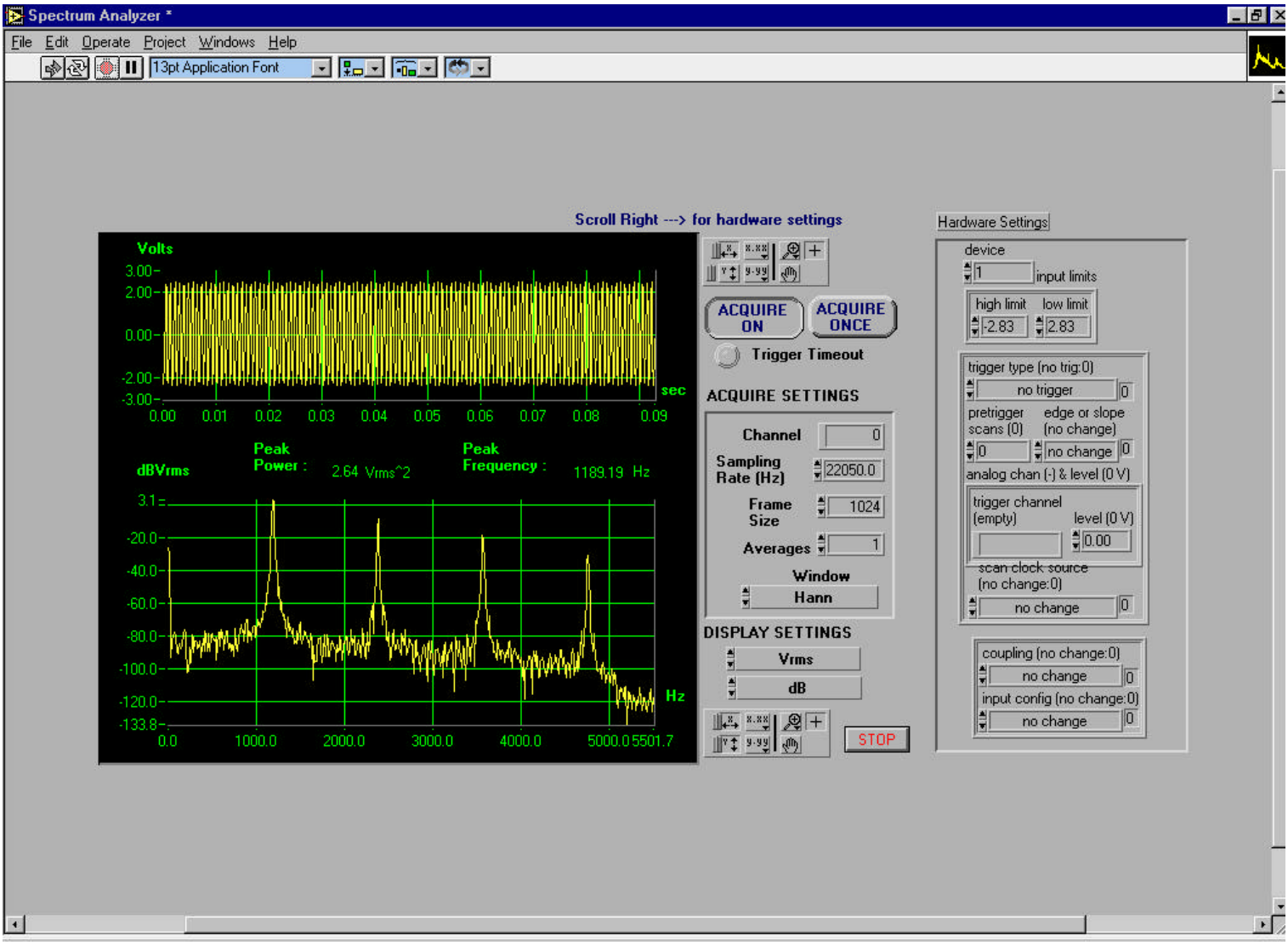


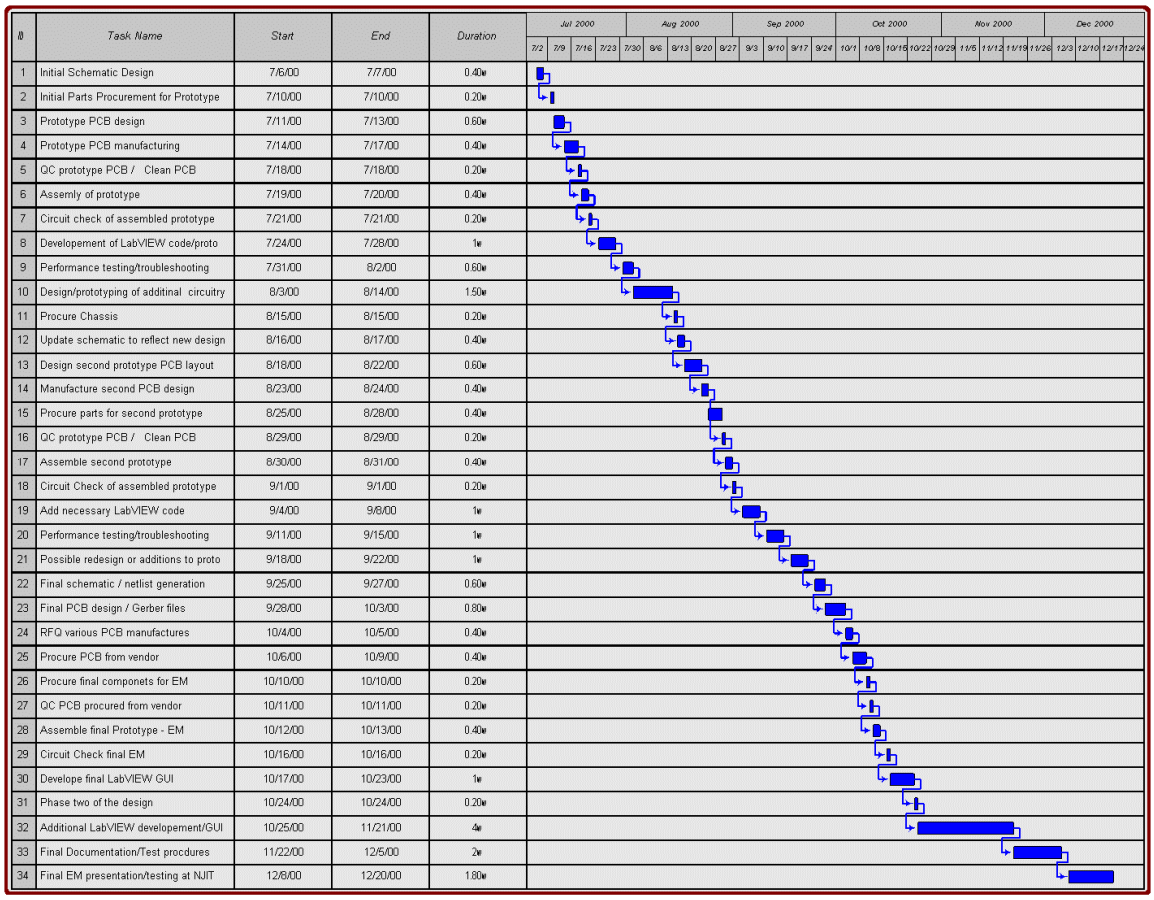
Figure 1.3 – Sample GUI

Phase Two

Software Design

Upon total completion of phase one of the design, a few improvements to the design will be explored making the product testing more efficient and automated. The designing and implementation of a method to test out the programmable software controlled synthesized frequency source, solely using the final setup shown in Figure 1.0 and software, will be attempted. The human interaction needed to perform the original manual testing will be minimized. The measurements will include, but are not limited to, the following areas: phase noise measurement, reference spurious location and power level determination, power output at the programmed frequency, and varying of output frequency in predetermined steps with the start and stop frequency entered as text fields in the front panel of the GUI. The need to use GPIB bus will become necessary in order to communicate with the HP8563E spectrum analyzer and it will require some additional LabVIEW software development. The tests, which will be performed, can be done using LabVIEW and the spectrum analyzer and will require some additional coding as well. Wherever possible, the specifications will be user-entered text fields and the unit will be tested solely using LabVIEW to determine if the hardware meets the requirements. This idea of automated testing will explore the possibilities of high volume production/testing, which will reduce labor costs and increase the profit per unit dramatically.

Schedule



ID	Task Name	Start	End	Duration
1	Initial Schematic Design	7/6/00	7/7/00	0.40w
2	Initial Parts Procurement for Prototype	7/10/00	7/10/00	0.20w
3	Prototype PCB design	7/11/00	7/13/00	0.60w
4	Prototype PCB manufacturing	7/14/00	7/17/00	0.40w
5	QC prototype PCB / Clean PCB	7/18/00	7/18/00	0.20w
6	Assemly of prototype	7/19/00	7/20/00	0.40w
7	Circuit check of assembled prototype	7/21/00	7/21/00	0.20w
8	Developement of LabVIEW code/proto	7/24/00	7/28/00	1w
9	Performance testing/troubleshooting	7/31/00	8/2/00	0.60w
10	Design/prototyping of additinal circuitry	8/3/00	8/14/00	1.50w
11	Procure Chassis	8/15/00	8/15/00	0.20w
12	Update schematic to reflect new design	8/16/00	8/17/00	0.40w
13	Design second prototype PCB layout	8/18/00	8/22/00	0.60w
14	Manufacture second PCB design	8/23/00	8/24/00	0.40w
15	Procure parts for second prototype	8/25/00	8/28/00	0.40w
16	QC prototype PCB / Clean PCB	8/29/00	8/29/00	0.20w
17	Assemble second prototype	8/30/00	8/31/00	0.40w
18	Circuit Check of assembled prototype	9/1/00	9/1/00	0.20w
19	Add necessary LabVIEW code	9/4/00	9/8/00	1w
20	Performance testing/troubleshooting	9/11/00	9/15/00	1w
21	Possible redesign or additions to proto	9/18/00	9/22/00	1w
22	Final schematic / netlist generation	9/25/00	9/27/00	0.60w
23	Final PCB design / Gerber files	9/28/00	10/3/00	0.80w
24	RFQ various PCB manufactures	10/4/00	10/5/00	0.40w
25	Procure PCB from vendor	10/6/00	10/9/00	0.40w
26	Procure final componets for EM	10/10/00	10/10/00	0.20w
27	QC PCB procured from vendor	10/11/00	10/11/00	0.20w
28	Assemble final Prototype - EM	10/12/00	10/13/00	0.40w
29	Circuit Check final EM	10/16/00	10/16/00	0.20w
30	Develope final LabVIEW GUI	10/17/00	10/23/00	1w
31	Phase two of the design	10/24/00	10/24/00	0.20w
32	Additional LabVIEW developement/GUI	10/25/00	11/21/00	4w
33	Final Documentation/Test procdures	11/22/00	12/5/00	2w
34	Final EM presentation/testing at NJIT	12/6/00	12/20/00	1.80w

Statement of work

Initial Schematic Design

Using OrCAD Capture 9.0 or the latest version available an initial schematic will be developed with only the core components of the design. The NETLIST will be generated using Tango format which Protel Advanced Schematic/PCB development packages requires. This technique is desirable since it allows a quick prototyping and turn around time using the T-Tek milling machine, which is available at In-Phase Technologies facilities.

Initial Parts Procurement for Prototype

The core components, which include the Synergy Synthesizer module and Hy-Q's VCXO 20 MHz frequency reference source, necessary to implement the design, will be ordered and stored in ESD (Electro-Static Discharge) safe bags until production and assembly of the prototype unit begins. Lead-time on these components should be less than a week and will not hold up the prototyping of the programmable frequency synthesizer's schedule.

Prototype PCB design

Protel Advanced Schematic/PCB development package will be utilized to complete the initial PCB layout necessary for the prototyping of the synthesizer. The components, which will be used, are mostly SMT (Surface Mount Technology) and the footprints can be created in Protel with little effort if they are unique. Importing OrCAD Capture's generated NETLIST file, which has been created in the Tango format, will be necessary. This technique has been determined in previous PCB design efforts to work correctly and will be applied here to limited unnecessary risk.

Prototype PCB manufacturing

The file completed in Protel Advanced Schematic/PCB and exported correctly will be ready for importing into IsoPro software for modifications and additions before the final step of milling using the QuickCAM software and the T-TEK machine. Isopro uses the image files generated from Protel Advanced Schematic/PCB, which are in Gerber format, to create the layout in a way that QuickCAM understands. After exporting the files necessary and importing them into QuickCAM the prototype PCB will be manufactured. The three main limitations to the manufacturing of a PCB using the T-TEK machine are: (1) two -sided boards or single sided boards can be created but not three layers or greater. This design can easily be developed using a two-sided PCB as the basis. (2) The space between two traces is limited to the smallest end mill available which is .011 inch in diameter. (3) Vias or through-holes are limited to a diameter size of .011 inch. With these limitations in mind the PCB design can be manufactured very quickly.

QC prototype PCB / Clean PCB

The use of the T-TEK machine to produce a fast turn around PCB does not eliminate the need to QC (Quality Check) and clean the finished product. When milling has finished there are times that small fragments of copper clad still remain between traces or pads, which have, in past designs, created shorts to ground or undesired connections. The time spent verifying these issues making sure they are non-existent will, in the long run, save schedule delays with the elimination of time spent troubleshooting a unit with problems. Using alcohol and a cotton swab allows quick cleaning of the PCB. This makes the assembly and soldering of components easier and manufacturing problems become easy to see.

Assembly of prototype

Using good ESD procedures and wrist strap for a good ground, the components will be placed on the PCB and soldered. The small SMT components may require soldering to be performed under a microscope to insure proper soldering with no cold solder joints or solder bridges to other traces. The microscope, if necessary, is available at In-Phase Technologies and can be accessed to perform the soldering.

Circuit check of assembled prototype

The use of a digital multimeter set to measure ohms (continuity) will allow the circuit check to be performed. Using the schematic diagram generated in OrCAD Capture 9.0 and Protel Advanced Schematic/PCB layout/silkscreen a continuity check can be performed from point to point to verify the connections exist. This check again saves time in the long run and limits the loss and overstress of expensive components due to reverse biasing, improper voltage levels being applied to a pin, or connection not originally intended being made.

Development of LabVIEW code/proto

Once the prototyped programmable software controlled synthesized frequency source has been assembled and circuit checked it can be setup and used to help in the development of the LabVIEW VI (Virtual Instrument) necessary to control the hardware. The initial development will include a front panel display, which will have programming input fields available to the user for inserting various values to determine the dynamics of the prototype. Interfacing the DIO 96 card and terminal block to the hardware will require a test harness to connect the signals LabVIEW will control and supply to the unit. Using this setup, the initial code will be developed, allowing the testing of the hardware.

Performance testing/troubleshooting

With the use of the VI software developed in the previous stage, some basic tests will be performed to determine the need of additional circuitry. There are some main areas, which will be examined, to determine these needs. The lock detect output, which indicates a lock on frequency condition, will be looked at to verify a high or low logic level. Then, using a spectrum analyzer, the carrier frequency spectrum will be examined to verify again that it is locked to the correct frequency. Following this test, the output power of the synthesizer module will be determined, using the peak search feature on the spectrum analyzer, and compared to the specifications on the manufacturers data sheet. Then, locating the reference spurious frequencies, the determination of their power level as compared to the carrier frequency will be determined. This can be accomplished by peaking to the carrier frequency; then, using the marker delta feature, picking the peak on the reference spurs, and then comparing it to the data sheet to see if it meets the manufacturer's specifications. Phase noise measurements can be done next to verify they meet the manufacturers specifications. Using the HP8563E spectrum analyzer, property of In-Phase Technologies, there are two techniques that can be implemented to do this measurement. The first option is to use the built in USER program add-on to do the measurement. Using the first can also produce the degrees RMS measurement. The

second is the manual technique of verifying the phase noise by setting the span to a value that is large enough to move the marker 10KHz/100KHz off the carrier frequency and measuring the power level at that point. Another test that will be performed is the sensitivity of the VCXO. Controlling the Vt signal using LabVIEW will accomplish this by measuring the change in the output frequency as the DC level is varied. This test is necessary to determine the maximum swing of the reference source. The currents will be measured using the digital multimeter so that they are known for possible circuit design development. Using the oscilloscope, all signals will be monitored and examined to determine which signals may need signal conditioning.

Design/prototyping of additional circuitry

When additional circuitry is determined necessary Pspice will be used, where possible, to simulate the design of the additional circuitry. With the knowledge gained from other design efforts, the process should flow smoothly. Research, if needed, will be done to locate the necessary components. With the use of a Digi-Key catalog, along with many other sources, this task can be accomplished.

Update schematic to reflect new design

Documentation control will be maintained and the original OrCAD Schematic will be updated as the design matures and will reflect the most recent design. The NETLIST that is created with the schematic file will be regenerated so that the layout in Protel Advanced Schematic/PCB can be updated to incorporate the changes in the design.

Design second prototype PCB layout

Using Protel Advanced Schematic/PCB, the new footprints will be generated in the library. When the NETLIST is imported again the old layout will be modified and the added component will be loaded into this file so the layout can be modified to represent the current design.

Manufacture second PCB design

When the Gerber files have been generated using Protel Advanced Schematic/PCB the same procedure used in the first prototyping unit will be used again to import them into IsoPro. Next it will be necessary to modify and then export the files in the QuickCAM format. The exported IsoPro files will then be imported into QuickCAM and the PCB can finally be milled and cutout yielding the new prototyping PCB.

Procure parts for second prototype

When the new design has been simulated using Pspice, or other simulation software, such as Matlab 5.0 or Touchtone, and a great degree of confidence with little risk exist the necessary parts will be procured. The main vendors that will be used as the sources of components are as follows: Digi-Key, Hy-Q, Newark Electronics and Compaq.

QC prototype PCB / Clean PCB

The use of the T-TEK machine to produce a fast turn around PCB does not eliminate the need to QC and clean the finished product. When milling has finished there are times that small fragments of copper clad still remain between traces or pads, which have, in past designs, created shorts to ground or undesired connections. The time spent verifying these issues making sure they are non-existent will, in the long run, save schedule delays with the elimination of time spent troubleshooting a unit with problems. Using alcohol and a cotton swab allows quick cleaning of the PCB. This makes the assembly and soldering of components easier and manufacturing problems become easy to see.

Assemble second prototype

Using good ESD procedures and wrist strap for a good ground, the components will be placed on the PCB and soldered. The small SMT components may require soldering to be performed under a microscope to insure proper soldering with no cold solder joints or solder bridges to other traces. The microscope, if necessary, is available at In-Phase Technologies and can be accessed to perform the soldering.

Circuit Check of assembled prototype

The use of a digital multimeter set to measure ohms (continuity) will allow the circuit check to be performed. Using the schematic diagram generated in OrCAD Capture 9.0 and Protel Advanced Schematic/PCB layout/silkscreen a continuity check can be performed from point to point to verify the connections exist. This check again saves time in the long run and limits the loss and overstress of expensive components due to reverse biasing, improper voltage levels being applied to a pin, or connection not originally intended being made.

Add necessary LabVIEW code

Once the prototyped programmable software controlled synthesized frequency source has been assembled and circuit checked it can be set up and used to help in the additional development of the LabVIEW VI necessary to control the hardware. The development will include modification to front panel display, which will have the programming input fields available for inserting various values to determine the dynamics of the prototype. Additional interfacing of the DIO 96 card and terminal block to the hardware might require modifications to the test harness, which connects the signals LabVIEW will control and supply to the hardware. Using the hardware setup, and code developed will allow debugging of the new code and additional testing of the hardware.

Performance testing/troubleshooting

With the use of the VI software developed in the previous stage, the basic tests will be performed again to determine the need of additional circuitry. There are some main areas, which will be examined to determine these needs. The lock detect output, which indicates a lock on frequency condition, will be looked at to verify a high or low logic level. Then, using a spectrum analyzer, the carrier frequency spectrum will be examined to verify that it is locked to the correct frequency. Following this test, the output power of the synthesizer module will be determined, using the peak search feature on the spectrum analyzer, and compared to the specifications on the manufacturers data sheet. Then locating the reference spurious frequencies, the determination of their power level as compared to the carrier frequency will be determined. This can be accomplished by peaking to the carrier frequency then, using the marker delta feature, picking the peak on the reference spurs and comparing it to the data sheet to see if it meets the manufacturer's specifications. Phase noise measurements can be done next to verify they meet the manufacturer's specifications. Using the HP8563E spectrum analyzer, property of In-Phase Technologies, there are two techniques that can be implemented to do this measurement. The first option is to use the built in USER program add-on to do the

measurement. Using the first can also produce the degrees RMS measurement. The second is the manual technique of verifying the phase noise by setting the span to a value that is large enough to move the marker 10KHz/100KHz off the carrier frequency, measuring the power level at that point. Another test that will be performed is the sensitivity of the VCXO. Controlling the Vt signal, using LabVIEW, will accomplish this by measuring the change in the output frequency as the DC level is varied. This test is necessary to determine the maximum swing of the reference source. The currents will be measured using the digital multimeter so that they are known for possible circuit design development. Using the oscilloscope, all signals will be examined to determine if visible improvements have occurred on those signals that had problems in the prior prototype. The signals that still may need signal conditioning will be examined again and a new design approach will be taken to improve the performance.

Possible redesign or additions to proto

If the need of additional circuitry is determined, Pspice will be used, where possible to simulate the design of the additional circuitry. With the knowledge gained from other design efforts, the process should flow smoothly. Research if needed, will be done to locate the necessary components and with the use of a Digi-Key catalog, along with many other sources, this task can be accomplished. This should bring the design and layout closer towards the final EM.

Final schematic / NETLIST generation

Documentation control will be maintained and the original OrCAD Schematic will be updated to refelect the final design. The final NETLIST will be generated using the schematic file so that the final PCB layout in Protel Advanced Schematic/PCB can be designed making sure to incorporate all changes made to the previous design.

Final PCB design / Gerber files

Protel Advanced Schematic/PCB will be used to create the final Gerber files necessary to have a vendor manufacture the final PCB. Great care will be taken to ensure all layout problems have been fixed and are non-existent in the final PCB layout. The final dimensions must correspond to the dimensions specified to the chassis vendor. The main

landmarks include the output SMA connector and the side rail hole indexes which will be used to mounted the PCB securely and supply the PCB with a solid ground.

RFQ various PCB manufactures

There are a variety of vendors that can be used to produce the PCB from Gerber file format. The approach that will be used here is finding the manufacturer, which will produce the PCB for a competitive price and have a quick turn around on the design. One possible vendor is Advanced Circuit Inc. Based upon previous PCB design experience, it has been found that they are very helpful and try their best to turn the design into a PCB as quickly as possible. Although this vendor has been used in the past at In-Phase Technologies, other vendors will receive a RFQ (Request for Quote) and the decision will be made on which one to select, depending on their response.

Procure PCB from vendor

When the vendor has been selected, the PCB will be ordered and, depending on the way the schedule on the project is going, the amount of time set aside for delivery of the final EM PCB will be determined. The fact that In-Phase Technologies has prior dealings with most PCB vendors should make it possible to expedite the shipment if necessary.

Procure final components for EM

Components will be procured for the final prototype EM. Most of the components will be obtained from prior prototyping units to save cost. Some SMT parts are available at In-Phase Technologies and have no delivery times associated with them. Those that will need procurement will be ordered and delivery times will be minimized as much as possible to keep the project schedule flowing smoothly.

QC PCB procured from vendor

The use of an outside source to produce a fast turn around PCB does not eliminate the need to QC (Quality Check) and clean the finished product. When PCBs are manufactured there can still be situations where traces connected to other traces or ground planes have created shorts to ground or undesired connections. The time spent verifying these issues making sure they are non-existent will, in the long run, save valuable resources with the elimination of effort spent troubleshooting a unit with problems. Using alcohol and a cotton swab allows the cleaning of the PCB. This makes the assembly and soldering of components easier and manufacturing problems become easy to see and proper actions can be taken to fix the problems.

Assemble final Prototype - EM

Using good ESD procedures and wrist strap for a good ground the components will be placed on the PCB and soldered. The small SMT components may require soldering to be performed under a microscope to insure proper soldering with no cold solder joints or solder bridges to other traces. The microscope, if necessary, is available at In-Phase Technologies and can be accessed to perform the soldering. With the EM design assembled the final results and performance can be studied.

Circuit Check final EM

The use of a digital multimeter set to measure ohms (continuity) will allow the circuit check to be performed. Using the schematic diagram generated in OrCAD Capture 9.0 and Protel Advanced Schematic/PCB layout/silkscreen a continuity check can be performed from point to point to verify the connections exist. This check again saves time in the long run and limits the loss and overstress of expensive components due to reverse biasing, improper voltage levels being applied to a pin, or connection not originally intended being made.

Develop final LabVIEW GUI

Once the EM prototype of the programmable frequency synthesizer has been assembled and circuit checked it can be set up and used to help in the additional development of the LabVIEW VI (Virtual Instrument) necessary to control the hardware. The development will include modification to front panel display, which will have the programming input

fields available for inserting various values to determine the dynamics of the prototype. Additional interfacing of the DIO 96 card and terminal block to the hardware may require modifications to the test harness which connects the signals LabVIEW will control and supply to the hardware. Using the hardware setup, the software developed will allow the final testing of verification of the unit as detailed in phase one of the design.

Phase two of the design

Depending on available time left in the schedule, phase two of the design will begin. Phase two consists of many small parts and a decision at this time will be made on the appropriate plan with a modified schedule, breaking down the details of the software development tasks to bring the new ideas into being. The main component of phase two of the project will require a variety of LabVIEW software development and interfacing.

Additional LabVIEW development/GUI

In-Phase Technologies has developed LabVIEW software for the automation of STE (Special Test Equipment) and STA (Special Test Assemblies) chassis, which are designed and manufactured at the Clarksburg NJ location for a variety of customers. With the use of some already written LabVIEW code, the modifications and changes that will become clearly apparent at the time and necessary to implement the improvements, the additional LabVIEW software can be realized with little risk associated with it. The main driving force here is the ability to incorporate the changes and additions using the available scheduling time or the time gained in other areas of the project where tasks were completed ahead of schedule.

Final Documentation/Test procedures

The programmable frequency synthesizer will have a final documentation package associated with it, which will include schematics, PCB artwork, mechanical drawings, part list, LabVIEW front panel description explaining the display/controls and indicators, final test procedures to verify the unit works, with a step-by-step test to be performed at NJIT. Other documents may be contained in the final documentation package as it becomes necessary to include them. The contents of the package will also depend on if phase two is also completed 100% or partially.
Final EM presentation/testing at NJIT

The final acceptance testing of the programmable software controlled synthesized frequency source will occur on a scheduled date at NJIT this date has not been set and is TBD (To Be Determined). The required hardware will be transported to the college and set up for the demonstration. In the event the demonstration spans overnight, the need to break down the setup and remove the high priced hardware will be necessary for security purposes as required by In-Phase Technologies management. The following day, the time required to set the test bed back up will be minimal. Dependent on whether phase two has been completed, the performance testing can be accomplished in about 20 minutes or less.

Budget

In-Phase Technologies and the student will subsidize the design and devopment of the programmable software controlled synthesized frequency source. The project, not including test equipment, pc and DIO 96 card should not cost more than 500 dollars. The test equipment, pc, and DIO 96 card will be borrowed when the final acceptance testing occurs at NJIT. This project is a sub-system of the larger system, which will be delivered to USA. This sub-system will be designed and developed at work, but certain phases will be done at other times, if the schedule is behind or other projects require work. The final completion date should remain sound but the intermediate schedule from week to week may differ slightly as priorities arise. When these situations arise, late night sessions or weekend sessions will be implemented to keep the project on course.

Appendix

Attached on the following pages are component data sheets and other helpful papers.

Bibliography

Hy-Q International – www.hy-q.com

Synergy Microwave Corporation – www.synergymwave.com