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Electrical Characteristics of Thermally Evaporated HfO_2

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The electrical characteristics of hafnium oxide (HfO_2) films, grown by standard thermal evaporation of hafnium while adding oxygen at constant partial pressure during evaporation, were investigated for the first time. The dielectric constant as measured by the capacitance-voltage technique is estimated to be in the range of 18-25. Metal oxide semiconductor (MOS) capacitors using HfO_2 as dielectric and annealed at 450°C show a hysteresis below 30 mV. A low leakage current density of $<10^{-7}$ A/cm^2 at 1 V and reduced bulk oxide charges 1.61×10^{11}/cm^2 were also observed. The interface state density and low-temperature charge trapping behavior of these films were also investigated. Observed characteristics indicate that HfO_2 films deposited by standard thermal evaporation are suitable for MOS device applications.
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Hafnium oxide (HfO_2) has been under intense investigation recently for replacing conventional SiO_2 (or SiO_xN_y) as a high dielectric constant (high-*k*) gate dielectric in complementary metal oxide semiconductor (CMOS) devices to reduce tunneling current and boron penetration.[1] Even though many high-*k* materials are currently being studied, poor short channel effects due to the fringing field induced barrier lowering effect[2] and thermal instability due to the formation of silicides or interfacial layers impede the effectiveness of these materials when directly in contact with silicon.[3] An HfO_2 film has a high dielectric constant (~25), high heat of formation (271 kcal/mol), and a large bandgap (5.68 ev),[4,5] and is thermally stable when in contact with silicon. In addition, HfO_2 is compatible with n^+ polysilicon without any barrier layer.[6] Various methods, such as atomic layer deposition,[7] evaporation with ion-assisted deposition,[8] sputtering,[9] *in situ* rapid thermal chemical vapor deposition,[10] and reactive electron beam evaporation[11] have been explored to deposit reliable and high-quality HfO_2 thin films. The properties of the grown film and interface show a pronounced dependence upon the deposition process and the precise deposition parameters chosen. Each technique has its own set of advantages and disadvantages. However, most of these techniques show some kind of interface damage. Sputtering and E-beam assisted depositions create radiation induced surface damage during film growth. Therefore, all these techniques require high-temperature annealing, which results in further deterioration of device performance and reliability. Because the HfO_2-Si interface is critical for excellent device characteristics, it is important to investigate other reliable deposition techniques for a high-quality interface.

In this work, HfO_2 thin films were deposited, for the first time, by a standard thermal evaporation technique while adding oxygen at constant partial pressure during evaporation. Thermal evaporation doesn't produce much damage to the interface, and it doesn't require high-temperature processing in comparison to the other techniques mentioned previously. Electrical characteristics of HfO_2 films have been studied using MOS capacitors. To investigate the charge trapping characteristics of HfO_2 films, a low-temperature characterization was done.

Experimental

HfO_2 films of two different thicknesses were deposited on n-type (resistivity of 10-20 Ω-cm) ⟨100⟩ Si wafers by standard thermal evaporation. Oxygen was added at constant partial pressure during evaporation. The base pressure was maintained at 10^{-6} Torr before oxygen was added. As oxygen was added during evaporation, the pressure in the chamber increased to 10^{-4} Torr. Tungsten boats were used in evaporating the hafnium. The films were deposited at room temperature. However, the measured substrate temperature was around 30-35°C because of source-induced substrate heating. No residual gas analysis was performed during evaporation. Immediately before the deposition of the films, the wafers were cleaned by the standard RCA clean (RCA-1 and RCA-2) followed by a 50:1 HF dip for 15 min. After the deposition of the HfO_2 film, a layer of 400 nm aluminum was deposited on top of the oxide film. Capacitors of various sizes were patterned by photolithography. Samples were subjected to post metal deposition annealing (PMA) at 350 and 450°C for 20 min in forming gas anneal (FGA: N_2/H_2 5%). HfO_2 film thicknesses of 50 and 60 nm were measured by ellipsometer after the deposition. Using the known physical thickness of the HfO_2 film, the dielectric constant was measured using accumulation capacitance. High-frequency capacitance-voltage (C-V) measurements and current-voltage measurements were performed using a Boonton 7200 capacitance meter and an HP4156B semiconductor parameter analyzer, respectively. The interface state density was estimated using the Terman method.[12] A CTI Cryogenics M22 closed-loop helium cooled refrigeration system and a Palm Beach Cryophysics model 4075 temperature controller were used for the low-temperature measurements.

Results and Discussion

The dielectric constant, estimated from electrical measurements, is in the range of 18-25. Table I[11,13-16] shows the dielectric constant obtained by thermal evaporation compared with the dielectric constants obtained for HfO_2 films by other techniques. It seems that the dielectric constant for thermally evaporated films is the highest. The lower values of effective dielectric constants for the HfO_2 gate stack formed by other techniques are attributed to the interfacial layer thickness between the silicon substrate and HfO_2 after post deposition anneal.[11,17] If there is a growth of thin SiO_2 layer at the HfO_2 and silicon interface, then a noticeable reduction in depletion capacitance is observed. This occurs because the effective oxide thickness is estimated from the two capacitances (interfacial layer and high-*k* layer) in series. The high dielectric constant of our thermally evaporated HfO_2 films could be attributed to a lack of interfacial layer, as our samples were not subjected to a high-temperature anneal. A partial condensation of the HfO_2 film may be possible, because an increased accumulation capacitance was observed after annealing.[17] In addition, there may be possible tungsten contamination from the tungsten boats used in evaporating hafnium, which is currently being investigated further.

Figure 1 shows the normalized C-V characteristics of the 50 nm HfO_2 film at various annealing temperatures. An ideal C-V curve, determined by calculating the differential capacitance across the MOS gate stack between the experimentally measured accumulation

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Table I. Dielectric constant comparison with other current techniques.

Film deposition techniques	Lowest dielectric constant	Highest dielectric constant
Thermal evaporation	18	25
Electron beam evaporation[11]	18	22
Sputtering[13]	18	21
Atomic layer deposition[14]	16	23
Remote plasma oxidation[15]	19	19
Plasma enhanced CVD[16]	14	16

capacitance and the silicon depletion capacitance as a function of gate voltage,[18] was also plotted in Fig. 1. For these measurements, Al gate MOS capacitors with an area of 1.26×10^{-3} cm^2 were used. Measurements were taken before annealing as well as after 350 and 450°C FGA annealing. The C-V curves show a reduction in hysteresis up to 30 mV after 350°C anneal in comparison to the as-deposited film. No significant improvement was seen in hysteresis characteristics after 450°C anneal, though the curve was shifted toward the left, indicating a negative shift in flatband voltage. The reduction in hysteresis indicates the reduced charge trapping under negative gate bias. Partial passivation of interface states was possibly achieved as a result of FGA. As no reduction in oxide capacitance was observed after 450°C annealing, it is believed that an Al_2O_3-like layer or SiO_2 layer could have formed at the aluminum-HfO_2 interface and silicon-HfO_2 interface, respectively, during PMA. Partial condensation of HfO_2 is also possible because of annealing. The observed combined effect shows an increase in net capacitance (inset Fig. 1) suggesting minimum impact of the interfacial layer. Comparison of experimental C-V curves with the ideal C-V curve (no oxide charge) shows that the experimental C-V curve has moved closer to the ideal curve, indicating a reduction in bulk oxide charge from $6.97 \times 10^{11}/cm^2$ before annealing to $1.61 \times 10^{11}/cm^2$ after 450°C annealing. The high value of oxide charge ($\sim 10^{11}/cm^2$) indicates a significant contribution from the interface-

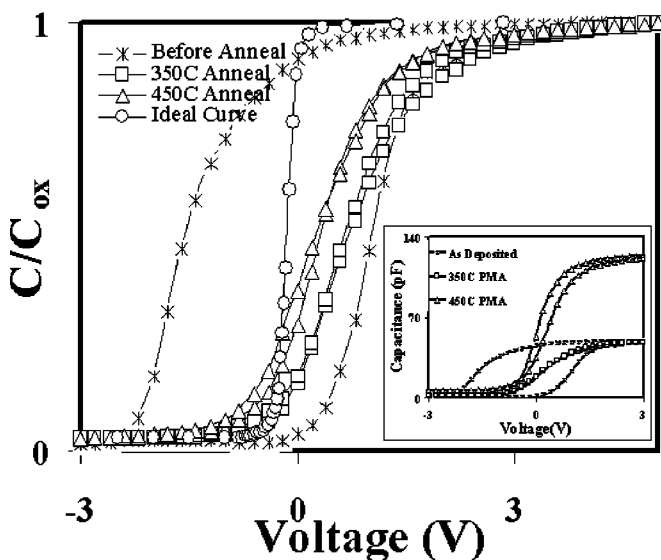

Figure 1. Normalized C-V curves of MOS capacitors with 50 nm HfO_2 film. Hysteresis was reduced to 30 mV after 450°C annealing. When compared to the ideal C-V curve, bulk oxide charges were reduced to $1.61 \times 10^{11}/cm^2$, and interface state density was $1.75 \times 10^{12}/cm^2$ eV after samples were annealed at 450°C. The inset shows the absolute capacitance behavior for 50 nm devices.

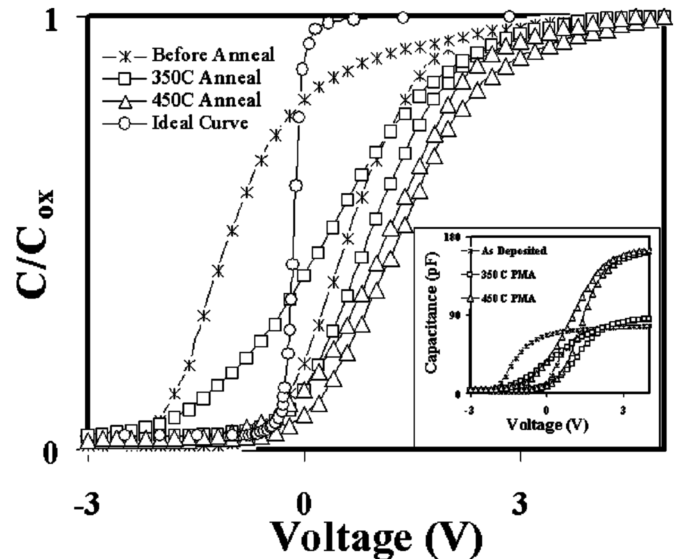

Figure 2. Normalized C-V curves of MOS capacitors with 60 nm HfO_2 film. Hysteresis of 175 mV can still be seen after 450°C annealing. When compared to ideal C-V curve, bulk oxide charges were increased to $1.15 \times 10^{12}/cm^2$, and interface state density was increased to $6.47 \times 10^{12}/cm^2$ eV after a 450°C anneal. The inset shows the absolute capacitance behavior for 60 nm devices.

trapped charge. The observed C-V stretch-out near inversion capacitance after 450°C annealing supports the presence of a high density of interface states.

The C-V characteristics for the 60 nm HfO_2 film are shown in Fig. 2. After 350°C anneal, hysteresis was reduced compared to the as-deposited films, but the stretch-out near inversion capacitance (C_{min}) indicates that significant charge trapping remains at the interfacial region near the Si substrate. After 450°C annealing, the C-V curves are more symmetric for the voltage sweep, indicating a partial passivation of interface states. The inset in Fig. 2 suggests that some condensation of HfO_2 has also occurred for the 60 nm films. Hysteresis was reduced to less than 175 mV, but is still much higher than that for the 50 nm HfO_2 film (Fig. 1). In addition, when the experimental C-V curves were compared with the ideal C-V curves, an increase in bulk oxide charges from $8.72 \times 10^{11}/cm^2$ before annealing to $1.15 \times 10^{12}/cm^2$ after 450°C annealing is noticed. This increase in oxide charge in 60 nm HfO_2 could be due to stoichiometric defects or extensive interface defects, as the C-V curves in Fig. 2 have moved farther away from the ideal curve after 450°C annealing. Therefore, the characteristics show that 50 nm HfO_2 films are electrically better than 60 nm thermally evaporated HfO_2 films.

To further investigate the oxide charge, the flatband voltage shift (ΔV_{FB}) was plotted as a function of annealing, as shown in Fig. 3. For the 50 nm HfO_2 film, ΔV_{FB} decreased from 1.1 V before annealing to 0.01 V after 450°C annealing, while for 60 nm thick hafnium oxide, ΔV_{FB} increased from 0.04 V before annealing to 0.8 V after 450°C annealing. One of the possible reasons for this behavior in 60 nm HfO_2 films could be due to higher built-in stress during the deposition of HfO_2 films, in comparison to the 50 nm film. Built-in stress generates bulk oxide defects as well as interface defects after the annealing of the films. The effect of annealing on the interface state density of these MOS capacitors is shown in Fig. 4. The Terman method was employed to estimate the interface trap density. Even though the Terman method has limited accuracy, it provides a quick estimate of interface trap density. The increase in interface state density was observed in both cases as a result of annealing. For the 50 nm HfO_2, it increased from $0.706 \times 10^{12}/cm^2$

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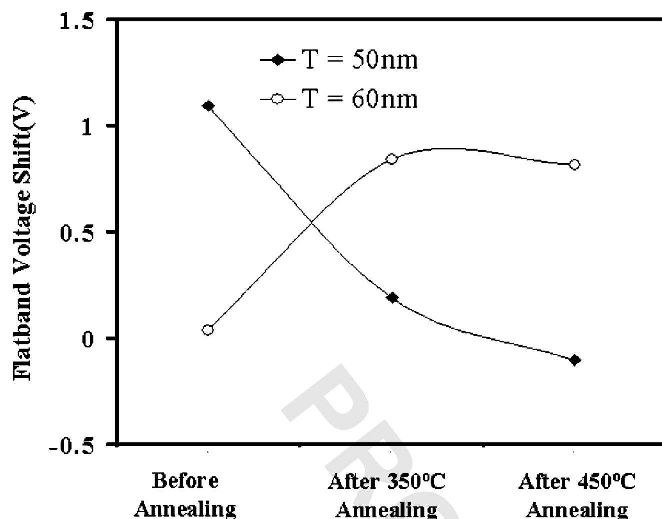

Figure 3. Effect of annealing on flatband voltage shift. In 50 nm HfO_2 films, ΔV_{FB} has reduced from 1.1 to 0.01 V; in 60 nm HfO_2 films, it has increased from 0.04 to 0.8 V.

eV before annealing to $1.75 \times 10^{12}/cm^2 eV$ after 450°C annealing, whereas for the 60 nm HfO_2, it increased from $2.2 \times 10^{12}/cm^2$ eV before annealing to $6.47 \times 10^{12}/cm^2$ eV after 450°C annealing. The increase in interface trap density can attributed to formation of a poor-quality interfacial layer. The significant degradation of interface quality in 60 nm HfO_2 films could be due to the relaxation of the stress after annealing.

The effect of annealing on the leakage current density of 50 and 60 nm HfO_2 films is shown in Fig. 5. The leakage current density was decreased by more than two orders of magnitude after 450°C annealing in comparison to 350°C annealing in both of the HfO_2 films. The leakage current density of the 50 nm HfO_2 films was reduced to $<10^{-7}$ A/cm^2 at 1 V after 450°C annealing. The leakage current density of 60 nm HfO_2 was reduced after 450°C annealing,

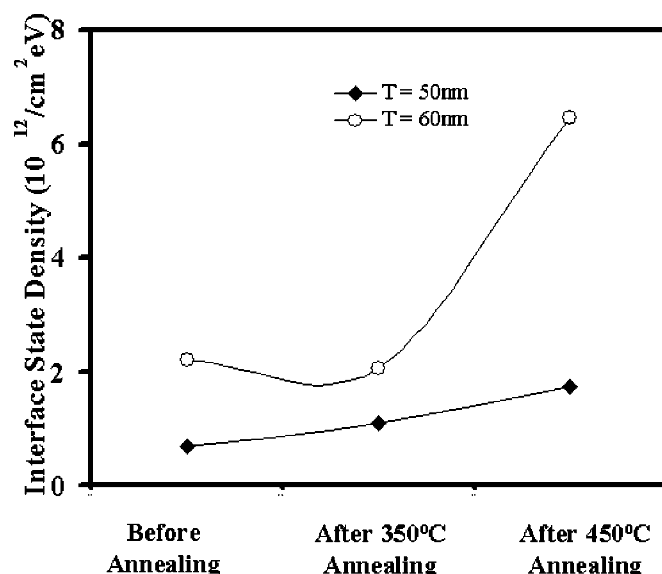

Figure 4. Effect of annealing on interface state density. In 50 nm HfO_2 films, it increased from $0.706 \times 10^{12}/cm^2$ eV before annealing to $1.75 \times 10^{12}/cm^2$ eV after 450°C annealing, whereas in 60 nm HfO_2 films, it increased from $2.2 \times 10^{12}/cm^2$ eV before annealing to $6.47 \times 10^{12}/cm^2$ eV after 450°C annealing.

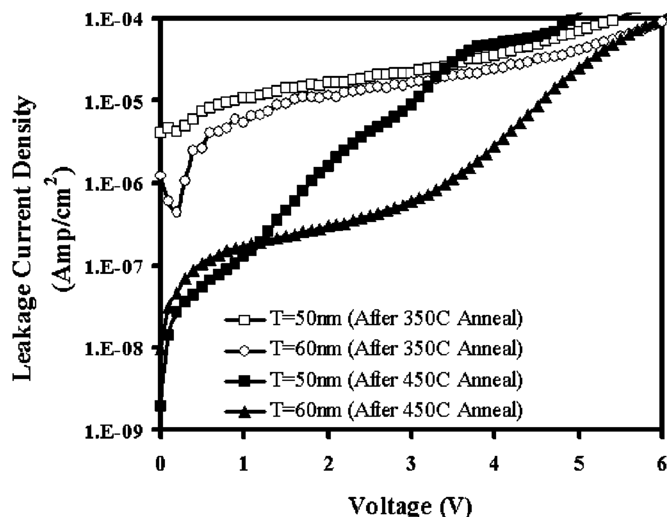

Figure 5. Leakage current density in 50 and 60 nm HfO_2 film MOS capacitors after 350°C and 450°C annealing.

but it was lower in the 50 nm films in comparison to the 60 nm ones. The observed improvement in leakage current in the 50 nm film is possibly due to the partial passivation of dangling bonds at the Si-HfO_2 interface, as noticed from the C-V characteristics. However, in the 60 nm films, the leakage current becomes resistive around 1 V, indicating a large increase of interface states after 450°C annealing. To further understand the mechanism of leakage current through the dielectric, we have plotted $\ln(J_{FN}/E_{ox}^2)$ *vs.* $1/E_{ox}$ in Fig. 6. The current due to Fowler-Nordheim (FN) tunneling at sufficiently high electric field E_{ox} follows the relationship given below[19]

$$\ln(J_{FN}/E_{ox}^2) = \ln(A) - B/E_{ox} \quad [1]$$

where J_{FN} is the density of the FN current, and A and B are constants for a particular insulating film.

From Fig. 5, E_{ox} was calculated using the following equation[19]

$$E_{ox} = V_{ox}/t_{ox}, \quad V_{ox} = V_G - V_{FB} - \phi_s \quad [2]$$

where ϕ_s is the surface potential at different positive bias voltages. The surface potential was estimated by comparing ideal and experimental C-V curves of the above mentioned MOS devices.[12] Considering the effective mass of the electron at the HfO_2 film to be $0.1m_0$,[20] we find that for $t_{ox} = 60$ nm, $\Phi_B = 0.3$ eV and for $t_{ox} = 50$ nm, $\Phi_B = 0.43$ eV when $1/E_{ox} > 9 \times 10^{-7}$ (cm/V) and $\Phi_B = 0.28$ eV when $1/E_{ox} < 9 \times 10^{-7}$ (cm/V). Here Φ_B is calculated from slope B of the FN plots, which is equal to $6.83 \times 10^7 ((m_{ox}/m)\Phi_B^3)^{1/2}$ (V/cm). The difference in effective barrier height is due to repairing of defects discrepancies. A straight line in Fig. 6b for the 60 nm film as predicted by Eq. 1 infers that at a high oxide electric field FN tunneling is the dominant leakage mechanism. However, the 50 nm film (Fig. 6a) shows the same FN tunneling characteristics at high fields, but at low fields some improvement in trap assisted tunneling is evident.

Because the 50 nm HfO_2 films have shown better device performance in comparison to the 60 nm HfO_2 films, we have investigated the charge trapping characteristics of 50 nm films at various temperatures. MOS capacitors with 50 nm HfO_2 films of area 1.96×10^{-3} cm^2 were studied. The temperature was gradually decreased from 290 to 130 K and high-frequency C-V measurements were taken once the sample attained a stable temperature. C-V curves at different temperatures (see Fig. 7) demonstrated both parallel shift and stretch-out along the bias axis as the temperature was decreased. This verifies the presence of a higher number of both

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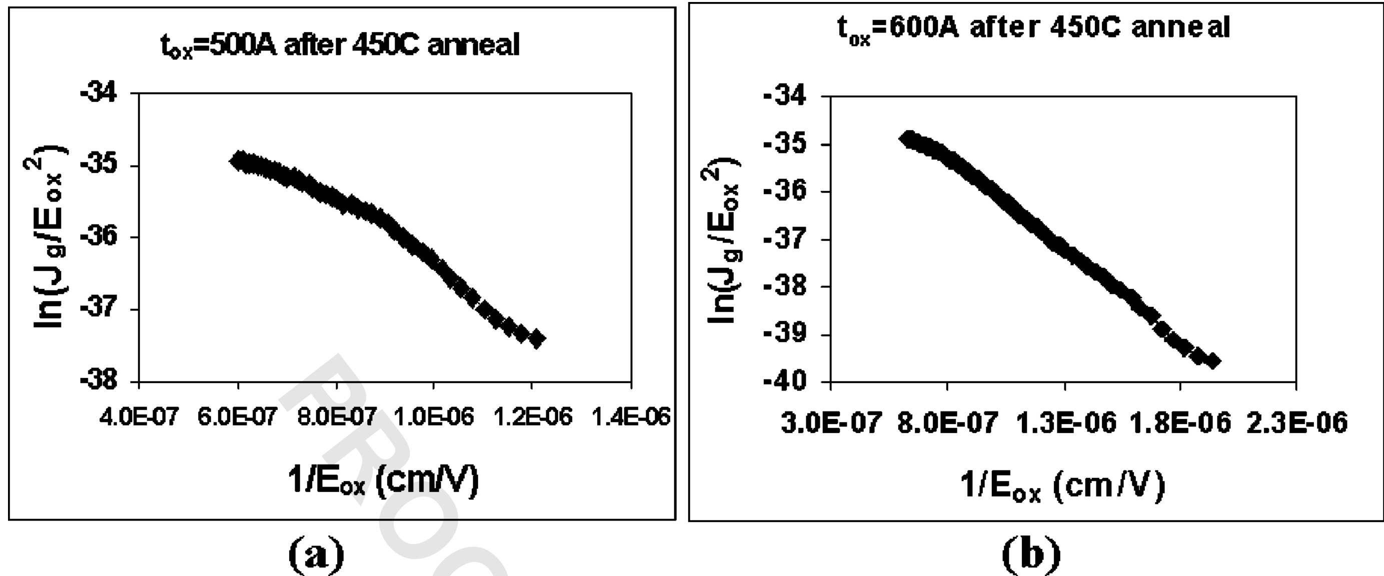

Figure 6. $\ln(J_{FN}/E_{ox}^2)$ *vs.* $1/E_{ox}$ plot for Al/HfO_2/n-Si MOS capacitors with (a) 50 nm of HfO_2 and (b) 60 nm of HfO_2.

shallow bulk oxide and interface trapped charges at low temperatures. Electron trapping seems to be dominant because the higher barrier for holes in HfO_2 (3.4 eV) compared to electrons (1.5 eV)[21] enhances the electron trapping probability.[21] The electron traps, especially shallow bulk oxide ones with energy levels close to the conduction band, became more active as the temperature went down, and this contributed to the shift of the C-V curves at low temperatures.[22] Moreover, we can observe hysteresis above the midgap voltage in the C-V curves at low temperature.

The flatband voltage shift (ΔV_{FB}) was calculated for the devices under test at different temperatures. Figure 8 shows the ΔV_{FB} for some samples at temperatures ranging from 290 to 130 K. A turnaround effect was observed in ΔV_{FB}, as it increased initially when the temperature was decreased to 210 K and then it started to decrease when the temperature was decreased further to 130 K.

To explain this turnaround effect in ΔV_{FB}, the concept of a trapped charge centroid model was used.[21] In these devices, oxide charge is the only variable observed when the temperature was reduced. Considering the one-dimensional distribution of trapped charges along the oxide thickness, the oxide charge centroid can be defined as[23]

$$q\int_0^{t_{ox}} x\rho(x)dx = qN_{t-equiv}\cdot x_t \qquad [3]$$

where $\rho(x)$ is the trapped charge distribution function, t_{ox} is the oxide thickness, and $N_{t-equiv}$ is the equivalent trapped charge per unit area having a centroid at x_t. Here, trapped charges consist of both interface and oxide trapped charges, and $x_t = 0$ at the gate and $x_t = t_{ox}$ at the substrate.

It is obvious from Eq. 1 that the density, location, and polarity (positively charged/negatively charged) of individual traps affect the location of the centroid. Considering only the contribution of trapped charges in ΔV_{FB},[23] we get

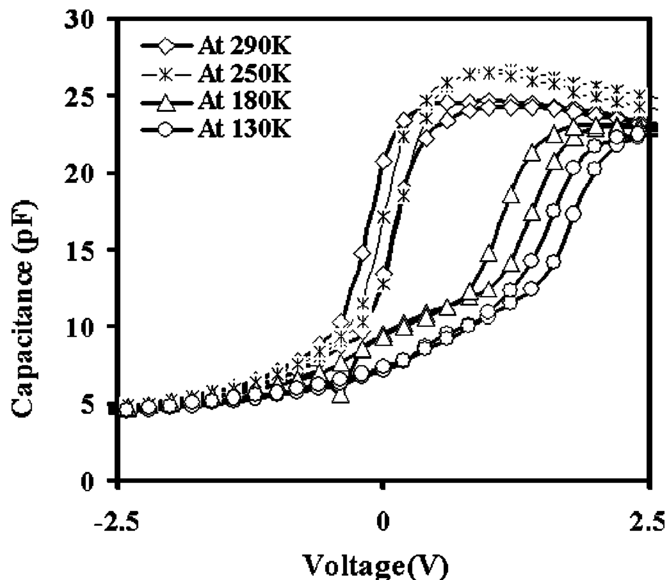

Figure 7. Low-temperature C-V curves for 50 nm HfO_2 MOS capacitor.

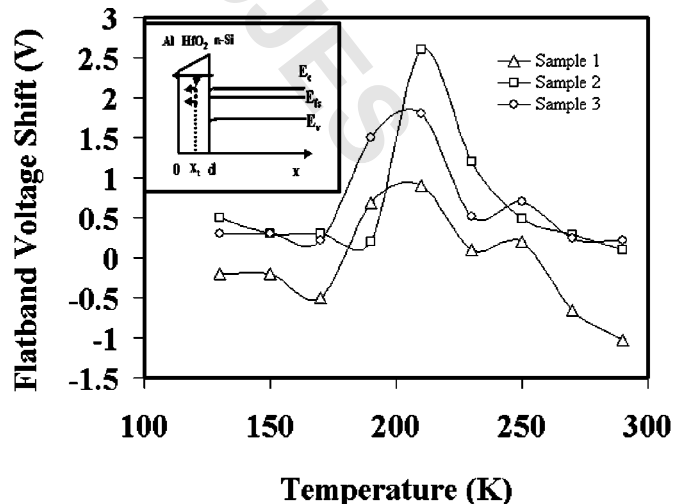

Figure 8. Flatband voltage shift as a function of temperature for 50 nm HfO_2 MOS capacitor. The inset shows the energy diagram for Al/HfO_2/n-Si, indicating a shift of the centroid toward the gate electrode.

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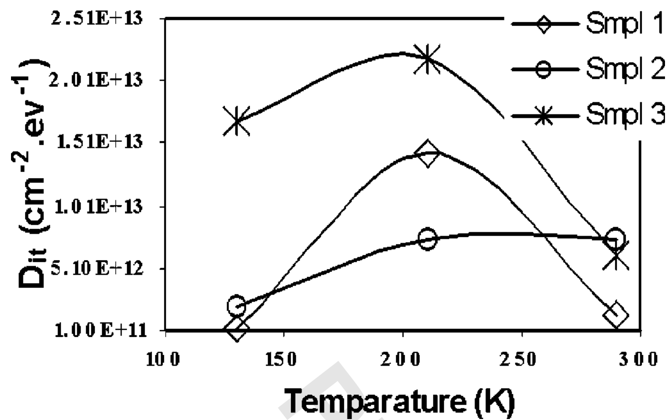

Figure 9. Interface states, D_{it}, as a function of temperature for various Al/HfO_2/n-Si MOS samples measured by conductance method.

$$\Delta V_{FB} = -q\frac{\Delta N_{t-equiv}}{C_{ox}} \cdot \frac{x_t}{t_{ox}} \quad [4]$$

Here, C_{ox} is the oxide capacitance, q is the charge of an electron, and $\Delta N_{t-equiv}$ is the change in equivalent trapped charge. If negatively charged bulk oxide traps dominate, and electron trapping mostly occurs near the substrate, the location of the centroid shifts toward the substrate, and a positive shift in flatband voltage takes place. However, if electron trapping near the gate dominates, the centroid moves toward the gate, as shown in the inset in Fig. 8, and this results in a less positive shift in flatband voltage compared to the former case.

Clearly, from Fig. 8 and Eq. 4, the charge centroid due to electron trapping was located near the substrate in the 290-210 K range as ΔV_{FB} steadily increased, but was located near the gate as ΔV_{FB} decreased in the 210-130 K range. As stated earlier, both interface traps and bulk oxide traps contribute to the location of the charge centroid. To investigate interface trap characteristics in detail, we performed a conductance test in the 130-290 K temperature range. The equivalent parallel conductance, G_p, of the MOS capacitor was measured using 20 Hz to 1 MHz test signals for different bias levels. G_p/ω curves with respect to frequency were used to determine the interface state density, D_{it}. Peak D_{it} values for different temperatures are shown in Fig. 9. Because the D_{it} shows a similar turnaround effect, and D_{it} is directly related to the amount of interface-trapped charge, it suggests that interface states strongly contribute to the low-temperature charge trapping characteristics. We also observed that the G_p/ω curves with respect to frequency get wider when the temperature is decreased (not shown) due to the presence of an increased number of active interface trap levels at lower temperatures. We may assume that at the Si/HfO_2 interface all interface states above the intrinsic level E_i are acceptor type and below E_i are donor type.[24] Acceptor-type traps are negatively charged when filled and neutral when empty, whereas donor-type traps are neutral when filled and positively charged when empty. At the flatband condition, the Fermi level E_{fn} is higher than E_i at the Si/HfO_2 interface for n-type substrates, and interface states above E_{fn} and below E_i are neutral.[24] Only the acceptor-type interface traps having energy levels between E_{fn} and E_i capture electrons and get negatively charged and thus contribute to the positive shift of the flatband voltage. Therefore, the concentration of interface states is highest within the energy levels between E_{fn} and E_i at the HfO_2/Si interface. It further confirms that the domination of electron trapping by shallow interface traps near the substrate in the 290-210 K range and near the gate in the 210-130 K range, which subsequently shifted the trapped charge centroid toward the substrate and gate, respectively, may be the principal cause behind the turnaround effect in ΔV_{FB}.

Conclusions

Electrical characteristics of MOS capacitors with thermally evaporated HfO_2 films have been reported. Characteristics such as hysteresis, leakage current density, and flatband voltage shift significantly reduced after 450°C FGA anneal in 50 nm HfO_2 films. Bulk oxide charges decreased after annealing in 50 nm HfO_2 films, whereas they increased for 60 nm films. The interface state density is toward the higher side and moderately increased with annealing. Furthermore, shifts in C-V curves and the turnaround effect in flatband voltage shifts were observed in the 290-130 K temperature range, giving the charge trapping characteristics of HfO_2 films. Even though the films studied in this work are thicker than the thickness required for nanoscale device applications, the electrical properties investigated here suggest that thermally evaporated HfO_2 films can be suitable for MOS device applications with enhanced process optimization.

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