

Screening of Si–H bonds during plasma processing

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Abstract

This work investigates the screening of Si–H bonds at the Si–SiO₂ interface in an n-channel MOSFET due to plasma charging damage. Since CMOS devices are subjected to high field electron injection during plasma processing, this condition was emulated by subjecting the devices to current stress (both gate injection and substrate injection). With the source and drain terminals reverse biased by a screening potential during stress, representing the impact from source and drain antenna, a decrease in stress-induced interface state density formation was noticed. Observed interface state density D_{it} before and after the high field injection, therefore, demonstrates an effective screening of the source and the drain edges. During gate injection the Si–H bond concentration, estimated using a model based on a simple first order kinetic equation, is inversely proportional to measured D_{it} at effective screening potentials. In substrate injection, however, the Si–H concentration does not relate to D_{it} creation. Similar trends were observed for transistors with different antenna ratios. Subsequent hot carrier stress confirms that the screening is mainly due to protected drain edges. These results suggest that effective screening of Si–H bonds is possible during plasma processing.

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1. Introduction

Plasma-induced wafer charging continues to receive considerable attention for CMOS transistors whose size has been drastically reduced due to its scalability. It is well known that the gate oxide of MOSFET experiences stress during plasma processing due to high field electron injection, caused by Fowler–Nordheim tunneling. Depending upon the plasma potential distribution on the surface of the wafer, the injection could be either substrate or gate injection [1–3]. In addition, plasma charge damage effects can be enhanced or exacerbated depending upon the direction, distance and size of the antennas connected to the drain, gate, source and substrate [4–6]. If these antennas are connected to source and drain (S/D) junctions, it can affect the damage magnitude of the CMOS gates significantly. It is because the floating potentials generated at these terminals can induce significant damage even with minimal non-uniformity in the

plasma. A reverse biased voltage at the source and drain termed as screening potential, to simulate the impact of source and drain antenna, was applied at the S/D junctions while the devices were subjected to a current stress. The depletion region extension to channel region at the source and drain edges can impact the device degradation. It is well known that the generation of Si dangling bonds during current stress contributes partly to the degradation of Si–SiO₂ interface [7–9]. However the processes that are responsible for the creation of Si dangling bonds during plasma damage processes have been the subjects of on-going investigations. In this paper, we have attempted to understand the variation of Si–H bond concentration at the Si–SiO₂ interface under high field stress when a screening potential exists. The devices were further subjected to hot electron stress after high field stress to confirm the effectiveness of screening on Si–H bonds at the drain edge.

2. Experimental setup

The wafers studied in this work consisted of nMOS transistors processed using 0.25 μm CMOS technology.

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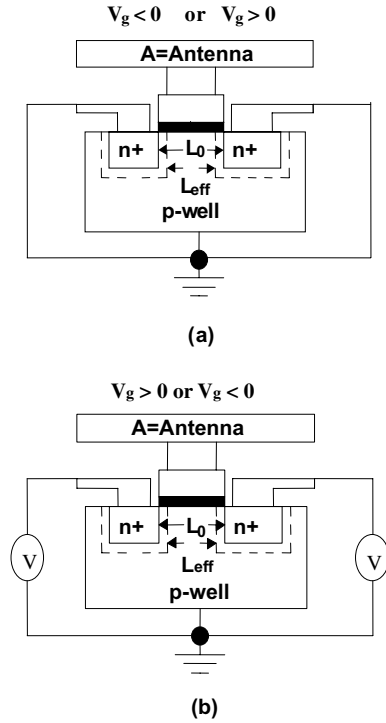


Fig. 1. The cross-sectional view of n-MOSFET (a) in a typical stressing condition (b) with source and drain at a screening potential.

Transistors had a channel area of $0.35 \mu\text{m}^2$ and thickness of the gate oxide was 6 nm. The schematic in Fig. 1(a) shows a typical injection mode used to evaluate the oxide integrity where all the source/drain and substrate terminals are connected together to form a common ground. The transistor parameters, threshold voltage and transconductance values were measured before stress and was seen to be quite uniform. Three groups of transistors based on antenna ratios viz. 2009, 10060 and 50050 were subjected to about 30 mA/cm^2 constant current stress for 3 s using gate injection and substrate injection mode. Screening effect at the junctions were studied by applying voltages of 0, 1, 1.5, 2 and 3 V at the source and the drain terminals when the current stress was applied at the gate using a setup as shown in Fig. 1(b). Charge pumping current (I_{cp}) was measured with gate pulses having a frequency $f = 1 \text{ MHz}$, rise and fall times $t_r, t_f = 100 \text{ ns}$ and amplitude = 0.1 V, with source and drain terminals reverse biased at 50 mV. The currents were measured for all groups of devices before and after the DC stress. Interface state density was calculated from the measured charge pumping current values. Following the current stress the devices were subjected to hot carrier aging stress using maximum substrate current. The interface trap density D_{it} was measured again using the charge pumping technique [10–12].

3. Concentration estimation

Based on the D_{it} values obtained experimentally, the concentration of Si–H bonds are then estimated based on a simple power law and kinetic equation [13,14]

$$D_{it} - D_{it0} = n_0 / (1 + (kt)^{-\alpha}) \quad (1)$$

where D_{it} and D_{it0} are final and initial interface state densities, n_0 is the initial concentration of Si–H bonds for the time dependence trap generation t , k is the reaction constant and α is a constant. It is also noted that $\alpha > 0.5$ for negative gate biases and $\alpha < 0.5$ for positive biases.

Evaluation of the reaction constant k is based on the nature of the stress i.e. DC stress or hot carrier stress. Reaction constant k is given by the formula

$$k = k_0 \exp(-\varepsilon_a / k_B T) \quad \text{for high field injection and}$$

$$k = k_0 \exp(-\varepsilon_a / k_B T) k_H \quad \text{for hot carrier degradation, where}$$

$$k_H = 1 + \delta_{HC} |I_{HC}|^{\rho_{HC}}$$

Expression for ε_a is evaluated based on the formula

$$\varepsilon_a = \varepsilon_{a0} + \beta \cdot k_B T \ln(D_{it} / D_{it0}) \quad \text{for high field and}$$

$$\varepsilon_a = \varepsilon_{a0} + \delta |F|^\rho + \beta \cdot k_B T \ln(D_{it} / D_{it0})$$

for hot carrier injection

β is approximately assumed to be twice of α for high field injection while it is evaluated to be $\beta = 1 + \beta_\perp F_\perp$ where F_\perp is the polarity dependent perpendicular component of the electric field at the interface for hot carrier stress and δ, ρ are fitting parameters. All calculations were based on the room temperature 300 K. Activation energy of 2 eV that dissociates hydrogen from the interface was used in our estimation.

4. Results and discussion

Fig. 2 shows the variation in interface state density $\Delta D_{it} / D_{it}$ of all groups of devices after being exposed to current stress with the applied screening potential under gate injection. It is seen that the screening effect is prominent for a wider range of screening voltage for transistors with the smallest antenna ratio (2009) and most effective (lowest D_{it}) at 2 V approximately. The most effective screening potential gradually decreases, as the antenna ratio becomes larger. For antenna ratios 10060 and 50050 the most effective screening potentials are 1.7 and 1.5 V respectively. An increase in antenna ratio suggests that the devices had increased plasma damage i.e. higher pre-existing oxide traps prior to current stress. These traps influence the value of effective

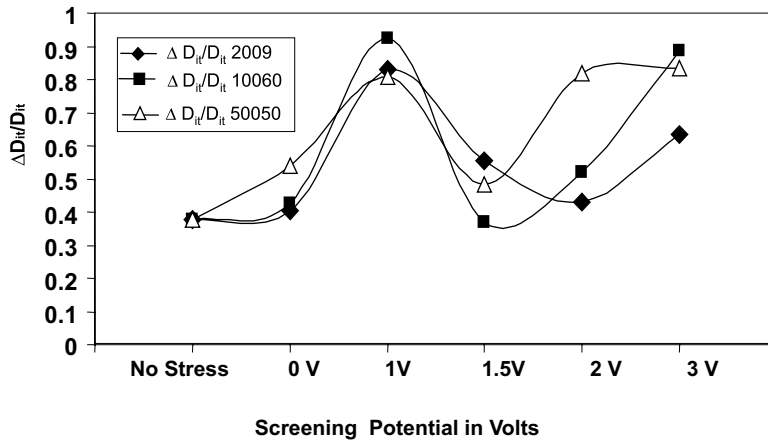


Fig. 2. Normalised interface state densities for applied screening potentials for various antenna ratios in gate injection.

screening potential for higher antenna ratio devices. D_{it} at the effective screening potential goes through a significant reduction as the interface at source and drain edges were prevented from further damage during stress. This is because the lateral depletion width will vary accordingly to screen the source and drain edges considering that the doping concentration of the n-region of the lightly doped drain (LDD) and the channel is constant.

At lower screening potentials the depletion width is not significant enough to screen the source/drain edge whereas when the screening potential is increased to a very high value the field across the oxide reaches a near-breakdown field. This near-breakdown potential causes an increase in D_{it} and the trapped charges near the drain edge. For screening potentials less than this breakdown potential, channel is effectively screened reducing the interface states. For a larger antenna ratio, the near-breakdown screening potential is comparatively lower,

because the transistors have higher pre-existing trapped charge at the interface as described earlier.

For substrate injection (Fig. 3), it is seen that the variation in interface state density $\Delta D_{it}/D_{it}$ for all antenna ratios does not change significantly for the applied screening potentials. The screening is not very effective for substrate injection. The source and drain depletion region has minimal effect as the injection process is mostly due to thermally generated electrons from the channel. In case of gate injection, on the other hand, more electrons are available at the heavily doped poly Si–SiO₂ interface as compared to substrate injection.

Fig. 4(a)–(c) shows the concentration of Si–H bonds for antenna ratio 2009, 10060 and 50050 as a function of screening potential immediately after the DC stress for gate injection. We have plotted $\Delta D_{it}/D_{it}$ in the same figure to observe the relationship of D_{it} with that of Si–H bonds at different screening potentials. It is noticed from the trend that with increase of screening potential when

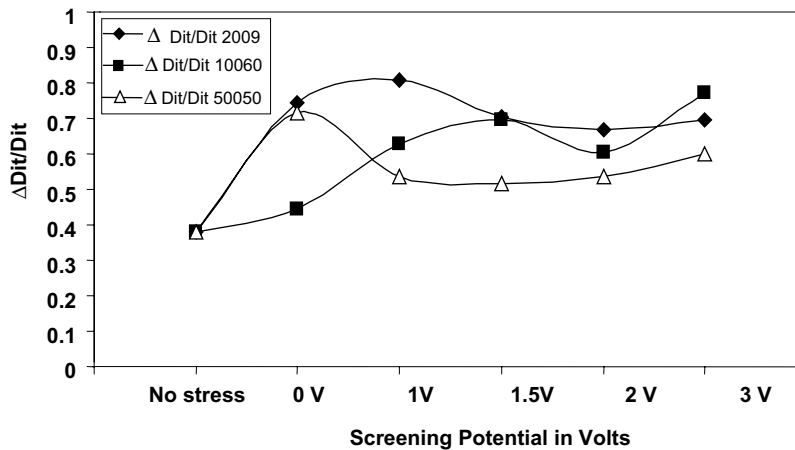


Fig. 3. Normalised interface state densities for applied screening potentials for various antenna ratios in substrate injection.

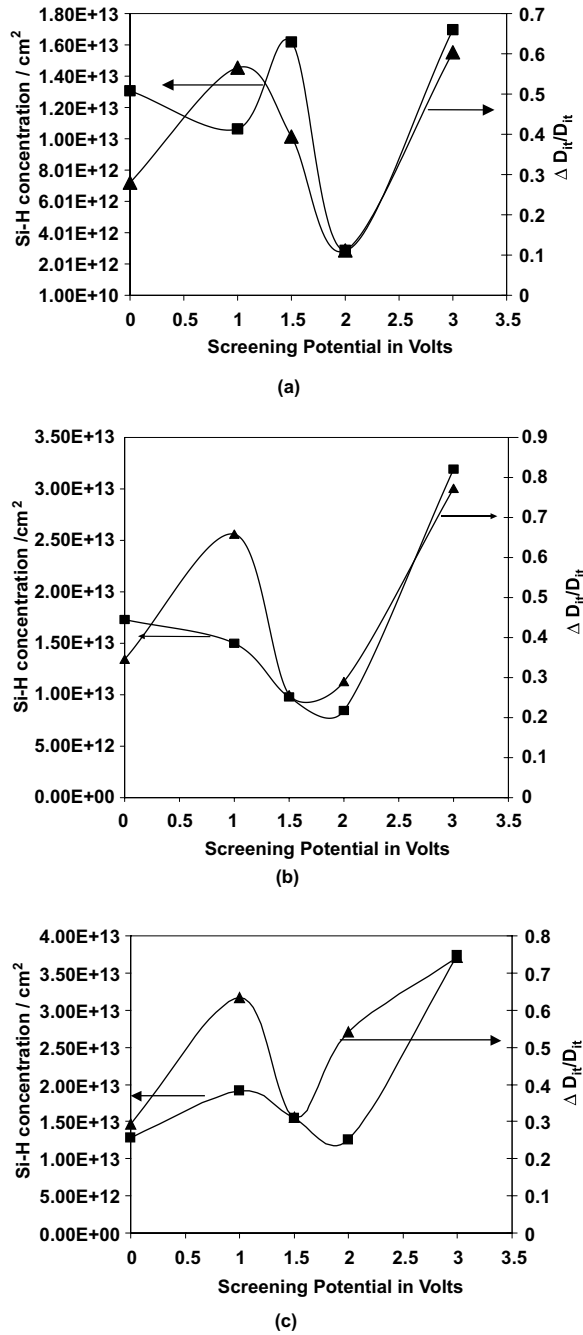
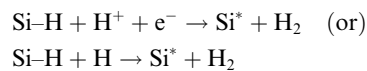


Fig. 4. Si–H bond concentration [■] and $\Delta D_{it}/D_{it}$ [▲] as a function of screening potential for gate injection (a) for antenna ratio 2009, (b) for antenna ratio 10060 and (c) for antenna ratio 50050.

D_{it} increases, Si–H concentration decreases for all groups of devices. It is expected because interface state density is directly proportional to concentration of Si dangling bonds at the interface. During the gate injection, electron–hole pairs are being generated at the Si–SiO₂ interface (anode), which react with Si–H bonds. In

this reaction, hydrogen (H: atom and H⁺: ion) is released breaking the Si–H bonds creating interface traps as described in the following equation.



where Si^* represents the Si dangling bond. At very high screening potentials (>2 V), D_{it} does not follow Si–H bond concentration for most of devices, which indicates that possible formation of electrically active border traps contribute significantly to D_{it} rather than Si dangling bonds. The depletion layer formation at the source and drain edges due to screening potential shields the source and drain edges from possible damage to the interface.

The depletion lengths, formed due to reverse biased voltages at source and drain, are W_S and W_D respectively. W_S or W_D is given by $[\{2\epsilon_0\epsilon_{Si}(V_{bi} + \psi_S + V_{D,S} - 2kT/q)\}/qN_A]^{1/2}$ where ϵ_0 is the free space permittivity, ϵ_{Si} is the silicon dielectric constant, V_{bi} is the built-in potential between the source/drain and substrate junction, ψ_S is the surface potential, $V_{D,S}$ is the screening potential, k is

Boltzmann’s constant, T is the temperature, q is electronic charge and N_A is the substrate doping. Formation of interface traps is reduced due to the protection by the depletion layer resulting in reduced D_{it} values.

Fig. 5(a)–(c) shows the concentration of Si–H bonds for antenna ratios 2009, 10 060 and 50 050 as a function of screening potential immediately after the DC stress for substrate injection. $\Delta D_{it}/D_{it}$ values are plotted along with secondary axis for comparison. Unlike the case of gate injection, the Si–H bond concentration does not follow the change in D_{it} during screening. For substrate injection, electron–hole pairs are generated at the gate– SiO_2 interface (anode) and hence there is no direct impact on the Si–H bond concentration at the Si– SiO_2 interface. Possible formation of depletion layer around the source and drain areas is ruled out during screening because a channel is formed during substrate injection. Therefore, the interface may not be effectively protected from possible damage. For substrate injection during screening, the dominant mechanism that contributes to D_{it} may not be due to Si–H bond breaking but may be due to creation of electrically active border traps that contribute to interface state density.

Hot carrier stress was applied to the devices to further understand the effectiveness of screening of Si–H bonds during gate injection. Two dominant mechanisms [15] play key roles at the interface during hot carrier degradation—the donor or the acceptor sites are being neutralized in the oxide affecting the interface trap generation and release of interfacial hydrogen that contributes to interface traps. Fig. 6 shows the change in concentration of the Si–H bonds after hot carrier stress in transistors with an antenna ratio of 2009 that were subjected to DC stress in gate injection mode at different screening potentials. The increase in Si–H bond concentration between 1 and 2 V of screening potential to a no-stress level suggests that under effective screening,

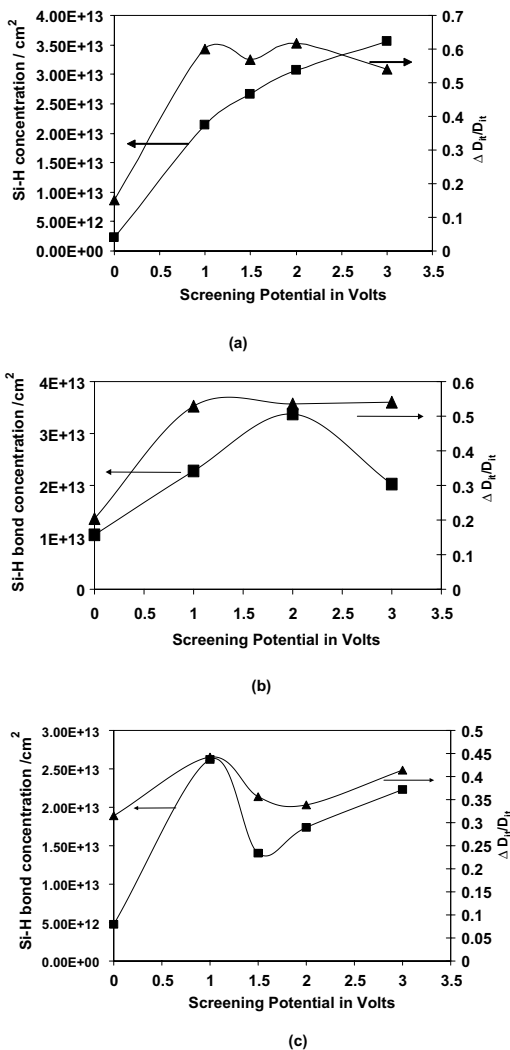


Fig. 5. Si–H bond concentration [■] and $\Delta D_{it}/D_{it}$ [▲] as a function of screening potential (a) for antenna ratio 2009, (b) for antenna ratio 10060 and (c) for antenna ratio 50050.

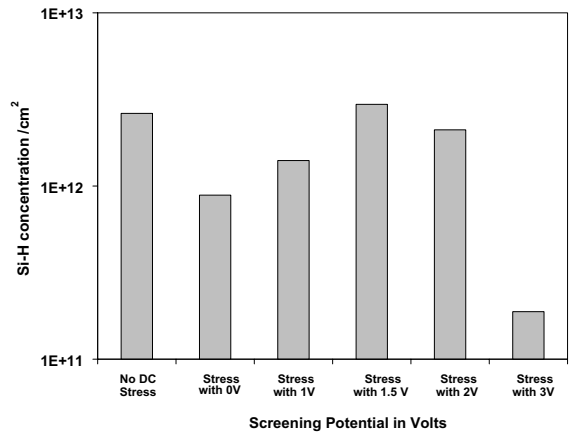


Fig. 6. Si–H bond concentration after hot electron stress for gate injection of antenna ratio 2009.

the interface near drain junctions are protected which helped to reduce the Si–H bond-breaking phenomenon. This further confirms the screening of Si–H bonds under these screening potentials during stress.

5. Conclusions

The impact of potentials developed due to the source and drain antenna during plasma processing, has been simulated by a reverse biased screening potential. It was observed that the screening potential could shield the Si–H bonds effectively during gate injection. It is also observed that the screening of Si–H bonds during plasma conditions depends on various parameters, namely, the size of the antenna ratios (2009, 10 060 and 50 050), the polarity of the stress involved (gate and substrate injection) and the gate oxide quality. Hot electron stress further confirms the screening effect on these transistors. Hence it is important to consider the vulnerability of the device due to source and drain antennas during VLSI processing.

Acknowledgements

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References

- [1] Cellere G, Valentini MG, Pantisano L, Cheung KP, Paccagnella A. Different nature of process-induced and stress-induced defects in thin SiO₂ layers. *IEEE Trans Electron Devices* 2003;24:393–5.
- [2] Misra D. Effect of reverse biased voltage at source and drain on plasma damage. *IEEE Trans Electron Devices* 2002;49:1090–3.
- [3] Cheung KP, Misra D, Colonell JI, Liu C-T, Ma Y, Chang C-P, et al. Plasma damage immunity of thin gate oxides grown on very lightly N-implanted silicon. *IEEE Electron Device Lett* 1998;19(7):231–3.
- [4] Cheung KP, Misra D. Effect of source and drain junctions on plasma charging. *Semicond Sci Technol* 1998;13:529–38.
- [5] Aum PK, Brandshaft R, Brandshaft D, Dao TB. Controlling plasma charge damage in advanced semiconductor manufacturing. Challenge of small feature size device, large chip size, and large wafer size. *IEEE Trans Electron Devices* 1998;45:722–30.
- [6] Cheung KP, Misra D, Steiner KG, Colonell JI, Chang C-P, Lai W-Y-C, et al. Is NMOSFET hot carrier lifetime degraded by charging damage? In: 2nd Int Sympos Plasma Process-induced Damage, vol. 13, 1997. p. 186–8.
- [7] Hu C, Tam SC, Hsu FC, Ko P-K, Chan TY, Terrill KW. Hot-electron induced MOSFET degradation-model, monitor and improvement. *IEEE Journal of Solid State Circuits* 1985;20(1):295–305.
- [8] Takeda E, Yang CY, Miura-Hamada A. Hot carrier effects in MOS devices. San Diego, CA: Academic; 1995.
- [9] Cartier E, Stathis JH. Hot-electron induced passivation of silicon dangling bonds at the Si(1 1 1)/SiO₂ interface. *Appl Phys Lett* 1996;69:103–5.
- [10] Heremans P, Witters J, Groeseneken G, Maes HE. Analysis of the charge pumping technique and its application for the evaluation of MOSFET degradation. *IEEE Trans Electron Devices* 1989;36:1318–35.
- [11] Mahapatra S, Parikh CD, Ramgopal Rao V, Viswanathan CR, Vasi J. A comprehensive study of hot-carrier induced interface and oxide trap distributions in MOSFETs using a novel charge pumping technique. *IEEE Trans Electron Devices* 2000;47(1):171–7.
- [12] Schroder DK. *Semiconductor Material and Device Characterization*. 2nd ed. Wiley Interscience Inc.; 1998. ISBN 0-471-24139-3.
- [13] Penzin O, Haggag A, McMohan W, Eugeny Lyumkis, Hess K. MOSFET degradation kinetics and simulation. *IEEE Trans Electron Devices* 2003;50(6):1445–50.
- [14] Stesmans A. Dissociation kinetics of hydrogen-passivated P_b defects at the (1 1 1)Si/SiO₂ interface. *Phys Rev B* 2000; 61:8393–403.
- [15] de Schrijver E, Heremans P, Bellens R, Groeseneken G, Maes HE. Post-stress interface trap generation: a new hot-carrier induced degradation phenomenon in passivated n-channel MOSFET's. In: *Int Rel Phy Sympos*, vol. 112, 1992. p. 112–5.