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Gate electrode effects on low-frequency (1/*f*) noise in p-MOSFETs with high-κ dielectrics

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Abstract

The defects related to the gate–dielectric in high-κ-MOSFETs are studied using the 1/*f* noise technique. Three different types of gate electrodes were used for this purpose – poly-Si, metal (TiN/TaN) and fully Ni Silicided (FUSI) electrodes with Hf-based oxides as the gate dielectric layer. All the three types of devices show a specific behavior near the gate electrode–dielectric interface when the trap profiles are assessed using $f \times S_I$ spectra. The tunneling depths were calculated and it was found that the high-κ oxide (bulk) layers are being probed. From the drain current spectra S_I vs. drain current I_D of the various gate material devices at given depths, it may be inferred that the concentration of oxygen-vacancy-related defects can significantly influence the 1/*f* noise performance, which can explain the differences observed in noise between the gate electrodes. Comparison of FUSI gated devices, with various percentages of Hf in the dielectric layer, shows comparable noise levels (S_{VG}), indicating a minor dependence on Hf-content in the gate dielectric layer.

Keywords: Low-frequency noise; Hafnium silicates; Poly-Si gate; Metal gates; FUSI; Trap profile; High-κ dielectric

1. Introduction

While a major consensus on Hf-based dielectrics as a short- to mid-term replacement dielectric for SiO_2 is growing, a number of reliability and operational problems still exists [1–4] mainly related to intrinsic material quality of these dielectrics. A further EOT reduction is achieved by the introduction of metal gates as the gate electrode material since the depletion effects of polycrystalline (poly-)Si gate electrode material have a significant effect on the EOT in inversion. Various characterization methods have been employed to describe the quality of high-κ dielectric layers. One of the potential characterization techniques is 1/*f* noise [5,6]: the current fluctuations caused by trapping–detrapping events can yield information on the defectiveness of the gate stack since these events occur within a few nm from the silicon interface.

Some researchers have carried out a comprehensive investigation on the impact of 1/*f* noise in high-κ dielectrics and it has been found that the noise levels typically are higher by an order of magnitude in high-κ-based devices [7–9]. The effect of various processing parameters such as the high-κ deposition technique, the HfO_2 thickness and the presence of a SiO_2 interfacial layer (IL) on the 1/*f* noise has been studied in detail [10,11].

However, as in most cases it is inevitable of retaining SiO_2 as an interfacial layer dielectric, various complications arise due to the presence of different interfaces in the gate stack as schematically shown in Fig. 1 – Si–IL (SiO_2)

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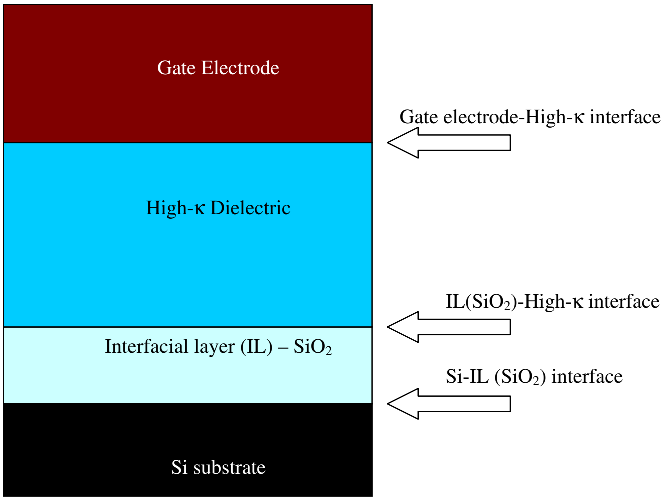

Fig. 1. Possible interfaces in a MOSFET with a high-κ gate dielectric.

interface, IL (SiO_2)–high-κ interface, high-κ–gate electrode interface. While Si–SiO_2 is a well-understood interface, the impact of the properties/quality of the other two interfaces needs further investigations. As $1/f$ noise has the ability to probe the device deeper into the oxide, it can be used as an effective tool to study noise related defects near or at the high-κ–gate electrode interface depending on the physical thickness of the layers. This paper reports the outcome of an initial study to get a better insight into the high-κ–gate electrode related defects in the vicinity of the high-κ–gate electrode interface, using $1/f$ as a diagnostic tool.

The noise investigations are performed for devices with three different gate electrode materials: poly-Si, metal (TiN–TaN) and Fully Ni Silicide (FUSI). These electrode materials enable a tuning of the work function, while the poly-Si allows to take into consideration the Fermi-level pinning at the gate electrode–dielectric interface. The value of the frequency exponent γ in $1/f^{\gamma}$ is investigated for these gate electrodes. The trap profiles of these devices were studied using frequency $f\times$ drain current noise S_I spectra, as a confirmation to the observed variation in frequency exponent γ. The gate electrode deposition and subsequent processing is then related to the concentration of oxygen vacancies in the bulk high-κ dielectric layer close to the gate electrode–dielectric interface and its role on $1/f$ noise is deduced. The impact of the composition of the high-κ dielectric layer is also studied for FUSI gates in detail and dependences observed have a much lower effect than the gate electrode itself.

2. Experimental

P-channel MOSFETs fabricated using a conventional CMOS process flow, with SiON (2.0 nm), pure HfO_2 and with various SiO_2/HfO_2 ratios classified as (I) silicon-rich (higher percentage of SiO_2), (II) hafnium-rich (higher percentage of HfO_2) and (III) equal amount of hafnium–silicon were considered as gate dielectric to study the trap profiles in $W/L = 10/1$ (μm) devices. A metal organic chemical vapor deposition (MOCVD) process was used to deposit the gate dielectrics. A 0.8 nm thin interfacial chemical oxide layer (IMEC clean) based on ozone chemistry was employed in all these devices prior to the high-κ gate dielectric deposition.

Three different gate electrode materials were considered to study the effects related to the gate electrode–dielectric interface: N-doped polysilicon (poly-Si) using phosphorus as the dopant material, TiN–TaN (metal) and fully NiSi (FUSI) gates. In the case of metal gates, TaN was the metal gate electrode while TiN acts as the capping layer – both deposited by physical vapor deposition (PVD). To study the effects of the composition of the underlying high-κ dielectric layer on the gate dielectric–electrode interface, the percentage of Hf was varied from 0% to 53% and 65% in the FUSI gate devices.

The physical thicknesses of the various high-κ dielectrics for p-MOSFETs and the estimated EOT of all devices studied are given in Table 1a. They all received a post-deposition anneal in NH_3 at 800 °C for 60 s before gate electrode deposition. A forming gas anneal (FGA) at 520 °C for 20 min was employed once the gate electrodes were formed. Dopant activation anneal was performed at 1000 °C and <1 s.

Table 1a
Estimated EOT values, physical thickness and tunneling depths of the devices studied for comparison of gate electrodes with dielectrics of various composition

Sl	Gate	Gate dielectric	Physical thickness (±0.1 nm)	EOT (±0.1 nm)	Estimated tunneling depths z (nm)
1	Poly	SiON	1.5	~1.60	2.01
		23% Hf	2.8	1.75	2.10
		47% Hf	2.8	1.47	2.35
		HfO_2	~2.8	1.90	2.60
2	Metal (TiN–TaN)	30% Hf	2.8	1.39	2.15
		55% Hf	2.8	1.46	2.34
		70% Hf	2.8	1.65	2.45
		HfO_2	2.8	1.39	2.60
3	FUSI (NiSi)	SiON	2.2	1.80	2.01
		53% Hf	3	1.35	2.30
		65% Hf	3	1.18	2.43

On-wafer noise measurements were performed in linear operation at a constant drain voltage $|V_{DS}| = 0.05$ V for gate voltages $|V_{GS}|$ of 0.5–2 V in steps of 50 mV using BTA9812 hardware and NoisePro software from Cadence. A channel length of 1 μm was chosen, to reduce device-to-device scatter in the noise magnitude.

3. Results and discussion

Fig. 2 shows the I_D–V_G and G_M–V_G characteristics of TiN–TaN (metal), poly-Si, NiSi (FUSI) gate electrodes of ~55% Hf-silicate gate dielectric oxides. A higher V_T shift and lower G_M is observed for poly-Si MOSFETs while metal and FUSI performances are quite comparable, which is mainly attributed to a work-function shift of the gate electrode material [12].

Figs. 3–5 represent the $f \times S_I$ vs. frequency f at $|V_G - V_T| = 0.1$–0.2 V and $|V_{DS}| \sim 0.05$ V, for p-MOSFETs with the different gate electrode materials studied (metal/poly-Si/FUSI), with every plot showing the performance for various Hf %. For the $f \times S_I$ spectra the translation of the frequency axis into a tunneling distance z is also indicated along a second x-axis, for some average composition x. Assuming a pure tunneling model for the trapping and neglecting the interfacial layer, the tunneling depth z can be calculated from [13]

$$\frac{1}{2\pi f} = \tau_0 \exp(\alpha_t z) \tag{1}$$

with τ_0 the tunneling time constant ($\sim 10^{-10}$ s) at the Si-oxide interface and α_t [13,18] the tunneling parameter, given by

$$\alpha_t = \sqrt{[(2m_h^* \phi_b)/\hbar^2]} \tag{2}$$

where $\hbar$ is Planck's constant divided by 2π. The tunneling parameter α_t is estimated semi-empirically from the expected values of the effective tunneling hole mass (m_h^*) in the dielectric and the potential barrier for hole emission at the silicon–oxide interface (ϕ_b), which varies with composition x.

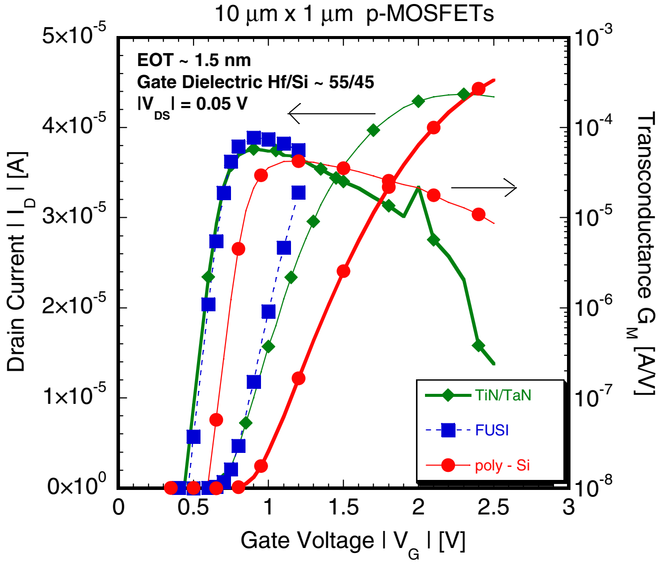

Fig. 2. Drain current $|I_D|$ [A] vs. gate voltage $|V_G|$ [V] and transconductance G_M [A/V] vs. gate voltage $|V_G|$ [V] characteristics of TiN–TaN, FUSI and poly-Si gate p-MOSFETs for 55% Hf-silicate gate oxides.

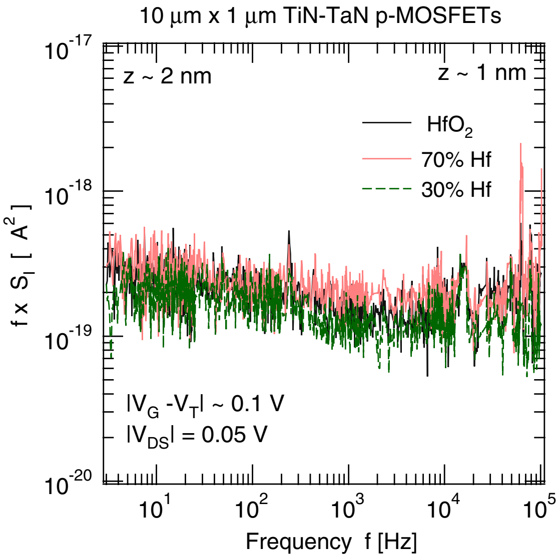

Fig. 3. Qualitative trap profile $f \times S_I$ [A^2] vs. frequency f [Hz] at $|V_G - V_T| \sim 0.1$ V of metal gate p-MOSFETs for various Hf-silicate gate oxides.

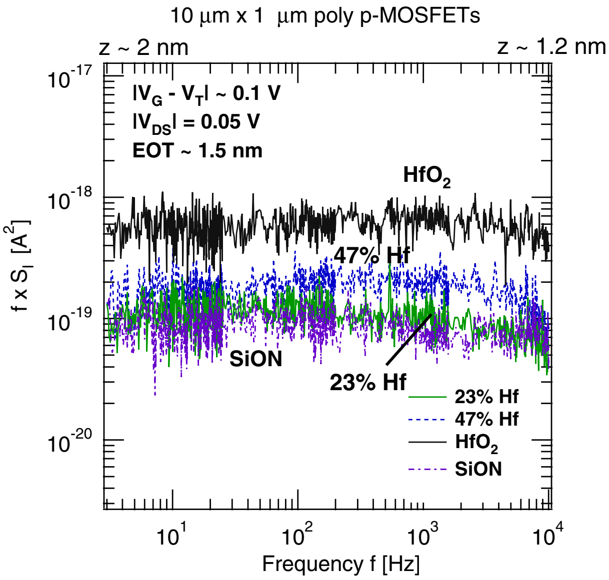

Fig. 4. Qualitative trap profile $f \times S_I$ [A^2] vs. frequency f [Hz] at $|V_G - V_T| \sim 0.1$ V of poly gate p-MOSFETs for various Hf-silicate gate oxides.

Assuming a Si/HfO$_2$ interface, the barrier height for the holes is taken as 3.4 eV for HfO$_2$ [14] while the effective hole mass in Si is taken as $0.15m_0$ [15], with m_0 the rest mass of the electron. The tunneling coefficient for holes is then estimated to be roughly 0.72×10^8 1/cm for the

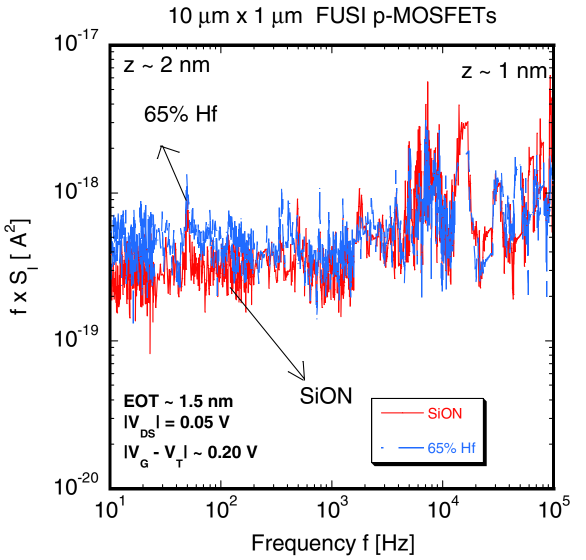

Fig. 5. Qualitative trap profile $f \times S_I$ [A^2] vs. frequency f [Hz] vs. f at $|V_G - V_T| \sim 0.2$ V of FUSI gate p-MOSFETs for various Hf-silicate gate oxides.

Si/HfO$_2$ system while it is $\sim 0.86 \times 10^8$ 1/cm for the Si/SiO$_2$ system [16]. For an intermediate Hf composition, α_t is interpolated by assuming a linear variation with x in barrier height from 3.4 eV to 4.4 eV for the HfO$_2$ and the SiO$_2$ system, respectively. The estimated tunneling depths at $f = 25$ Hz are also given in Table 1a for the devices studied.

It is also noted that these spectra roughly correlate with trap density profiles in the oxide, though accurate capacitance equivalent thickness (CET) values need to be considered. The impact due to the gate electrode material is clearly seen when Figs. 3–5 are compared.

The SiON devices are probed very close to the gate–dielectric interface as the physical thickness of the devices is ~ 2.0 nm, while for Hf-oxide devices, the tunnel depths at low frequencies indicate that one is probing the bulk of the high-κ layer close to the gate electrode–dielectric interface.

The three sets of devices with different gate electrodes (Figs. 3–5) show different qualitative trap profiles with tunneling depth. While the metal gate devices (Fig. 3) give higher values in the high-κ layer (lower frequency values) and at the interfacial layer of the device, a constant value is observed throughout the oxide and at the interface in the case of poly-Si electrodes (Fig. 4). FUSI gates behave differently, where the lowest values were seen to be in the bulk high-κ layer and an increasing trend is observed towards the substrate–dielectric interface.

The frequency exponent γ of the observed $1/f^\gamma$ behavior was also studied and was observed to change as $\gamma \sim 1$ for poly-Si, $\gamma > 1$ for TiN–TaN while for FUSI it is $\gamma < 1$. Christensson et al. [13] and Surya and Hsiang [17] have already shown in SiO$_2$ devices that the deviation in γ relates to the distribution of traps across the bandgap. If $\gamma < 1$, there is a greater number of high-frequency traps and the trap distribution is skewed towards the IL–Si interface, while for $\gamma > 1$, there is a greater number of low-frequency traps where the trap distribution is skewed away from the interface [18–20]. In our case on high-κ devices, FUSI gates ($\gamma < 1$) and TiN–TaN metal gates ($\gamma > 1$) emulate the behavior respectively. Alternatively, the behavior of the frequency exponent in these devices can also be regarded as a confirmation to the profile distribution observed from the $f \times S_I$ spectra as in Figs. 3–5.

The possible influence of gate electrode material on the properties of the high-κ layer near the gate electrode/high-κ interface and, therefore, on the $1/f$ noise parameters is also studied. Fig. 6 shows the drain current noise S_I vs. drain current $|I_D|$ of the three types of gate electrodes for a high-κ gate oxide of ~55% Hf. The fit shows that for all the cases S_I is proportional to I_D^2, indicating that the noise mechanism could be related to trapping effects in the oxide following the number fluctuation (ΔN) theory. The drain current noise S_I is found to be lower for FUSI and metal gates when compared to poly-Si, which correlates with the transconductance G_M and threshold voltage V_T in these devices (Fig. 2).

From Figs. 2–6, it is inferred that the gate electrode material has a significant impact on $1/f$ noise and on the behavior of trap profiles when considering equivalent energy levels. For poly-Si (Fig. 4), it is seen that HfO$_2$ has comparatively higher values in the $f \times S_I$ spectra while Hf-silicates have values in between SiON and HfO$_2$. This difference is not noticeable in the case of metal gates (Fig. 3), while the differences are found to be smaller in the case of FUSI gate devices (Fig. 5).

For the poly p-MOSFET case, Fig. 4 – which shows the $f \times S_I$ spectra for different compositions of x, it may be

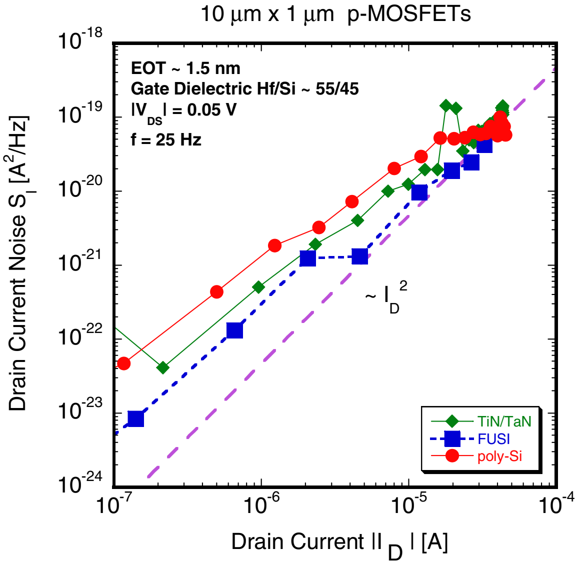

Fig. 6. Drain current noise spectral density S_I [A^2/Hz] vs. drain current $|I_D|$ [A] characteristics of TiN–TaN, FUSI and poly-Si gate p-MOSFETs for 55% Hf-silicate gate oxides.

possible that the defect centers related to oxygen vacancies may have different concentrations depending on the Hf composition. Fleetwood et al. [21,22] have shown that these *E*′ defect centers have an impact on $1/f$ noise in SiO_2. Although it has been recently reported that these defect centers have a higher concentration in Hf-based oxides [23,24], their complete role is currently still under further investigations. It is quite well known that the high-κ layer, which is generally considered more defective than SiO_2, has a lower affinity towards oxygen and the Gibbs free energy for $HfO_2 + Si$ is smaller [25]. Hence it may be possible that during gate electrode processing a higher oxygen out-diffusion to the interfaces occurs leading to a high vacancy concentration and, therefore, resulting in more oxygen related defects in the HfO_2 case. The oxygen vacancy concentration is expected to be higher in HfO_2 than Hf-silicates because of the higher Hf concentration in the bulk high-κ layers. The fact that no pronounced differences are observed in the case of FUSI or metal gates may be due to the possible impact of the gate electrode material on the oxygen related defects, as explained below.

Considering the HfO_2 (or a 55% Hf) case for the three gate electrodes, a higher O_2 transport (out-diffusion) is possible in the case of poly-Si gate electrodes due to a greater probability of a $HfO_2 + Si$ reaction, whereas this may be less applicable for FUSI gate devices due to the lower Si content in the gate electrode and not applicable at all in the case of a metal gate. Hence oxygen transport may be retarded or inhibited during the metal gate deposition process in the case of metal and FUSI gates leading to a lower concentration of oxygen related defect centers in the high-κ oxide. Due to these lower densities one observes a lower $1/f$ noise compared to poly-Si as seen in Fig. 6.

This behavior is found to be quite consistent with a similar study conducted by Yu et al. [26], where they observed the influence of two types of FUSI gate electrodes (NiSi and NiSiGe) on the oxygen transport in HfSiON-based high-κ devices.

It has to be mentioned that although we observed in the past more scattering related effects in the case of metal gate p-MOSFETs [27], the assumption of a tunneling model for metal gate electrode p-MOSFETs is here taken into consideration only to enable a comparison between the three gate electrode materials. Recently, a similar study by another group attributes $1/f$ noise in metal gate p-MOSFETs to number fluctuation theory [28], in which case, the tunneling model is applicable. The present data does not allow to make a conclusive decision.

Fig. 7 shows the log–log plot of the input-referred noise S_{VG} (S_I/G_M^2) vs. the gate voltage overdrive $|V_G - V_T|$ of poly-Si, metal and FUSI gates for oxides with ∼55% Hf. The S_{VG}'s have a parabolic nature with an increasing trend in all the three cases at higher gate voltages. This is believed to be partly due to an increased gate leakage current at higher gate voltage overdrives as shown in the inset of Fig. 7. Gate current noise measurements and a correlation between drain and gate current noise would help to confirm this hypothesis. The input-referred noise is seen to be the lowest in the case of FUSI gate devices while poly-Si gate p-MOSFETs have the highest input referred noise values. This is attributed to both higher G_M and lower S_I values of FUSI devices.

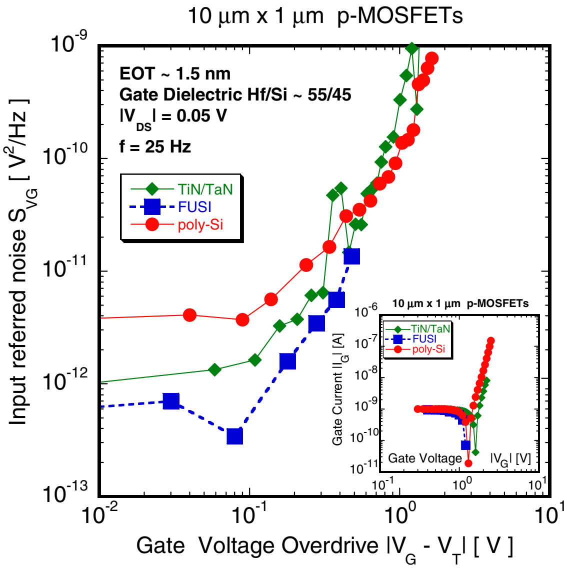

Fig. 7. Input referred noise S_{VG} [V^2/Hz] vs. gate voltage overdrive $|V_G - V_T|$ [V] characteristics of TiN–TaN, FUSI and poly-Si gate p-MOSFETs for ∼55% Hf-silicate gate oxides. (Inset) Gate leakage $|I_G|$ [A]–gate voltage $|V_G|$ [V] characteristics of TiN–TaN, FUSI and poly-Si gate p-MOSFETs for 55% Hf-silicate gate oxides.

In order to investigate the possible influence of the composition of the underlying high-κ dielectric layer on the $1/f$ noise, various percentages of Hf in the high-κ dielectric layer were studied for FUSI gates. From the $S_I - I_D$

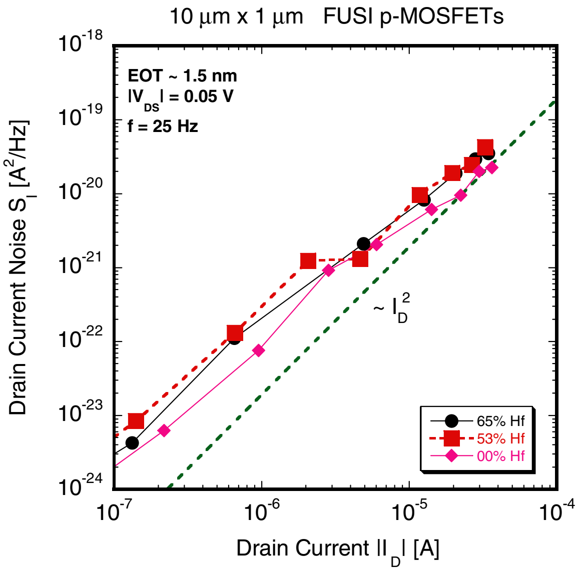

Fig. 8. Drain current noise spectral density S_I [A^2/Hz] vs. drain current $|I_D|$ [A] characteristics of FUSI gate p-MOSFETs for various Hf-silicate gate oxides.

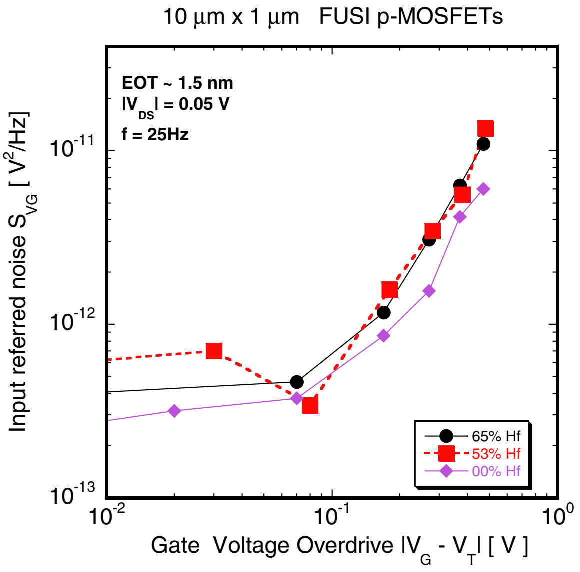

Fig. 9. Input referred noise S_{VG} [V^2/Hz] vs. gate voltage overdrive $|V_G - V_T|$ [V] characteristics of FUSI gate p-MOSFETs for various Hf-silicate gate oxides.

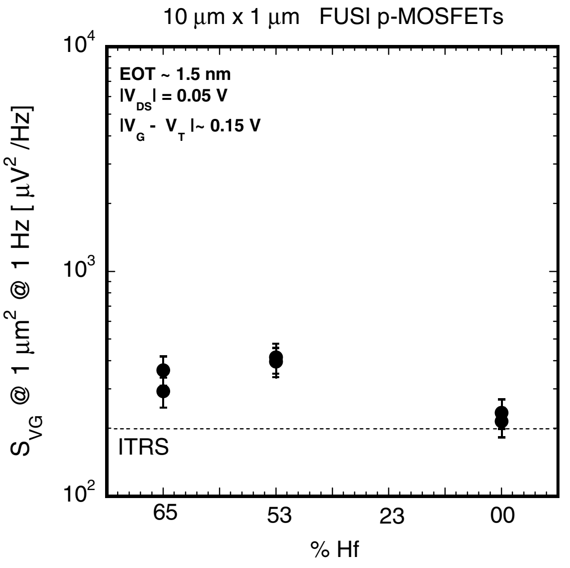

Fig. 10. Input referred noise S_{VG} [V^2/Hz] vs. % HfO_2 of FUSI gate p-MOSFETs at $|V_G - V_T| \sim 0.15$ V.

characteristics in Fig. 8, it looks like that this parameter has little or no effect on the 1/*f* noise. This is confirmed by the input referred noise of Fig. 9 showing a very weak or no dependence on Hf-content while the reference SiON transistors have somewhat lower values. These results are found to be quite consistent with the explanation given above relating to oxygen-vacancy-related defects and their effect on the high-κ gate stack composition.

Combining the results of all the samples in the S_{VG} vs. % Hf plot at $|V_G - V_T| \sim 0.15$ of Fig. 10, the values are seen to be more or less comparable among various Hf-content devices, while for SiON, a slightly lower value is noticed. The latter meets the ITRS specification of 200 µV^2/Hz. From these results, it is seen that there is a weak or no correlation between the Hf-content and the 1/*f* noise magnitude in FUSI gate p-MOSFETs.

Assuming a trapping origin of the 1/*f* noise, an effective volume trap density N_T can be estimated from the values of S_{VG}, using the formula:

$$S_{VFB} = q^2kTN_T/(WLC^2_{INV}\alpha_t f) \quad (3)$$

where kT is the thermal energy, q is the electron charge and C_{INV} is the inversion capacitance per unit area. Due to errors introduced by the poly-Si depletion region during measurement of the equivalent oxide thickness in poly-Si and FUSI-based devices, the inversion capacitance C_{INV} is mainly considered [29] instead of the oxide capacitance C_{OX}. This would allow a right comparison of trap density values between the three gate electrodes. Table 1b shows for the FUSI devices the volume N_T and surface trap densities D_T, and the S_I and S_{VG} values along with the tunneling depth z. The surface trap densities, calculated from N_T, are estimated using the formula $4kTzN_T$, where z is the tunneling distance of the carrier from the Si/high-κ interface at $f = 25$ Hz. From Table 1b, it can be inferred that the surface trap densities are higher for high-κ-based devices when compared to SiON-based FUSI gate devices.

4. Conclusions

Summarizing the results, it has been shown that in high-κ p-MOSFETs the region near the gate electrode–dielectric interface can effectively be studied using the 1/*f* noise technique. Three types of gate electrode materials – poly-Si, metal and FUSI gates were used for this study. 1/*f* noise spectra are typically observed and the tunneling depths were calculated for high-κ-based p-MOSFETs. From the frequency–depth axis relationship, it was found that the high-κ devices are being probed close to the dielectric–electrode interface. The qualitative trap profile variations studied using $f \times S_I$ spectra showed marked

Table 1b
Noise parameters and estimated trap densities for FUSI gate devices with different Hf-percentages of high-κ dielectric

Hafnium content in the high-κ dielectric	Values at $\vert V_{GS} - V_T\vert = 0.10$–$0.20$ V, $\vert V_{DS}\vert = 0.05$ V, $f = 25$ Hz						
	S_I [A^2/Hz]	S_{VG} [V^2/Hz]	$\sqrt{S_{VG}}$ [V/$\sqrt{Hz}$]	z [nm]	α_t [1/cm]	N_T [1/cm^3 eV]	D_T [1/cm^2]
00% Hf	6.12E−21	9.00E−13	9.48E−07	2.01	0.86E08	2.30E+18	4.81E+10
53% Hf	9.58E−21	1.62E−12	1.27E−06	2.30	0.78E08	2.76E+18	6.60E+10
65% Hf	8.18E−21	1.31E−12	1.14E−06	2.43	0.74E08	1.95E+18	4.92E+10

differences depending on the gate material, confirming the observed behavior of the frequency exponent factor γ. From the trap profiles in poly-Si gate devices, it may be inferred that the concentration of oxygen vacancies could influence the $1/f$ noise, which can explain the differences observed between the gate electrode materials. An influence of the gate electrode on the trap density was observed and discussed. The effect of the Hf-content in the underlying high-κ dielectric layer for FUSI gates was also studied: the almost identical noise magnitude for devices with various Hf-content points out that there seems to be no direct correlation between the Hf-content and the concentration of oxygen vacancies in that case.

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