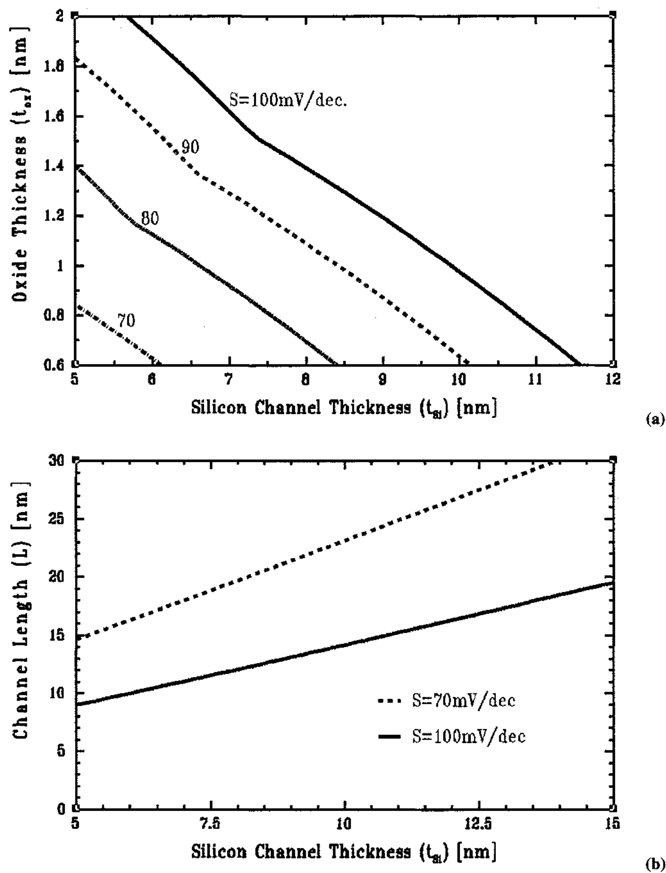

Fig. 5. Scaling capability of DG MOSFETs. (a) Design contours of a 15-nm undoped DG MOSFETs for different $\boldsymbol{S}$ requirements. (b) Projections of minimum channel length as a function of silicon thickness ($\boldsymbol{t}_{ox}$ is assumed to be 0.8 nm).

(t_{ox} is assumed to be 0.8 nm). Clearly, 10 nm undoped DG MOSFETs are likely to find their first applications in places where $S = 100$ mV/dec is tolerable.

III. Conclusions

A general analytical S model for symmetric DG MOSFETs is derived using evanescent-mode analysis. Through a concept of effective conducting path, the model explains a unique N_A dependence of S, providing a unified understanding of previous S models and leading to a new improved S model for undoped DG MOSFETs. Compact, explicit expressions of a scale length are derived that expedite projections of scalability of DG MOSFETs and its requirement.

Acknowledgment

The authors would like to thank E. Harrell and L. Wang for helpful discussions.

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Effect of Reverse Biased Voltage at Source and Drain on Plasma Damage

Durga Misra

***Abstract*—We have examined the possible effects of reverse-biased floating potential at the source and drain during plasma processing on the performance of n-channel metal–oxide–semiconductor field-effect transistors (MOSFETs). Threshold voltage degradation was evaluated by subjecting the gate oxide to high-field injection. Device degradation is found to be enhanced with the floating potential at source and drain for the devices subjected to substrate injection. An increase in electron trapping was observed with an increase in floating potential. Estimation shows that the effective antenna ratio of MOSFET increases with the reverse-biased floating voltage at source and drain. Our results indicate that plasma-charging damage can be significant even under uniform plasma if a potential is developed at the antenna-connected source and drain terminals. Damage in devices subjected to gate injection on the other hand, could have minimal dependence on source and drain potential.**

***Index Terms*—Current stress, effective antenna ratio, plasma damage.**

I. Introduction

Plasma-induced wafer charging is a serious problem in plasma processing. Thin gate oxide in metal–oxide–semiconductor (MOS) transistor is damaged during plasma processing due to high-field electron

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injection. Depending upon the plasma potential distribution on the surface of the wafer high-field injection process could be either substrate injection or gate injection. It has been reported that damages are more pronounced for substrate injection [1]–[3]. In addition, plasma charge damage effects can be enhanced or exacerbated depending upon the relative direction, distance, and size of antennas connected to the gate, source, drain, and substrate [4], [5]. The floating potentials generated due to circuit elements (antenna) at these terminals can induce significant damage even with minimal nonuniformity in the plasma. The interaction of source and drain (S/D) junctions of a transistor with the charging source is, therefore, a high-priority issue to further understand charging damage caused during the metal etching and subsequent dielectric deposition. This paper reports the possible effect of floating potential at the S/D junctions of a transistor during high-field electron injection. To estimate the effect of antenna-connected to S/D terminals during a plasma processing condition, a reverse bias potential was applied at the S/D junctions during stress.

II. Experimental

nMOS transistors were processed using a 0.25 μm complementary metal-oxide semiconductor (CMOS) technology. Transistors had a physical gate length of 0.35 μm. Gate oxide was 60-Å-thick. Transistors were subjected to a forming gas anneal before any measurement. Transistors with a single metal-1 antenna with antenna ratio of 10 000 : 1 were subjected to about 400 mA/cm^2 constant current stress for 3 s using gate injection and substrate injection mode. In a typical injection case, when a transistor is used to evaluate the gate-oxide integrity, source, drain, and substrate are connected together to ground [Fig. 1(a)]. In this work, we have applied voltages of 0 V, 2 V, and 4 V at source and drain terminals [Fig. 1(b)] with substrate grounded where the 0 V case is a typical injection mode [Fig. 1(a)]. Threshold voltage V_t values measured before stress were quite uniform. During constant current stressing the voltage required to sustain the current is recorded as a function of time. After initial decrease (hole trapping) the slowly increasing portion of the V–t curve corresponds to net electron trapping, which is initially dominated by the filling of existing empty electron traps. The slope of the initial portion of the curve represents the net charge-trapping slope per injected electron under the stress condition thus defined as initial electron trapping slope (IETS) [6]. IETS were obtained from the voltage curve. Threshold voltage shifts due to stress were quickly obtained through an automated measurement set up using an HP4156B Semiconductor Parameter Analyzer to minimize the effect of detrapping.

III. Results and Discussion

Fig. 2 shows the variation of threshold voltage shift (ΔV_t) with IETS for both gate injection and substrate injection. For gate injection, the variation of ΔV_t is minimal (tight distribution), whereas it can be observed that for substrate injection as the reverse biased voltage at source and drain increases ΔV_t increases with IETS. It is known that for a given oxide, hole trapping depends on level of current stress, while electron trapping increases with damage. As can be seen from Fig. 2, devices subjected to gate injection have lower IETS and lower ΔV_t, which indicate lower damage (electron traps) and reduced number of trapped holes. We have also observed a higher threshold voltage prior to stress (not shown) than the threshold voltage after stress for gate injection case. This indicates that hole trapping is dominant and charge build-up from electron trapping is negligible [7]. When source and drain junctions are at reverse-biased floating voltages of 0 V, 2 V, and 4 V, the high field zones of gate-to-drain and gate-to-source regions in localized overlap areas dominate the stress. Therefore, a significant portion of stress current is drained through the high field zones at source

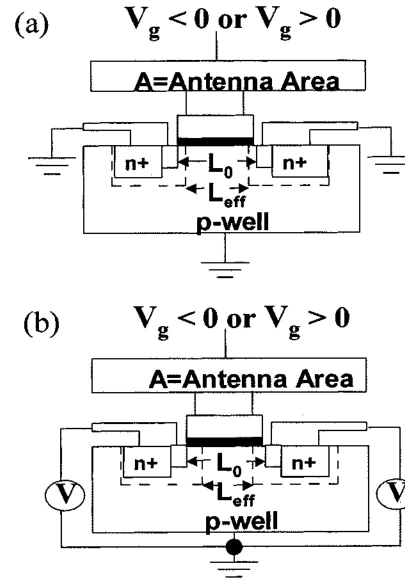

Fig. 1. Cross section of n-MOSFET (a) in a typical stressing condition and (b) with source and drain at reverse-biased floating voltage.

and drain resulting in small current density in the oxide-semiconductor region. This small current density results in almost constant hole trapping and constant threshold voltage shifts.

On the other hand, for substrate injection, the experimentally observed threshold voltage prior to stress is lower than threshold voltage after stress, indicating dominant electron trapping. Moreover, the electron trapping depends upon oxide damages and electron-trapping cross section. As the reverse-biased voltage is increased depletion regions are formed on the source and drain junctions, thereby reducing the effective channel length and increasing the effective current density through the oxide. The scaling of stress current density effectively increases the electron capture probability and therefore, the electron capture cross section is increased with reverse biased voltage, which results in higher threshold voltage degradation. It is interesting to note that ΔV_t for 0 V substrate injection case (Fig. 2) has a large deviation for a fixed IETS value. However, the average value of ΔV_t follows the trend. A significant difference in plasma damage due to stress polarity difference is already reported [1]. The intensity of damage can increase in substrate injection case when the source and drain junctions have significant floating potential depending on plasma potential distribution on the wafer, [8] which makes the junctions reverse biased.

During plasma processing, since the capacitance of the substrate is higher than the device capacitances the substrate potential lags the gate and source/drain potentials. In case of substrate injection, therefore, even if gate/source/drain antennas are located at the same potential, damage can still exist for nMOS [8] if the source/drain junctions are reverse biased and the floating gate potential is above the substrate potential. Aum *et al.* [4] found no damage even if the gate/source/drain antennas are at the same potential because the substrate potential was strongly influenced by source and drain potentials. This is possible when the junctions are forward biased during gate injection for nMOS transistors and during substrate injection for pMOS transistors. Our results suggest that once high field injection process is initiated a reverse biased source/drain junction will make the charge damage worse by enhancing both electron and hole traps in the oxide.

It is known that the oxide charging current produced by plasma processing increase with the "antenna" size of the device structure. Fig. 3 shows the effective antenna ratio as a function of reverse biased voltage at source and drain junctions on nMOS transistors with gate

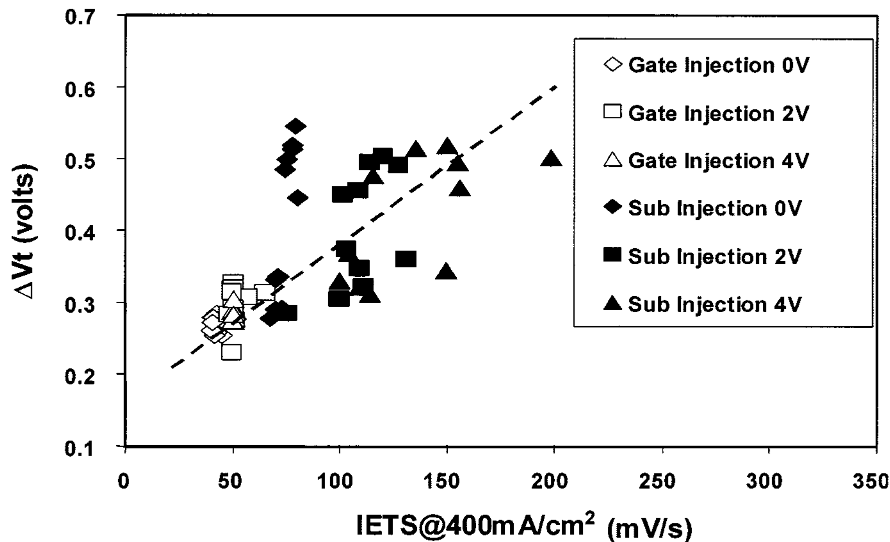

Fig. 2. Threshold voltage shift due to current stress as a function of IETS for both gate-injection and substrate-injection mode at different source/drain floating potentials.

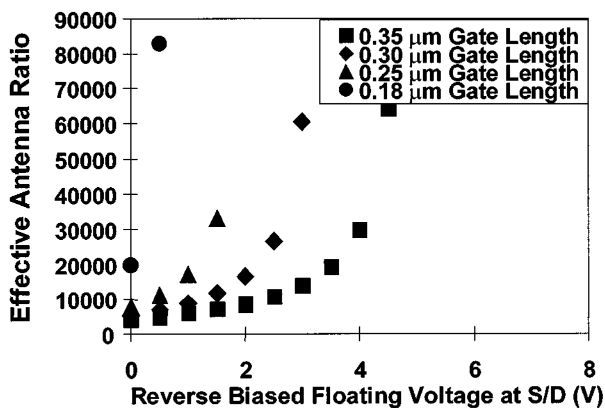

Fig. 3. Effective antenna ratio as a function of reverse-biased floating potentials at source and drain terminals of transistors with two different gate lengths.

lengths of 0.18, 0.25, 0.30, and 0.35 μm with an initial antenna ratio of 20 000 : 1, 8 000 : 1, 5 500 : 1 and 4 000 : 1, respectively. If L_0 is the as drawn length of a transistor (Fig. 1) then with depletion regions formed due to reverse biased voltages at source and drain the effective channel length L_{eff} is given by $L_{eff} = L_0 - (W_S + W_D)$ where W_S and W_D are the drain and source depletion lengths and are given by

$$W_S = W_D = \sqrt{\frac{2\varepsilon_s(V_{bi} + V_{D,S} - 2kT/q)}{qN_B}} = L_D\sqrt{2[q/kT(V_{bi} + V_{D,S}) - 2]}$$

where

$$L_D = \sqrt{\frac{\varepsilon_s kT}{q^2 N_B}}$$

is the Debye length. For a channel doping of 2.5×10^{17} cm^{-3} with a Debye length of 80 Å and a LDD doping of 1.5×10^{18} cm^{-3}, the effective channel length was calculated. It can be noticed that the effective antenna ratio increases with reverse biased source/drain potential. This is in line with the expected behavior in threshold voltage degradation for substrate injection case. Besides, the increase in effective antenna ratio will also prevail for scaled CMOS devices. Even though we have not investigated the device degradation as a function of oxide thickness it is believed that the mechanism of trap build up will be in effect till the oxide reaches the direct-tunneling regime [9]. For thin oxides in direct-tunneling regime electron energy rather than oxide field will dominate as electron transport in quasi-ballistic [9] and defect generation will be independent of oxide thickness.

IV. Conclusion

In conclusion, we studied plasma-processed gate-oxide integrity with reverse-biased voltage at source and drain during gate injection and substrate injection. Observed V_t shift indicates that electron trap concentration is directly proportional to reverse-biased floating voltage for substrate injection and almost constant for gate injection with reverse-biased voltage in the range of 2 V to 4 V. It was estimated that the effective antenna ratio of a transistor is increased when the reverse-biased potential at the source/drain junctions is increased. It is therefore clear that during plasma processing, if a potential is developed at the antenna connected source and drain terminals, then the device will encounter enhanced adverse effect from the antenna connected to the gate.

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InGaN/GaN Tunnel-Injection Blue Light-Emitting Diodes

T. C. Wen, S. J. Chang, L. W. Wu, Y. K. Su, W. C. Lai, C. H. Kuo, C. H. Chen, J. K. Sheu, and J. F. Chen

***Abstract*—A charge asymmetric resonance tunneling (CART) structure was applied to nitride-based blue light emitting diodes (LEDs) to enhance their output efficiency. It was found that with a 20-nm-thick $In_{0.18}Ga_{0.82}N$ electron emitter layer, we could increase the LED output intensity from 28.3 minicandela (mcd) to 43.2 mcd (i.e., a 53% increase). However, a further increase in electron emitter layer thickness will reduce the intensity due to relaxation. It was also found that we could decrease the 20 mA forward voltage from 4.16 V to 3.58 V with a proper electron emitter layer.**

***Index Terms*—Charge asymmetric resonance tunneling (CART), InGaN/GaN, light-emitting diode (LED), MOCVD, multiquantum well (MQW).**

I. Introduction

Recently, tremendous progress has been achieved in GaN-based light-emitting diodes (LEDs). This has resulted in a variety of applications such as traffic light, full color display, optical storage, and lighting [1]. Conventional nitride-based LEDs use multiple quantum wells (MQW) as the active light-emitting region. In such an MQW LED, most of the injected electrons are captured and confined inside the well layers of the MQW active region. These captured and confined electrons can recombine with holes. As a result, photons can be generated and emitted from the LEDs. However, those electrons not captured and/or confined inside the well layers of the MQW active region will be wasted and become leakage current. Thus, one should maximize the number of electrons recombined inside the well layers of the MQW active region so as to increase the light output efficiency. In other words, one needs to maximize the electron capture rate and the carrier confinement effect at the same time. It is known that electron capture rate can be estimated roughly as the quantum well width divided by the product of electron thermal velocity and phonon emission time [2], [3]. Thus, a larger quantum well width can provide us with a larger electron capture rate. However, the carrier confinement effect will decrease as the well width increases. One possible way to solve this problem is to use the charge asymmetric resonance tunneling (CART) structure [4]. The CART structure is to insert a wide electron emitter layer and a thin electron tunneling barrier in between the MQW active region and the n-cladding layer of the LED. Since the width of the electron-emitter layer is large, electrons can be captured efficiently into the electron emitter layer. These captured electrons can subsequently tunnel through the tunneling barrier into the thin well layers of the MQW active region. Thus, one can achieve a large electron capture rate and a large carrier confinement effect simultaneously. In fact, such a CART structure can also be used to enhance the performance of laser diodes [5]–[10]. In this study, we have applied the CART structure to InGaN/GaN blue LEDs. The effects of the electron emitter layer width on the optical and electrical properties of these CART InGaN/GaN blue LEDs will be reported.

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II. Experiment

The InGaN/GaN CART LEDs used in this study were all grown by a metalorgainic chemical vapor deposition (MOCVD) system using a high-speed rotating disk in a vertical growth chamber on (0001) sapphire substrates [11]–[15]. During the growth, trimethylgallium (TMGa), rimethylaluminum (TMAl) trimethylindium (TMIn), and ammonia (NH_3) were used as gallium, aluminum, indium, and nitrogen sources, respectively. Biscyclopentadienyl magnesium (CP_2Mg) and disilane (Si_2H_6) were used as the p-type and n-type doping sources, respectively. The structure of the CART LEDs consists of a 30 -nm-thick GaN nucleation layer grown at a low temperature of 560 °C, a 4-μm-thick Si-doped GaN buffer layer ($n = 2 \times 10^{18}$ cm^{-3}), an Si-doped $In_{0.18}Ga_{0.82}N$ electron emitter layer ($n = 2 \times 10^{17}$ cm^{-3}) with different thickness, a 3-nm-thick Si-doped GaN electron tunneling barrier ($n = 2 \times 10^{17}$ cm^{-3}), an unintentionally doped InGaN/GaN MQW active region, a 30-nm-thick Mg-doped $Al_{0.15}Ga_{0.85}N$ cladding layer ($p = 5 \times 10^{17}$ cm^{-3}), and a 0.25- μm-thick Mg-doped GaN contact layer ($p = 5 \times 10^{17}$ cm^{-3}). The unintentionally doped InGaN/GaN MQW active region consists of three periods of 2.5 nm-thick $In_{0.3}Ga_{0.7}N$ well layers and 7-nm-thick GaN barrier layers. Our Mg-doped contact layer shows an *in-situ* p-type conductivity after growth. Thus, no postgrowth thermal annealing is needed to activate magnesium. In order to increase the indium incorporation rate, nitrogen was used as the carrier gas when we grew the InGaN/GaN MQW active regions. Hydrogen was used as the carrier gas when we grew the other parts of the samples. The growth pressure was kept at 100 mTorr throughout the growth. In this study, three CART LEDs with different electron emitter layer thickness (i.e., 10, 20, and 40 nm) were prepared. A normal MQW LED without the CART structure (i.e., the electron emitter layer and electron tunneling barrier) was also prepared for comparison. Other parts of the sample structure were all the same. We also used the same growth conditions for all these LEDs. The schematic diagram and band diagram of the InGaN/GaN CART LEDs are shown in Fig. 1(a) and 1(b), respectively. The purpose of the CART structure is to increase the LED light output intensity. With the CART structure, injected electrons are effectively captured by the electron emitter layer since its width is much larger than that of the well layers in the

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