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Charge trapping and interface characteristics of thermally evaporated HfO_2

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Charge trapping and interface characteristics of hafnium oxide (HfO_2) films, grown by standard thermal evaporation, were investigated. High frequency capacitance–voltage and conductance measurements were carried out at various temperatures on aluminum gate metal–oxide–semiconductor capacitors, annealed at 450 °C. A hysteresis below 30 mV was observed. Electrical data show, that charge trapping in HfO_2 initially increases with decrease in temperature while it shows a turnaround phenomenon when the temperature is decreased further. Interface state density distribution observed at low temperatures suggests that charge-trapping behavior of these films is mostly due to shallow traps at the interface. © *2004 American Institute of Physics*. [DOI: 10.1063/1.1805708]

To reduce gate leakage, hafnium oxide (HfO_2) has been under intense investigation recently for replacing conventional SiO_2 as the gate dielectric in complementary metal–oxide–semiconductor (CMOS) devices. Even though significant efforts have been dedicated to the investigation of Hf-based gate dielectric material systems, key issues like charge trapping, specifically bulk and interface charge trapping, pose a serious threat to the long-term operation of HfO_2 based devices.[1,2] To address these issues not only high quality films need to be deposited but also excellent electrical characteristics need to be obtained before HfO_2 can be integrated into standard CMOS process flow.[3–6] Charge trapping properties of high-quality HfO_2 thin films deposited by various methods such as atomic layer deposition,[7] evaporation with ion-assisted deposition,[8] sputtering,[9] and *in situ* rapid thermal chemical vapor deposition[10] have been evaluated. The properties of grown film and interface show a pronounced dependence upon the deposition process and the precise deposition parameters chosen. Sputtering and e-beam assisted depositions create radiation induced surface damage during film growth. All these techniques, therefore, require high temperature annealing which further results in the deterioration of device performance and reliability. Charge trapping characteristics of HfO_2 films, deposited by standard thermal evaporation, have been studied using MOS capacitors.

HfO_2 films of two different thicknesses were deposited on *n*-type (resistivity of 10–20 Ω cm) ⟨100⟩ Si wafers by standard thermal evaporation. Oxygen was added at constant partial pressure during evaporation. After the deposition of HfO_2 film, a layer of 400 nm aluminum was deposited and patterned. Samples were annealed at 350 and 450 °C for 20 min in forming gas (FGA: N_2/H_2 5%). HfO_2 film thicknesses of 50 and 60 nm were measured by ellipsometer after the deposition. Dielectric constant estimated from electrical measurements is found to be in the range of 18–25. Further details of HfO_2 film deposition and dielectric constant measurements are presented elsewhere.[11] High-frequency capacitance–voltage ($C-V$) measurements, parallel conductance and capacitance measurements in the 20 Hz–1 MHz range, and current–voltage measurements were performed by Boonton 7200 capacitance meter, HP4284A LCR meter, and HP4156B semiconductor parameter analyzer, respectively. Interface state density was measured using conductance method.[12]

Figure 1 depicts the $C-V$ characteristics of the as-deposited and annealed (350 and 450 °C) 50 and 60 nm Al/HfO_2/n-Si gate stacks. The hysteresis in the films is mostly due to slow interface states as modern fabrication facilities significantly reduce mobile ionic charges in the deposited films. In the case of 50 nm film after 450 °C annealing hysteresis reduced to 30 mV as partial annealing of defects occurred at both gate and substrate interfaces. Moreover, oxide charge density, measured from flatband voltage shift (ΔV_{FB}) with respect to ideal $C-V$, reduced to $1.61\times10^{11}/cm^2$ after 450 °C annealing. In the case of 60 nm film, hysteresis was reduced approximately to 175 mV but

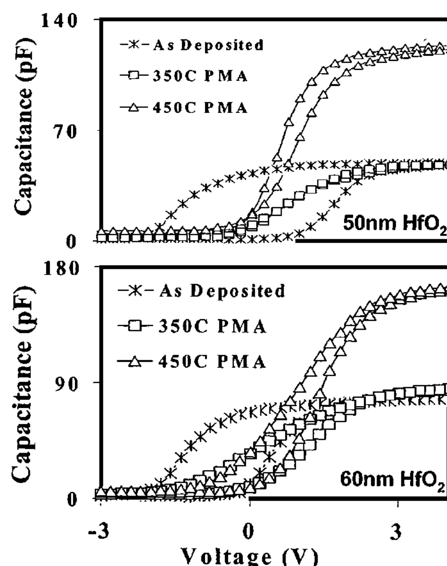

FIG. 1. $C-V$ curves of MOS capacitors with 50 and 60 nm HfO_2 films. Hysteresis was reduced to 30 and 175 mV, respectively, after 450 °C annealing. Oxide charges were reduced to $1.61\times10^{11}/cm^2$ and increased to $1.15\times10^{12}/cm^2$ for 50 and 60 nm HfO_2 films when samples were annealed at 450 °C.

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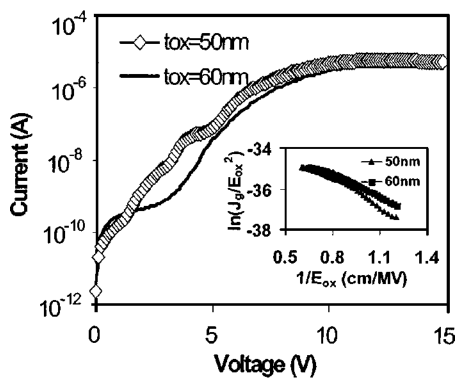

FIG. 2. Leakage current in 50 and 60 nm HfO_2 film MOS capacitor (1.96×10^{-3} cm^2 area) after 450 °C annealing. The insert shows the $\ln(J_g/E_{ox}^2)$ vs $1/E_{ox}$ plot that suggests that the combination of FN and interface state assisted tunneling is responsible for leakage current.

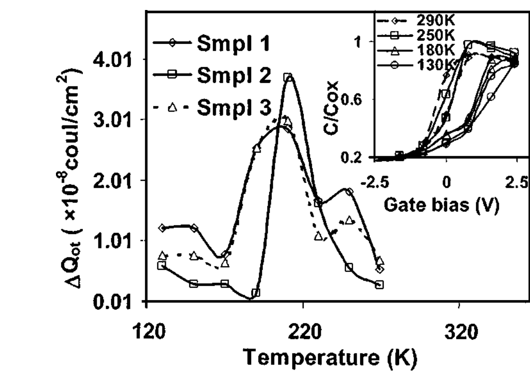

FIG. 3. The variation in effective oxide trapped charge as a function of temperature for 50 nm HfO_2 MOS capacitor. The insert shows low temperature high-frequency $C-V$ curves for 50 nm HfO_2 MOS capacitor.

still remained higher than that of 50 nm HfO_2 film as it has more slow states.[13] In addition, an increase in oxide charges to $1.15\times10^{12}/cm^2$ after 450 °C annealing was noticed. This increase in oxide charges in 60 nm HfO_2 could be due to higher built-in stress in the bulk oxide during deposition, irreparable stoichiometric defects or extensive interface defects. After annealing built-in stress generates both bulk and interface defects. The stretchout effects in the $C-V$ curve for 60 nm HfO_2 along the bias axis near inversion capacitance after 450 °C annealing further suggests that interface states, possibly slow states, were created after annealing.

It was noted that postmetal anneal (PMA) can introduce an interfacial layer (IL)[14–16] and an increase of IL leads to decreased effective dielectric constant of the gate stack. The total capacitance of the gate stack, therefore, decreases due to the series combination of capacitance of IL and bulk HfO_2. It was also reported that annealing in H_2 (FGA) at low temperatures reduces the formation of IL and partially passivates the interfacial defects.[15] On the other hand, increase in density of deposited HfO_2 may be possible after PMA due to condensation.[14] In our experiment, it was observed (Fig. 1) that oxide capacitance remained almost the same after 350 °C anneal for both 50 and 60 nm stacks but increased considerably after 450 °C annealing. We, therefore, believe that significant increase in IL might not have occurred. On the other hand, the combined effect of higher density of the film due to condensation that increased the dielectric constant and a decrease in oxide thickness is the reason for the capacitance increase after 450 °C annealing.

As can be seen from Fig. 2 both the samples showed high leakage current after 450 °C annealing. At flatband, the leakage current density for 50 nm HfO_2 films is $<10^{-7} A/cm^2$ whereas for 60 nm film it is even higher. For large leakage current, charge injection can contribute to hysteresis observed in $C-V$ characteristics (Fig. 1). To further understand the leakage characteristics the calculated Fowler–Nordheim (FN) tunneling plots of $\ln(J_g/E_{ox}^2)$ versus $1/E_{ox}$ of the gate stack at room temperature is depicted in the insert of Fig. 2. It is obvious from Fig. 2 (insert) that FN tunneling is the dominant leakage mechanism.[17–19] Here, the oxide electric field, E_{ox}, was estimated from potential difference across oxide, V_{ox}.[17] The effective barrier height (Φ_B) can then be estimated by using the negative of the slope of the FN plots, B (Fig. 2, inset), which can be calculated from the following equation:[17]

$$B = 6.83 \times 10^{7*}(m_{OX}^{*}\Phi_B^3)^{1/2}\ (\mathrm{V/cm}). \quad (1)$$

Considering the effective mass of electron (m_{OX}) in HfO_2[18,19] in Eq. (1), Φ_B=0.3 eV for 60 nm film with 450° anneal where as Φ_B=0.43 eV when $1/E_{ox}>9\times10^{-7}$(cm/V) and Φ_B=0.28 eV when $1/E_{ox}<9\times10^{-7}$(cm/V) for 50 nm film with 450 °C anneal. During FN tunneling under positive gate bias, electrons tunnel from conduction band to metal at comparatively low E_{ox} in metal/high-k/semiconductor MOS devices due to lower potential barrier of the high-k materials.[20] A second current component due to interface trap assisted tunneling contributes to the leakage current at high E_{ox}. Φ_B decreases further once the interface states start contributing to leakage current.[21] In the case of 50 nm HfO_2 film, tunneling from conduction band is dominant at comparatively low E_{ox}, but at higher E_{ox} interface states assisted tunneling becomes significant and decreases Φ_B. In 60 nm films interface states contribute to the leakage current for the entire range of E_{ox} and Φ_B is almost the same as that of 50 nm films at higher E_{ox}. This further confirms the degraded quality of the 60 nm films even after 450 °C annealing. However, there is significant presence of interface states in 50 nm film that become activated at relatively high E_{ox} and increases the leakage current.

Due to considerable stretch-out near inversion capacitance compared to V_{FB} shift in $C-V$ curves in the 130–290 K range (insert of Fig. 3), interface states are more dominant than bulk traps. ΔQ_{ot}, estimated from ΔV_{FB}, increase in 200–290 K but decrease in 130–200 K ranges. Since the density, location, and polarity of individual trapped charge affect the location of the centroid,[22] it is possible that oxide border traps and shallow traps at Si/HfO_2 interface cause turn-around in ΔQ_{ot} as 450 °C PMA eliminates traps at Al/HfO_2 interface. $G_p/\omega-\log(f)$ curves in 130–290 K (Fig. 4) show peaks at lower frequencies and become wider with decreasing temperature because of increase in response time[12] (insert in Fig. 4) and in number of shallow interface traps. Turn-around in D_{it} (Fig. 5), estimated from $G_p/\omega-\log(f)$, confirms that shallow interface charges dominate in 130–290 K in our films and cause turn-around in ΔQ_{ot}. D_{it} versus (E_T-E_i) (insert of Fig. 5) further suggest that shallow interface traps dominate charge trapping characteristics. Moreover, D_{it} is within a typical range of HfO_2 films unless special interface (e.g., ozone) treatments are performed before deposition. High D_{it} values compared to Si/SiO_2($\sim10^{10}$ cm^{-2} eV^{-1}) or Si/HfSiO interfaces[23,24]

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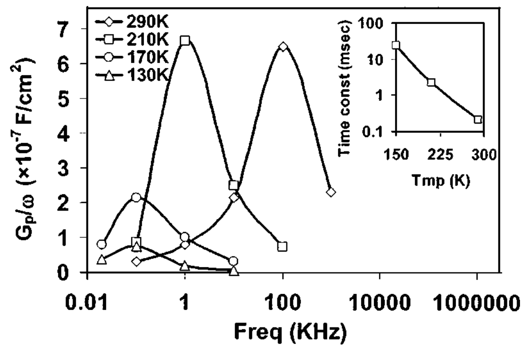

FIG. 4. Conductance measurement shows the G_p/ω curves at different temperatures, with respect to frequency. The insert shows the interface trap time constant with respect to temperature.

($\sim 10^{11}$ cm^{-2} eV^{-1}), and low Φ_B show absence of IL in our devices.

As reported elsewhere,[25] during substrate injection, gate voltage threshold of electron trap generation was found to be 2–2.5 V due to low Φ_B at HfO_2/Si interface. Kang *et al.*[24] found threshold to be –1.5 to –2.5 V during gate injection in Pt/HfO_2/HfSiO/*p*-Si devices due to the absence of IL and subsequent low Φ_B at Pt/HfO_2 interface, which supports absence of IL in our films.

In summary, charge-trapping characteristics of MOS capacitors with thermally evaporated HfO_2 films have been reported. The initial measurements suggest that interface states dominate the charge trapping characteristics observed in $C-V$ measurements and the leakage current through the dielectric is the combination of FN and interface states assisted tunneling. The interface states characteristics at low temperatures suggest a strong contribution from shallow traps and a turn-around effect is noticed when temperature is lowered because of charge trapping in those traps.

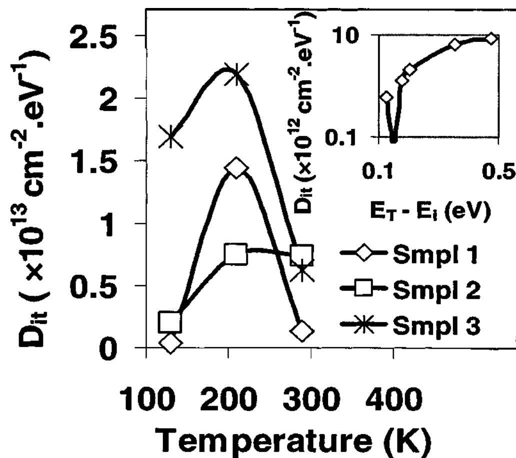

FIG. 5. Peak D_{it} values estimated from those G_p/ω versus frequency curves as a function of temperatures. The insert is the distribution of D_{it} as a function of trap energy level plotted with respect to intrinsic Fermi level (E_T-E_i) at 290 K (insert).

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