

Table 1: Correlator design parameters.

Parameter	Units	Description
B	Hz	bandwidth of IF sub-band
$f_D = 2B$	Hz	digitizer clock frequency (Nyquist rate sampling)
f_C	Hz	correlator clock frequency
N_B	-	basic number of correlator chips required
N_{CC}	-	number of cascaded chips
N_T	-	total number of correlator chips used
N_C	-	number of lags per correlator chip
N_R	-	number of lags required
N_I	-	number of independent lags obtained
$\Delta_f = 2B/N_I$	Hz	spectral sample spacing
$D = \text{round_up}(f_D/f_C)$	-	digitizer to correlator chip clock ratio
$\gamma = N_I/N_R$	-	overkill ratio

3.3 Cross correlator design equations

This section details the steps required to evaluate whether time demultiplexing or the deep memory model will meet the spectral resolution requirements of a cross correlator design (auto-correlator designs use similar equations, but since they do not need to calculate negative lags, their spectral resolving capability, for the same number of lags, is twice as good as a cross correlator). Some of the relevant system parameters are shown in Table 1.

The basic requirement of any cross correlator is usually specified in terms of the spectral resolution it can obtain across the IF bandwidth, i.e., the basic requirement is to produce a cross power spectrum with a spectral sample spacing Δ_f (depending on the windowing function used in the lag domain, the spectral resolution is typically on the order of twice Δ_f). If we consider that the IF bandwidth is filtered into sub-bands of bandwidth B , then each cross correlator must produce a spectral sample spacing of Δ_f across bandwidth B . This spectral sample spacing is achieved using a digitizer with a clock frequency $f_D = 1/(2B)$ and a cross correlator chip with a clock frequency f_C and N_C lags.

If the digitizer clock frequency and the cross correlator clock frequency are the same, then the design is trivial—data from the digitizer is sent directly to one or more cross correlator chips. In this case, the spectral sample spacing in the Fourier transform of the cross correlation function is

$$\Delta_f = \frac{2B}{N_I}. \quad (18)$$

where $N_I = N_{CC}N_C$ and N_{CC} is the number of cascaded correlator chips used to achieve the desired spectral resolution.

In cases where the digitizer clock frequency exceeds the cross correlator chip clock frequency by a factor of two or more, a digital parallel processing scheme is employed. The design of a cross correlator then follows the following steps:

1. Determine the number of lags required to obtain the desired spectral sample spacing; that is,

$$N_R = \frac{2B}{\Delta_f} \quad (19)$$

2. Calculate D , the ratio of the digitizer clock frequency to the correlator clock frequency.
3. (a) For a time demultiplexed design, the basic number of correlator chips required is $N_B = D^2$, and the number of independent lags is $N_I = DN_C$.
(b) For a deep memory model based design, the basic number of correlator chips required is $N_B = D$, and the number of independent lags available from this design is $N_I = N_C$ (each of the D chips calculate the same lags from different temporal samples).
4. Calculate the ratio of the number of independent lags to the number of lags required, i.e.,

$$\gamma = \frac{N_I}{N_R}. \quad (20)$$

For reasons that will become clear, this ratio is referred to as the *overkill* ratio. If $\gamma \approx 1$, then the design produces the required spectral sample spacing, if $\gamma < 1$ then the next integer above $(1/\gamma)$ gives the number of cascaded chips required to produce the desired spectral sample spacing, i.e., $N_{CC} = \text{round_up}(1/\gamma)$, and if $\gamma > 1$, then the design exceeds the desired spectral sample spacing. If γ is greater than 1, by a small margin, then the design meets the specified spectral sample spacing. However, if γ is significantly larger than 1, then the design has overkilled on the spectral sample spacing and redesign may be necessary.

5. If γ was less than or equal to 1, then the total number of correlator chips required in each design is

$$N_T = \begin{cases} D^2 N_{CC} & \text{time demultiplexing} \\ DN_{CC} & \text{deep memory} \end{cases} \quad (21)$$

and the number of independent lags available in each design is

$$N_I = \begin{cases} DN_C N_{CC} & \text{time demultiplexing} \\ N_C N_{CC} & \text{deep memory} \end{cases} \quad (22)$$

and the final spectral sample spacing is then,

$$\Delta_f = \frac{2B}{N_I}. \quad (23)$$

To achieve equivalent spectral sample spacings between a time demultiplexed correlator and a deep memory correlator, the number of independent lags in each design must be equivalent. Equation (22) indicates that chips used in a deep memory model need to have D times the number of lags as those used in a time demultiplexed model (or that you need to cascade D chips in the deep memory model).