

# Jie Hu

Assistant Professor  
Electrical and Computer Engineering  
New Jersey Institute of Technology  
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## RESEARCH INTERESTS

Computer Architecture, Power-Aware Systems Design, High-Performance Low Power Microprocessor Design, Reliable Power-Efficient Systems Design, Reconfigurable Computing Architecture, Networks-on-Chip.

## EDUCATION

- 2004 Ph.D., Computer Science and Engineering, The Pennsylvania State University – UP  
Dissertation: Orchestrating the Compiler and Microarchitecture for Reducing Cache Energy  
2000 M.E., Signal and Information Processing, Peking University, China  
1997 B.E., Computer Science and Engineering, Beijing University of Aeronautics and Astronautics, China

## EMPLOYMENT

08/2004 - Present	Assistant Professor	Electrical and Computer Engineering, New Jersey Institute of Technology
08/2000 - 07/2004	Grad. Research/Teaching Asst.	Computer Science and Engineering, The Pennsylvania State University
01/1997 - 07/2000	Grad. Research/Teaching Asst.	Center for Information Science, Peking University, China
09/1996 - 12/1996	Research Assistant	Computer Science and Engineering, Beijing University of Aeronautics and Astronautics, China

## TEACHING

Spring 2009	ECE252: Microprocessors	Dept. ECE, New Jersey Institute of Technology
Spring 2009	ECE252: Microprocessors	Dept. ECE, New Jersey Institute of Technology
Fall 2008	ECE252: Microprocessors	Dept. ECE, New Jersey Institute of Technology
Fall 2008	ECE692: Embedded Computing Systems	Dept. ECE, New Jersey Institute of Technology
Spring 2008	ECE252: Microprocessors	Dept. ECE, New Jersey Institute of Technology
Spring 2008	ECE251: Logic Design	Dept. ECE, New Jersey Institute of Technology
Fall 2007	ECE252: Microprocessors	Dept. ECE, New Jersey Institute of Technology
Fall 2007	ECE692: Embedded Computing Systems	Dept. ECE, New Jersey Institute of Technology
Spring 2007	ECE395: Microprocessors Lab (Re-design)	Dept. ECE, New Jersey Institute of Technology
Spring 2007	ECE252: Microprocessors	Dept. ECE, New Jersey Institute of Technology
Fall 2006	ECE252: Microprocessors	Dept. ECE, New Jersey Institute of Technology
Fall 2006	ECE692: Embedded Computing Systems	Dept. ECE, New Jersey Institute of Technology
Spring 2006	ECE789: Advanced Topics in Computer Arch.	Dept. ECE, New Jersey Institute of Technology
Fall 2005	ECE692: Embedded Computing Systems	Dept. ECE, New Jersey Institute of Technology
Spring 2005	ECE690: Computer Systems Architecture	Dept. ECE, New Jersey Institute of Technology
Fall 2004	ECE692: Embedded Computing Systems	Dept. ECE, New Jersey Institute of Technology
Fall 2003	CSE271: Introduction to Digital Systems (As A Teaching Assistant)	Dept. CSE, The Pennsylvania State University
Spring 2001	CSE271: Introduction to Digital Systems	Dept. CSE, The Pennsylvania State University
Fall 2000	CSE514: Computer Networks	Dept. CSE, The Pennsylvania State University
Fall 1999	CS: Introduction to Database Systems	Dept. of CS, Peking University, Beijing, China
Spring 1997	CS: Data Structures and Algorithms	Dept. of CS, Peking University, Beijing, China

## SELECTED RESEARCH PROJECTS

- 08/2004 - Present      Electrical and Computer Engineering, New Jersey Institute of Technology
- Transactional Processors for Reliable Computing

- Networks with Extended Quality of Service using Service Vectors
- Complexity-Effective Microprocessors Design in Future Technologies
- Self-Adaptive Reliable Memory Systems
- Novel Architectures for Soft-Error Fault Tolerance
- Thermal-aware microarchitectures

01/2001 - 07/2004 Research Assistant Microsystems Design Lab, CSE, The Pennsylvania State University

- Modeling the Soft Error Impact on Processor Datapath
- Scalable Wakeup-Free Instruction Scheduler
- Scheduling Reusable Instructions for Power Efficiency
- Application-Aware Instruction Cache Leakage Management
- Compiler-Directed Instruction Cache Leakage Optimization
- Dynamic Energy Reduction via Cache Reconfiguration
- Optimizing Power Efficiency in Trace Cache Fetch Unit

01/1997 - 07/2000 Research Assistant Database Research Group, CS, Peking University, China

- ECOBASE – Mobile & Embedded Database Management System
- COBASE VII (Multimedia Version)
- COBASE for RedFlag LINUX

09/1996 - 12/1996 Research Assistant Network Information Center, CSE, Beijing Univ. of Aero. and Astro., China

- BUAA Campus Network Project

#### PROFESSIONAL ACTIVITIES

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- NSF Panel: NSF/CISE/CCF/CPA 2008.
- Proposal Review for Villanova University.
- Proposal Review for HongKong Research Council.
- PC Member, Registration & Local Arrangement Chair, the 21st Intl Conf. on Tools with AI (ICTAI09), Nov. 2009.
- PC Member, the 1st International Conference on Contemporary Computing, NOIDA, India August 17-19, 2008.
- PC Member, the 22nd Annual ACM Symposium on Applied Computing (SAC 2007), Seoul, Korea, March 11 - 15, 2007.
- Web Master, the 16th Wireless & Optical Communications Conference (WOCC 2007), NJIT, Newark, NJ, April 27 - 28, 2007.
- Session Chair for Future VLSI Technologies and Their Impact, IEEE International Conference of Computer Design (ICCD-2005), October 2-5, 2005.
- Reviewer for Journals: ACM TODAES, IEEE TVLSI, ACM TECS, IEEE TCAD, IEEE SMC, IEEE Trans. on CSVT, ASP JOLPE, Journal of Systems and Software, IEE Proc. Computers & Digital Techniques, Journal of Modeling and Simulation, International Journal of Computers and Applications, Journal of Circuits, Systems, and Computers (JCSC), Research Letters in Electronics, Computer Languages, Systems and Structures Journal, for Conferences: VLSI Design 2008, SAC 2007, CASES06, MASCOTS06, HPCA-12, ISPASS'05, HPCA-11, DATE'04, HPCA-10, ICS-2004, ICCD'03, HiPC 2003, ISLPED'03, PACT'03, LCTES'03, ISCA'03, DATE'03, ISVLSI'03, GLVLSI'03, COLP'02, CASES'02.

## UNIVERSITY SERVICE ACTIVITIES

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- NJIT: Poster judge, 2nd Graduate Student Research Day (GSRD), Nov. 6, 2006.
- NJIT: Student Advisor, McNair Post-Baccalaureate Achievement Program, 2006
- ECE Department: Member of Committee on UG Laboratory Facilities (2006-2008)
- ECE Department: Member of Committee on Seminars (2006-2008)

## HONORS AND AWARDS

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- 2nd Place Award in ECE Senior Design Project Workshop, Project Title: ASIC Encoder with an Integrated Look-up Table (Student team: Gian Francisco, Swati Jani, Akinola Akiwowo; Advisor: Jie Hu), May 1st, 2007.
- Certificate of Outstanding contribution to the Ronald E. McNair Post-Baccalaureate Achievement Program at New Jersey Institute of Technology, April 7, 2006.
- CRA Academic Careers Workshop Graduate Funding, Feb. 22-23, 2004.
- ACM SIGPLAN PAC (Professional Activities Committee) Professional Activities Grant for LCTES'02 / SCOPES'02, June 19-21, 2002.
- 1997, Privilege to enter the graduate school of Peking Univ, waived of the admission test.
- 1996, Excellent Student Scholarship, BUAA.
- 1995, the People's Scholarship, BUAA.
- 1994, the People's Scholarship, BUAA.

## SPONSORED RESEARCH PROJECTS

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- Networks with Extended Quality of Service using Service Vectors. Sponsor: NSF. Roberto Rojas-Cessa (PI), Jie Hu (Co-PI), Nirwan Ansari (Co-PI), Symeon Papavassiliou (Co-PI), and Sotirios Ziavras (Co-PI), Continuous Grant awarded for FY 2007-2008, Total Grant duration: 48 months, September 2004 - August 2008, Total sponsor support: \$450,000 + NJIT Cost sharing: \$171,524.
- Transactional Processors: Exploiting Hardware Transaction Processing for Reliable Computing. Sponsor: NSF, Amount: \$74,999. Role: PI, Proposed Start Date: Jul. 1, 2009, End Date: Jun. 30, 2010. Renewable after first year. (Recommended by NSF Program Director, currently in budget revise stage)
- Equipment Grant for Establishing ARM-based Embedded System Design Lab. Sponsor: ARM Ltd., Amount: \$109,925. Role: PI, September 1st, 2008.

## PUBLICATIONS

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### Book Chapters

- J. S. Hu, G. Chen, M. Kandemir and N. Vijaykrishnan. Software Power Optimzation. Book Chapter in *System on Chip: Next Generation Electronics*, pp. 289 - 316, edited by Bashir M. Al-Hashimi, IEE Press, ISBN: 0-86341-552-0 & 978-086341-552-4, 2006.

### Journals/Magazines

- Shuai Wang, Jie Hu, and Sotirios G. Ziavras. On the Characterization and Optimization of On-Chip Cache Reliability against Soft Errors. Accepted for publication in *IEEE Transactions on Computers (TC)*, 2009.
- Jie Hu, Shuai Wang, and Sotirios G. Ziavras. On the Exploitation of Narrow-Width Values for Improving Register File Reliability. Accepted for publication in *IEEE Transactions on Very Large Scale Integration (VLSI) Systems (TVLSI)*, 2008.
- Shuai Wang, Jie Hu, and Sotirios G. Ziavras. Self-Adaptive Data Caches for Soft-Error Reliability. In *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Volume 27, No. 8, pp. 1503 - 1507, 2008.
- S. Wang, H. Yang, J. Hu, and S. G. Ziavras. Asymmetrically Banked Value-Aware Register Files for Low Energy and High Performance. In *Microprocessors and Microsystems*, Volume 32, Issue 3, pp. 171 - 182, May 2008.
- Hongyan Yang, Sotirios G. Ziavras, and Jie Hu. Reconfiguration Support for Vector Operations. In *International Journal of High Performance Systems Architecture (IJHPSA)*, Volume 1, No. 2, pp. 89 - 97, 2007.

- J. Hu, N. Vijaykrishnan, M. J. Irwin, and M. Kandemir. Optimizing Power Efficiency in Trace Cache Fetch Unit. In *IET Computers & Digital Techniques*, Volume 1, Issue 4, pp. 334 - 348, July 2007.
- J. Hu, F. Li, V. Degalahal, M. Kandemir, N. Vijaykrishnan, M. J. Irwin. Compiler-Assisted Soft Error Detection under Performance and Energy Constraints in Embedded Systems. Accepted for publication in *ACM Transactions on Embedded Computing Systems (TECS)*, 2006.
- J. Hu, M. Kandemir, N. Vijaykrishnan, M. J. Irwin. Analyzing Data Reuse for Cache Reconfiguration. In *ACM Transactions on Embedded Computing Systems (TECS)*, Volume 4, No. 4, pp. 851 - 876, November 2005.
- W. Zhang, J. S. Hu, V. Degalahal, M. Kandemir, N. Vijaykrishnan, M. J. Irwin. Reducing Instruction Cache Energy Consumption Using a Compiler-Based Strategy. In *ACM Transactions on Architecture and Code Optimization (TACO)*, Volume 1, No. 1, pp. 3 -33, March 2004.
- N. Kim, T. Austin, D. Blaauw, T. Mudge, K. Flautner, J. S. Hu, M. J. Irwin, M. Kandemir, and N. Vijaykrishnan. Leakage Current: Moore's Law Meets Static Power. In *IEEE Computer Special Issue on Power- and Temperature-Aware Computing*, pp. 68 - 75, December, 2003.

#### Refereed Conferences

- S. Wang, J. Hu, S. G. Ziavras, and S. W. Chung. Exploiting Narrow-Width Values for Thermal-Aware Register File Designs. Accepted for publication in *Proc. of the Conference on Design, Automation and Test in Europe (DATE'09)*, Nice, France, April 20-24, 2009.
- Shuai Wang, Jie Hu, and Sotirios G. Ziavras. BTB Access Filtering: A Low Energy and High Performance Design. In *Proc. of the IEEE Computer Society Annual Symposium on VLSI (ISVLSI 2008)*, pp. 81 - 86, Montpellier, France, April 7-9, 2008. (accepted 74 out of 245 submissions, acceptance rate: 30%) (**Nominated for Best Paper Award**)
- Xiaofang Wang, Sotirios G. Ziavras, and Jie Hu. Energy-Aware System Synthesis for Reconfigurable Chip Multiprocessors. In *Proc. of the 2007 International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA'07)*, pp. 61 - 70, Las Vegas, Nevada, June 25-28, 2007.
- S. Wang, H. Yang, J. Hu, and S. Ziavras. Asymmetrically Banked Value-Aware Register Files. In *Proc. of the IEEE Computer Society Annual Symposium on VLSI (ISVLSI 2007)*, pp. 363 - 368, Porto Alegre, Brazil, May 9-11, 2007. (accepted 66 out of 174 submissions, acceptance rate: 38%)
- H. Yang, S. Wang, S. Ziavras, and J. Hu. Vector Processing Support for FPGA-Oriented High Performance Applications. In *Proc. of the IEEE Computer Society Annual Symposium on VLSI (ISVLSI 2007)*, pp. 447 - 448, Porto Alegre, Brazil, May 9-11, 2007. (Poster, accepted 27 out of 174 submissions)
- Hongyan Yang, Sotirios Ziavras and Jie Hu. FPGA-based Vector Processing for Matrix Operations. In *Proc. of the Fourth International Conference on Information Technology: New Generations (ITNG 2007)*, Las Vegas, Nevada, April 2-4, 2007.
- X. Wang, S. G. Ziavras, and J. Hu. System-Level Energy Modeling for Heterogeneous Reconfigurable Chip Multiprocessors, To appear in *Proc. of IEEE International Conference on Computer Design (ICCD2006)*, San Jose, CA, Oct. 1-4, 2006. (accepted 72 out of 231 submissions, acceptance rate: 31%)
- Shuai Wang, Jie Hu, and Sotirios G. Ziavras. On the Characterization of Data Cache Vulnerability in High-Performance Embedded Microprocessors. In *Proc. of the 6th International Conference on Embedded Computer Systems: Architectures, Modeling, and Simulation (SAMOS VI)*, Samos, Greece, July 17-20, 2006. (accepted 26 (for IC-SAMOS) out of 130 submissions, acceptance rate: 20%)
- Jie Hu, Shuai Wang and Sotirios G. Ziavras. In-Register Duplication: Exploiting Narrow-Width Value for Improving Register File Reliability. In *Proc. of the International Conference on Dependable Systems and Networks (DSN-2006)*, pp. 281 - 290, Philadelphia, PA, June 25-28, 2006. (accepted 34 out of 187 submissions, acceptance rate: 18%)
- Jie S. Hu, G. M. Link, Johnsy K. John, Shuai Wang, and Sotirios G. Ziavras. Resource-Driven Optimizations for Transient-Fault Detecting SuperScalar Microarchitectures. In *Proc. of the 10th Asia-Pacific Computer Systems Architecture Conference (ACSAC05)*, pp. 200 - 214, Singapore, October 24-26, 2005.
- Johnsy K. John, Jie S. Hu, and Sotirios G. Ziavras. Optimizing the Thermal Behavior of Subarrayed Data Caches. In *Proc. of IEEE International Conference of Computer Design (ICCD-2005)*, pp. 625 - 630, San Jose, California, October 2-5, 2005.

- J. S. Hu, F. Li, V. Degalahal, M. Kandemir, N. Vijaykrishnan, and M. J. Irwin. Compiler-directed instruction duplication for soft error detection. In *Proc. of the Design, Automation and Test in Europe (DATE'05)*, 1056 - 1057, Munich, Germany, March 7-11, 2005.
- J. S. Hu, N. Vijaykrishnan, S. Kim, M. Kandemir, M. J. Irwin. Scheduling Reusable Instructions for Power Reduction. In *Proc. of the Conference on Design, Automation and Test in Europe Conference (DATE'04)*, pp. 10148 - 10155, Paris, France, February 16-20, 2004. (accepted 181 out of 780 submissions, acceptance rate: 23%)
- Jie S. Hu, N. Vijaykrishnan, and Mary Jane Irwin. Exploring Wakeup-Free Instruction Scheduling. In *Proc. of the International Symposium on High Performance Computer Architecture (HPCA-10)*, pp. 232 - 241, Madrid, Spain, February 14-18, 2004. (accepted 27 out of 151 submissions, acceptance rate: 18%)
- J. S. Hu, A. Nadgir, N. Vijaykrishnan, M. J. Irwin, M. Kandemir. Exploiting Program Hotspots and Code Sequentiality for Instruction Cache Leakage Management. In *Proc. of the International Symposium on Low Power Electronics and Design (ISLPED'03)*, pp. 402 - 407, Seoul, Korea, August 25-27, 2003. (accepted 54 out of 221 submissions, acceptance rate: 24%)
- J. S. Hu, N. Vijaykrishnan, M. J. Irwin, M. Kandemir. Using Dynamic Branch Behavior for Power-Efficient Instruction Fetch. In *Proc. of IEEECS Annual Symposium on VLSI (ISVLSI 2003)*, pp. 127 - 132, Tampa, Florida, February 20-21, 2003. (accepted 26 out of 115 submissions, acceptance rate: 23%)
- W. Zhang, J. S. Hu, V. Degalahal, M. Kandemir, N. Vijaykrishnan, and M. J. Irwin. Compiler-Directed Instruction Cache Leakage Optimization. In *Proc. of the 35th Annual International Symposium on Microarchitecture (MICRO-35)*, pp. 208 - 218, Istanbul, Turkey, November 18-22, 2002. (accepted 36 out of 150 submissions, acceptance rate: 24%)
- J. S. Hu, M. Kandemir, N. Vijaykrishnan, M. J. Irwin, H. Saputra, and W. Zhang. Compiler-Directed Cache Polymorphism. In *Proc. of ACM SIGPLAN Joint Conference on Languages, Compilers, and Tools for Embedded Systems (LCTES'02) and Software and Compilers for Embedded Systems (SCOPES'02)*, pp. 165 - 174, Berlin, Germany, June 19-21, 2002. (accepted 25 out of 73 submissions, acceptance rate: 34%)
- H. Saputra, M. Kandemir, N. Vijaykrishnan, M. J. Irwin, J. S. Hu, C-H. Hsu, and U. Kremer. Energy-Conscious Compilation Based on Voltage Scaling. In *Proc. of ACM SIGPLAN Joint Conference on Languages, Compilers, and Tools for Embedded Systems (LCTES'02) and Software and Compilers for Embedded Systems (SCOPES'02)*, pp. 2 - 11, Berlin, Germany, June 19-21, 2002. (accepted 25 out of 73 submissions, acceptance rate: 34%)
- J. S. Hu, N. Vijaykrishnan, M. Kandemir, and M. J. Irwin. Power-Efficient Trace Caches. In *Proc. of the 5th Design Automation and Test in Europe Conference (DATE'02)*, p. 1091 (Poster), Paris, France, 4-8 March, 2002. (accepted 210 out of 476 submissions, acceptance rate: 44%)

#### Miscellaneous

- N. Vijaykrishnan and Jie S. Hu. Designing Energy Aware Systems. In MRTC (Malardalen Real-Time Research Centre) Report, pp. 12 - 15. ISSN 1404-3041, ISRN MDH-119/2004-1-SE, 2004. Invited Paper.
- J. S. Hu, M. J. Irwin, N. Vijaykrishnan, M. Kandemir. Selective Trace Cache: A Low Power and High Performance Fetch Mechanism. Technical Report CSE-02-016, Department of Computer Science and Engineering, Pennsylvania State University, October 22, 2002.

#### THESES

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- Ph.D. Dissertation: Orchestrating the Compiler and Microarchitecture for Reducing Cache Energy.
- Master's Degree Thesis: The Design and Implementation of the MicroKernel for ECOBASE - An Embedded Database Management System (in Chinese).
- Bachelor's Degree Thesis: The Adoption of the Kernel I of COBASE in HongBo Communication Network (in Chinese).

#### PROFESSIONAL TALKS

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- *In-Register Duplication: Exploiting Narrow-Width Value for Improving Register File Reliability*, at the International Conference on Dependable Systems and Networks (DSN-2006), Philadelphia, PA, June 25-28, 2006.
- *Optimizing the Thermal Behavior of Subarrayed Data Caches* at IEEE International Conference of Computer Design (ICCD-2005), San Jose, California, October 2-5, 2005.

- *Orchestrating the Compiler and Microarchitecture for Reducing Cache Energy* at Electrical and Computer Engineering Department, University of Rochester, Rochester, NY, March 23, 2004.
- *Orchestrating the Compiler and Microarchitecture for Reducing Cache Energy* at Electrical and Computer Engineering Department, University of Minnesota, Minneapolis, MN, March 9, 2004.
- *Orchestrating the Compiler and Microarchitecture for Reducing Cache Energy* at Electrical and Computer Engineering Department, New Jersey Institute of Technology, Newark, NJ, March 2, 2004.
- *Exploiting Program Hotspots and Code Sequentiality for Instruction Cache Leakage Management* (Poster Presentation) at GSRC Annual Symposium, Santa Clara, CA, September 18-19, 2003.
- *Compiler and Architectural Mechanisms for ICache Leakage Management* at GSRC Workshop, Oakland, CA, March 20-21, 2003.
- *Compiler-directed Cache Polymorphism* at LCTES'02/SCOPEs'02, Berlin, Germany, June 19-21, 2002.
- *Energy-Conscious Compilation Based on Voltage Scaling* at LCTES'02/SCOPEs'02, Berlin, Germany, June 19-21, 2002.

#### GRADUATE/UNDERGRADUATE STUDENT SUPERVISING

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Name	Program	Research Topic
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- Shuai Wang, Ph.D., On the Characterization and Optimization of On-Chip Memory Structure Reliability, Spring 2009
- Chaoyi Wang, MS, Power/Energy Management in Wireless Sensor Networks, Fall 2009
- Parijat Shukla, MS, Reliable Computing via Hardware Transaction Processing, Fall 2009

#### GRADUATED STUDENTS

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Name	Program	Research Topic
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- Yuncong Zhang, MS, Exploiting Narrow-Width Value for VLIW Register File Designs, Fall 2008
- Chris Onjian, MS, Case Studies of Design and Implementation Issues Resulting in Data Integrity Problems in Real Time Embedded Systems, Spring 2008
- Gobinder Waraich, MS, Digital Alarm Clock with Temperature Display, Fall 2007
- Ying Zhu, MS, Adopting Freescale PBMUSLK/AP52233SLK for Educational Projects, Fall 2007
- Carla Nunez, MS, Power-/Complexity-Effective Register Files in SMT Processors, May 2007
- Michael Kramarczyk, MS, A System Approach for Designing and Implementing TTDL, Fall 2006
- Sree Lakshmi, MS, Improving Data Cache Performance and Power Efficiency via Store Buffering, 2005
- Farhan Javed, Senior Project, Sensor Network Communication, Spring 2007
- Muzaffar Zaman, Senior Project, Sensor Network Communication, Spring 2007
- Gian Francisco, Senior Project, ASIC Encoder with an Integrated Look-up Table (2nd Place Winner), Spring 2007
- Swati Jani, Senior Project, ASIC Encoder with an Integrated Look-up Table (2nd Place Winner), Spring 2007
- Akinola Akiwowo, Senior Project, ASIC Encoder with an Integrated Look-up Table (2nd Place Winner), Spring 2007
- Joannie Bautista, Senior Project, Power-Aware Register File Designs, 2006
- Luis Salinas, Senior Project, Power-Aware Register File Designs, 2006
- Waqas Mahmood, Senior Project, Leakage Behavior of SRAM Memory and Its Optimizations, 2005
- Tim Hutchins, Senior Project, Leakage Behavior of SRAM Memory and Its Optimizations, 2005

Name	Advisor	Thesis
		<ul style="list-style-type: none"><li>• Jingong Pan, Dr. Mengchu Zhou, Modeling and Analysis of Bionetwork Using Petri Nets, 2008</li><li>• Muhammad Z. Hasan, Dr. Sotirios G. Ziavras, Vector Customization and Reconfiguration Management for Dynamic Embedded Applications, 2007</li><li>• Chuan-bi Lin, Dr. Roberto Rojas-Cessa, Design and Analysis of Scalable Scheduling Schemes for High-Speed Input-Queued Packet Switches, 2007</li><li>• Ziqian Dong, Dr. Roberto Rojas-Cessa, Architecture Design and Performance Analysis of Practical Buffered Crossbar Switches, 2007</li><li>• Xin Tang, Dr. Constantine N. Manikopoulos, Generalized Anomaly Detection Model for Windows-Based Malicious Program Behavior, 2007</li><li>• Li Ling, Dr. Constantine N. Manikopoulos, Unified Architecture of the Mobile Ad Hoc Network Security (MANS) System, 2006</li><li>• Xizhen Xu, Dr. Sotirios G. Ziavras, H-SIMD Machine: Configurable Parallel Computing for Data-Intensive Applications, 2006</li><li>• Zhen Guo, Dr. Roberto Rojas-Cessa, Design and stability analysis of high performance switches, 2005</li><li>• Sui Song, Dr. Constantine N. Manikopoulos, Management and Control of A Computer Under Denial of Service Attacks, 2005</li><li>• Zhen Guo, Dr. Lev Zakrevski, Mobility Prediction in Mobile Ad Hoc Networks and Sensor Networks, 2005</li><li>• Xiaofang Wang, Dr. Sotirios G. Ziavras, Design and Resource Management of Reconfigurable Multiprocessors for Data-Parallel Applications, 2005</li><li>• Dejiang Jin, Dr. Sotirios G. Ziavras, A Versatile Programming Model for Dynamic Scheduling on Cluster Computers, 2005</li><li>• Nabeel Al-Saber (MS), Dr. Sotirios G. Ziavras, Kerberos Secure Phone Messenger, Fall 2007</li><li>• Qing Zhu (MS), Dr. Sotirios G. Ziavras, Two Factor Authentication and Authorization in Mobile Computing, Fall 2007</li><li>• Ronak Sutaria (MS), Dr. Constantine N. Manikopoulos, Classifying Malicious Windows Executables Using Anomaly based Detection, 2005</li></ul>