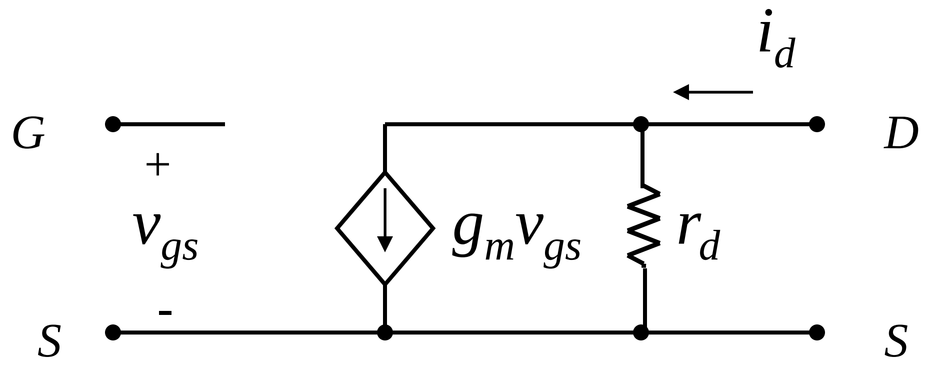
Frequency Response

Lesson #10

FET

Section 8.2

Equivalent Circuit Of An FET



where

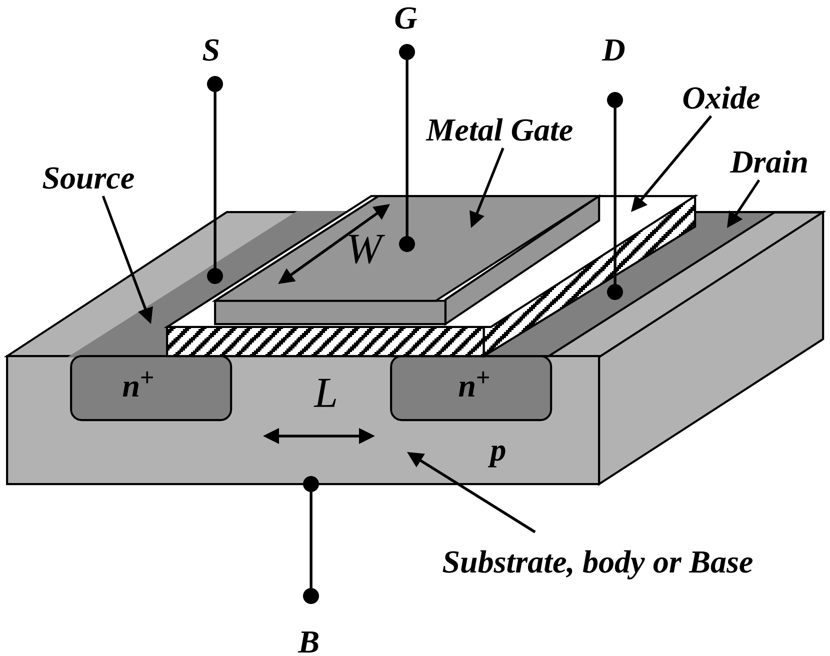
and

$$i_d(t) = g_m v_{gs}(t) + \frac{v_{ds}(t)}{r_d}$$

$$g_m = \left.\frac{i_d}{v_{gs}}\right|_{v_{ds}=0} \cong \left.\frac{\Delta i_D}{\Delta v_{GS}}\right|_{v_{DS}=V_{DSQ}} \qquad \frac{1}{r_d} = \left.\frac{i_d}{v_{ds}}\right|_{v_{gs}=0} \cong \left.\frac{\Delta i_D}{\Delta v_{DS}}\right|_{v_{GS}=V_{GSQ}}$$

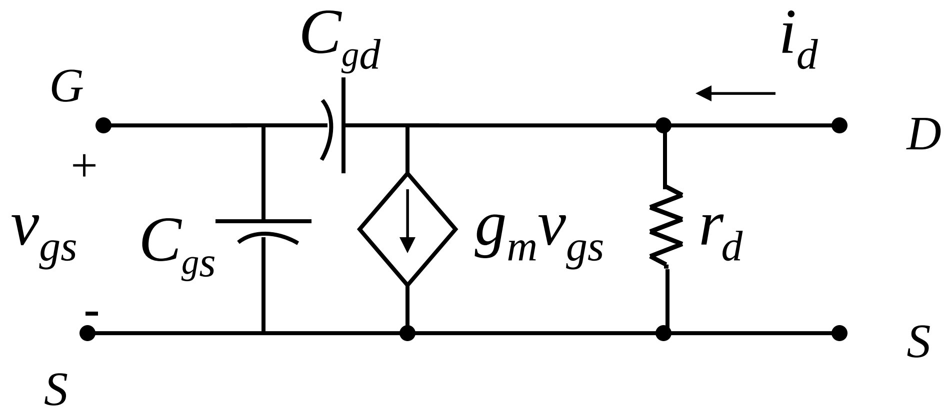
$$g_m = \left.\frac{\partial i_D}{\partial v_{GS}}\right|_{\text{Q-point}} \qquad \frac{1}{r_d} = \left.\frac{\partial i_D}{\partial v_{DS}}\right|_{\text{Q-point}}$$

Metal Oxide Semiconductor Field Effect Transistor MOSFET (NMOS) Enhancement Mode



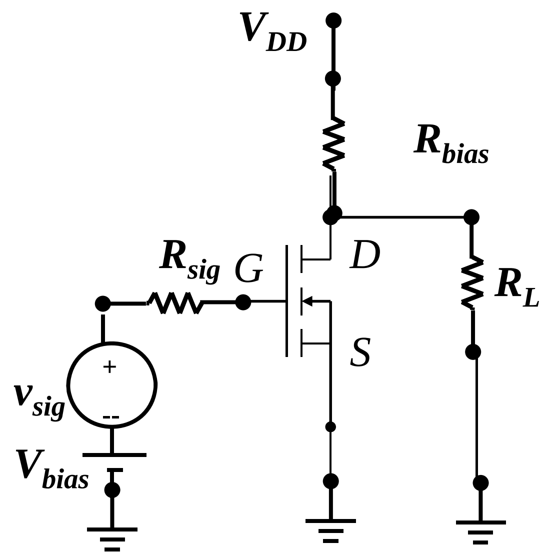
- Consists of Four terminals
  - Drain which is *n*-doped material
  - Source also *n*-doped material
  - Base which is *p*-doped material
  - Gate is a metal and is insulated from the Drain, Source and Base by a thin layer of silicon dioxide ~ .05-.1μm thick
- Basically, an electric current flowing from drain to source, i_D, is controlled by the amount of voltage (electric field) appearing between the gate and base (note that the base and source are usually tied together and therefore, it is referred to as the gate to source voltage or gate voltage), v_{GS}.
- i_D flows through a channel of n-type material which is induced by v_{GS}. The amount of i_D is a function of the thickness of the channel and the voltage between drain and source, v_{DS}
- However, the thickness of channel is controlled by the level of gate voltage. (The width, .5 to 500 μm, and length, .2 to 10 μm, of the channel is shown in the diagram.)

FET Equivalent Circuit Updated for High Frequencies

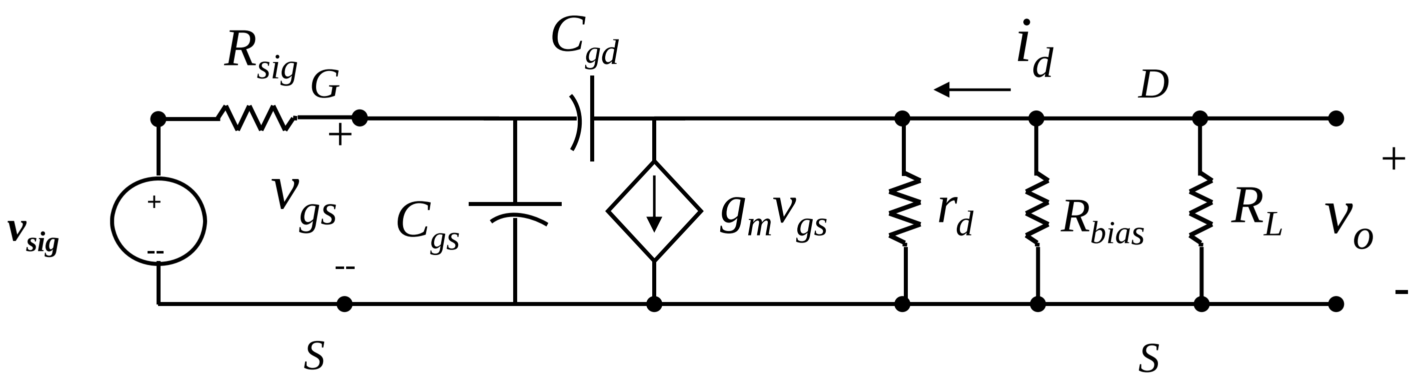


C_{gs} and C_{gd} account for the capacitance effects between the gate and source and between the gate and drain.

An Example

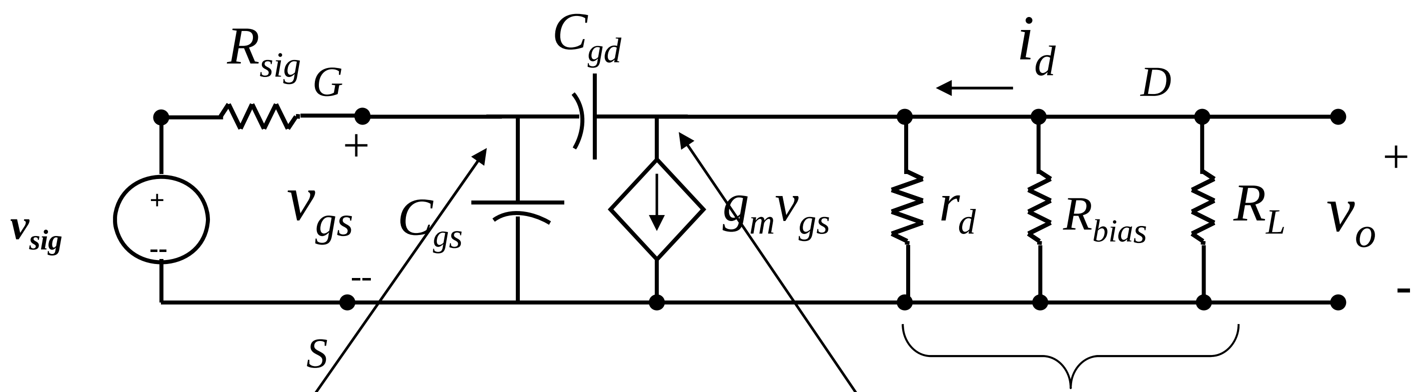


V_DD
R_bias
R_sig
G
D
S
R_L
v_sig
V_bias



R_sig
G
C_gd
i_d
D
+
v_gs
--
C_gs
g_m v_gs
r_d
R_bias
R_L
v_o
+
-
v_sig
S
S

Example Continued



$$\text{Equivalent Load} = R'_L = \frac{1}{1/r_d + 1/R_{bias} + 1/R_L}$$

Gate Nodal Equation using KCL

$$\frac{V_{gs}(s) - V_{sig}(s)}{R_{sig}} + \frac{V_{gs}(s)}{1/(sC_{gs})} + \frac{V_{gs}(s) - V_0(s)}{1/(sC_{gd})} = 0$$

Drain Nodal Equation using KCL

$$\frac{V_o(s) - V_{gs}(s)}{1/(sC_{gd})} + \frac{V_o(s)}{R'_L} + g_m V_{gs}(s) = 0$$

Solving these two equations for V_{gs} and combining:

$$A_v(s) = \frac{V_o}{V_{sig}} = -g_m R'_L \times \frac{1 - s(C_{gd}/g_m)}{1 + s[C_{gs}R_{sig} + C_{gd}(R_{sig} + g_m R'_L R_{sig} + R'_L)] + s^2 C_{gs} C_{gd} R_{sig} R'_L}$$

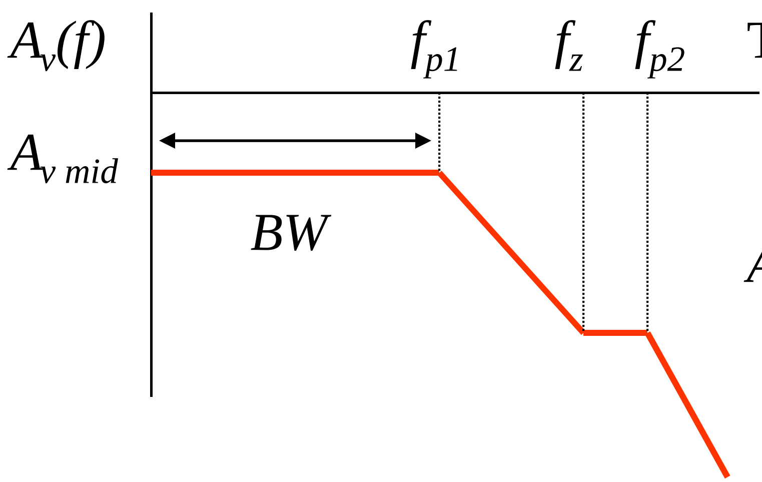
Breakpoint Frequencies

$$f_z = \frac{g_m}{2\pi C_{gd}}$$

$$f_{p1} = \frac{1}{2\pi\{C_{gd}(R'_L + R_{sig} + R_{sig}R'_L\, g_m) + C_{gs}R_{sig}\}}$$

$$f_{p2} = \frac{\{C_{gd}(R'_L + R_{sig} + R_{sig}R'_L\, g_m) + C_{gs}R_{sig}\}}{2\pi(C_{gs}C_{gd}R_{sig}R'_L)}$$

Assume that $f_{p2} > f_z >> f_{p1}$, then the bode plot would look like this:



Then the 3dB point (half-power point) frequency is f_{p1}, and the Bandwidth is defined as BW= $f_{p1} - 0 = f_{p1}$

$A_{v\ mid}$ is defined as the value of $Av(f)$ when the effects of frequency are small (i.e., when $|A_v(f)| > A_v(f_{3dB})$)

Bandwidth

$$BW = \frac{1}{2\pi\{C_{gd}(R'_L + R_{sig} + R_{sig}R'_L\, g_m) + C_{gs}R_{sig}\}}$$

Note that to increase the bandwidth we can:

1. Reduce device capacitances: C_{gs} & C_{gd}
2. Reduce source and load resistances
3. Reduce the capacitance which has the biggest effect. In this case $C_{gd}g_mR'_LR_{sig}$ (= $C_{gd}|A_{mid}|R_{sig}$) dominates, so reducing C_{gd} as opposed to C_{gs} would have a bigger payoff.
4. Reducing $|A_{mid}|=|g_mR'_L|$ will also increase the bandwidth.

NOTE increasing the BW will reduce the gain. We define Gain-BW product.

The Algebra

$$V_{gs}[\frac{1}{R_{sig}} + s(C_{gs} + C_{gd})] = V_{sig}\frac{1}{R_{sig}} + V_o s C_{gd}$$

$$V_{gs}(g_m - sC_{gd}) + V_o(sC_{gd} + \frac{1}{R'_L}) = 0$$

$$V_{gs} = -V_o\frac{(sC_{gd} + \frac{1}{R'_L})}{(g_m - sC_{gd})}$$

$$-V_o\frac{(sC_{gd} + \frac{1}{R'_L})}{(g_m - sC_{gd})}[\frac{1}{R_{sig}} + s(C_{gs} + C_{gd})] = V_{sig}\frac{1}{R_{sig}} + V_o s C_{gd}$$

$$V_o\{sC_{gd} + \frac{(sC_{gd} + \frac{1}{R'_L})}{(g_m - sC_{gd})}[\frac{1}{R_{sig}} + s(C_{gs} + C_{gd})]\} = -V_{sig}\frac{1}{R_{sig}}$$

$$V_o\{sR_{sig}C_{gd} + \frac{(sC_{gd} + \frac{1}{R'_L})}{(g_m - sC_{gd})}[1 + sR_{sig}(C_{gs} + C_{gd})]\} = -V_{sig}$$

$$V_o\{sR_{sig}C_{gd} + \frac{(sR'_L C_{gd} + 1)}{R'_L(g_m - sC_{gd})}[1 + sR_{sig}(C_{gs} + C_{gd})]\} = -V_{sig}$$

$$\frac{V_o}{V_{sig}} = -R'_L g_m \frac{(1 - s\frac{C_{gd}}{g_m})}{s^2 R_{sig}R'_L C_{gs}C_{gd} + s(R_{sig}C_{gd}R'_L g_m + R'_L C_{gd} + R_{sig}C_{gs} + R_{sig}C_{gd}) + 1}$$

$$s_{12} = \frac{-(R_{sig}C_{gd}R'_L g_m + R'_L C_{gd} + R_{sig}C_{gs} + R_{sig}C_{gd}) \pm \sqrt{(R_{sig}C_{gd}R'_L g_m + R'_L C_{gd} + R_{sig}C_{gs} + R_{sig}C_{gd})^2 - 4R_{sig}R'_L C_{gs}C_{gd}}}{2R_{sig}R'_L C_{gs}C_{gd}}$$

$$(s + s_1)(s + s_2) = s^2 + (s_1 + s_2)s + s_1 s_2 = s^2 + bs + c$$

$$s_1 + s_2 = b; s_1 s_2 = c$$

if $s_1 >> s_2$; then $s_1 + s_2 \approx s_1 = b; s_2 = \frac{c}{s_1} = \frac{c}{b}$

$$s_1 = \frac{R_{sig}C_{gd}R'_L g_m + R'_L C_{gd} + R_{sig}C_{gs} + R_{sig}C_{gd}}{R_{sig}R'_L C_{gs}C_{gd}};$$

$$s_2 = \frac{\frac{1}{R_{sig}R'_L C_{gs}C_{gd}}}{s_1} = \frac{\frac{1}{R_{sig}R'_L C_{gs}C_{gd}}}{\frac{R_{sig}C_{gd}R'_L g_m + R'_L C_{gd} + R_{sig}C_{gs} + R_{sig}C_{gd}}{R_{sig}R'_L C_{gs}C_{gd}}}$$

$$= \frac{1}{R_{sig}C_{gd}R'_L g_m + R'_L C_{gd} + R_{sig}C_{gs} + R_{sig}C_{gd}}$$

$$f_1 = \frac{R_{sig}C_{gd}R'_L g_m + R'_L C_{gd} + R_{sig}C_{gs} + R_{sig}C_{gd}}{2\pi R_{sig}R'_L C_{gs}C_{gd}};$$

$$f_2 = \frac{1}{2\pi(R_{sig}C_{gd}R'_L g_m + R'_L C_{gd} + R_{sig}C_{gs} + R_{sig}C_{gd})}$$

and $f_1 >> f_2$ and Bandwidth is f_2

Homework

- FET
  - Problems: 8.12 (r_d=*40k*),13,14,16,17