Field Effect Transistors

Lesson #3

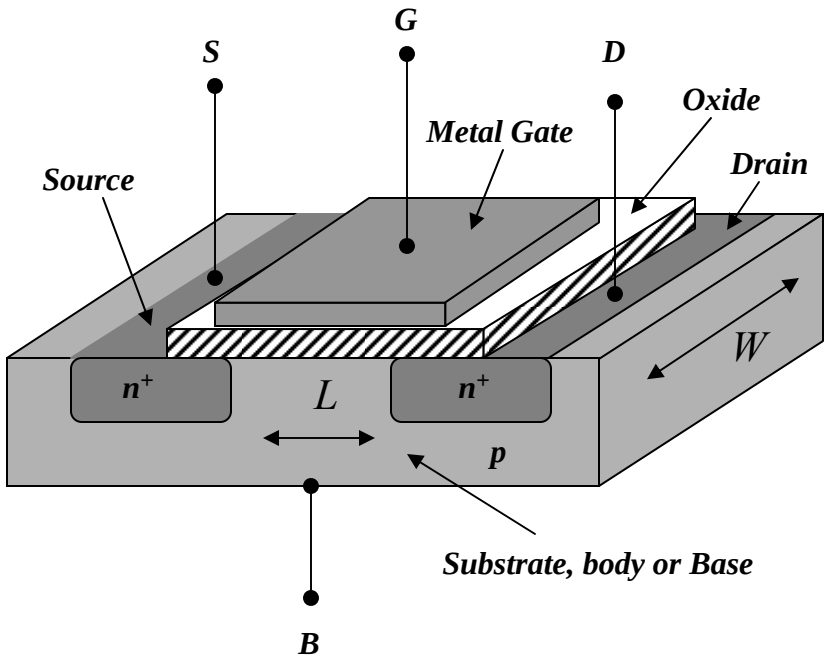
MOSFETS

Sections 5.1-3

Types of FET

- Metal Oxide Semiconductor Field Effect Transistor – MOSFET
  - Enhancement mode
  - Depletion mode
- Junction FETs
- *p* channel vs *n* channel

Metal Oxide Semiconductor Field Effect Transistor MOSFET (NMOS) Enhancement Mode



- Consists of Four terminals
  - Drain which is *n*-doped material
  - Source also *n*-doped material
  - Base which is *p*-doped material
  - Gate is a metal and is insulated from the Drain, Source and Base by a thin layer of silicon dioxide ~ .05-.1μm thick
- Basically, an electric current flowing from drain to source, $\boldsymbol{i_D}$, is controlled by the amount of voltage (electric field) appearing between the gate and base (note that the base and source are usually tied together and therefore, it is referred to as the gate to source voltage or gate voltage), $\boldsymbol{v_{GS}}$.
- $\boldsymbol{i_D}$ flows through a channel of n-type material which is induced by $\boldsymbol{v_{GS}}$. The amount of $\boldsymbol{i_D}$ is a function of the thickness of the channel and the voltage between drain and source, $\boldsymbol{v_{DS}}$
- However, the thickness of channel is controlled by the level of gate voltage. (The width, .5 to 500 μm, and length, .2 to 10 μm, of the channel is shown in the diagram.)

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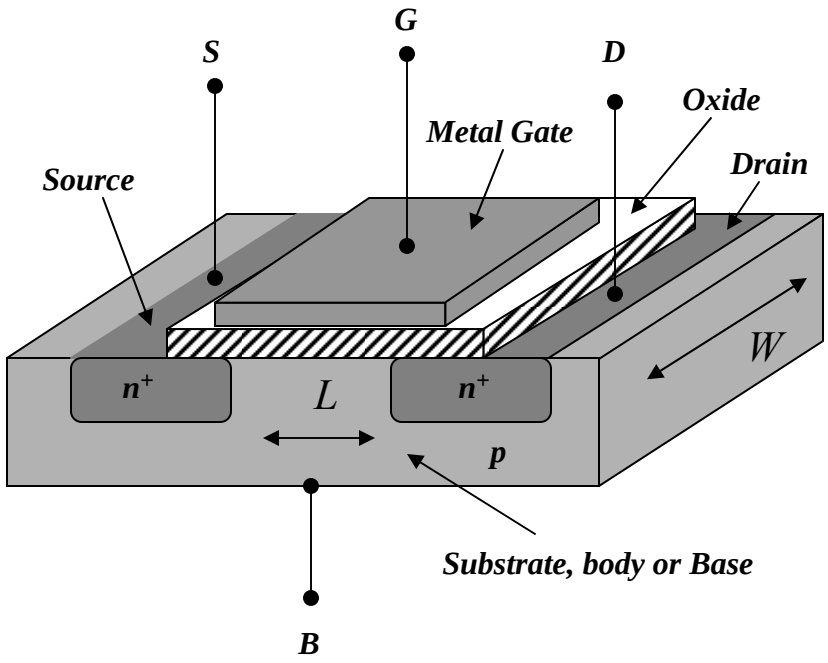

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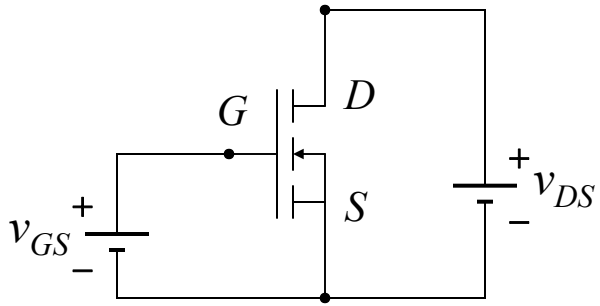
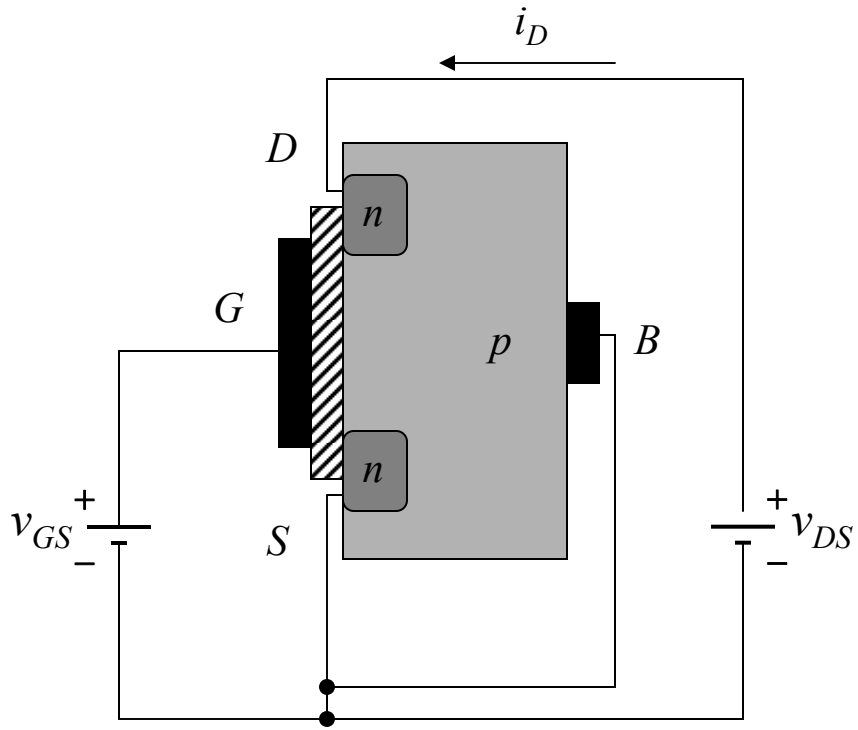
Modes of the NMOS
Cutoff

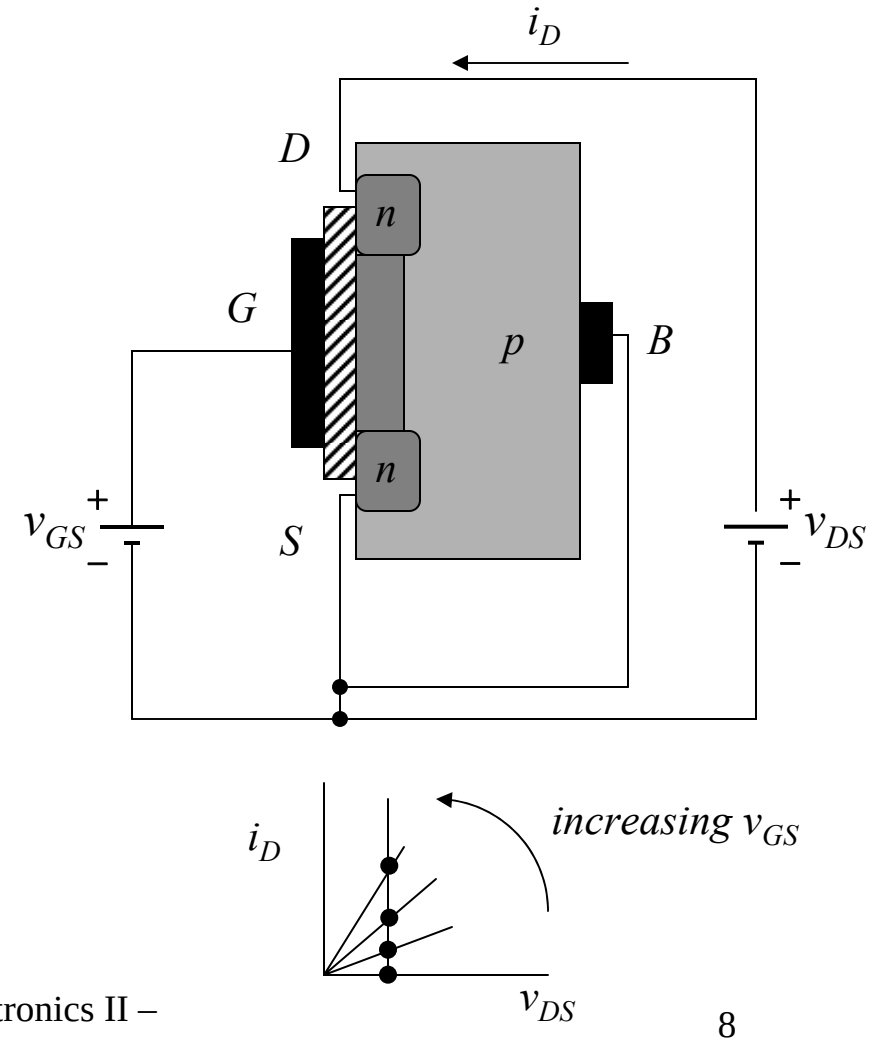
- $v_{GS} = 0$
- *pn* junctions at the drain and source are reverse biased due to v_{DS}
- i_D is zero





Modes of the NMOS Triode Region

- $v_{GS} \geq V_{to}$ a threshold voltage which causes electrons in the base to be attracted to and holes to be repelled from the region just below the gate
- This process causes a n-type channel to form below the gate
- As v_{DS} is increased, i_D starts to flow. For small values of v_{DS}, $i_D \propto v_{DS}$
- In addition, $i_D \propto v_{GS}$- V_{to}, the excess gate voltage
- Therefore, the MOSFET can act as a voltage controlled resistor in the Triode Region (e.g., used in AGC circuits)



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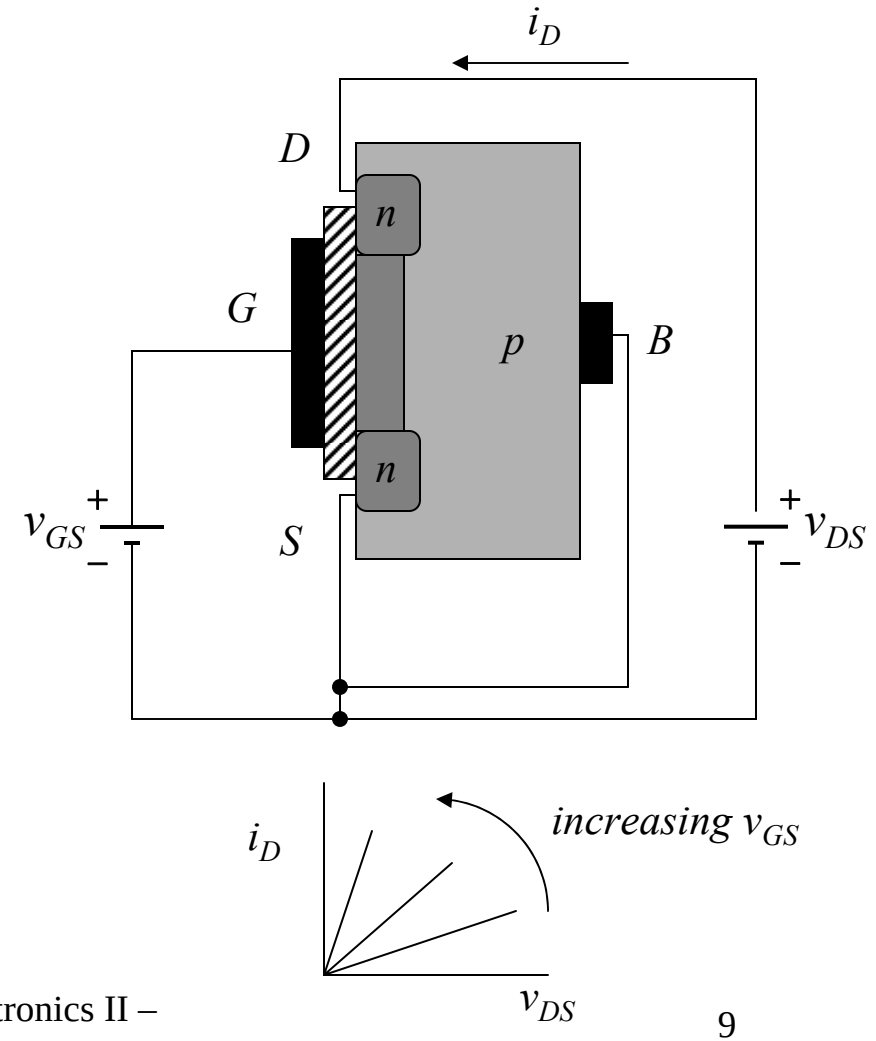


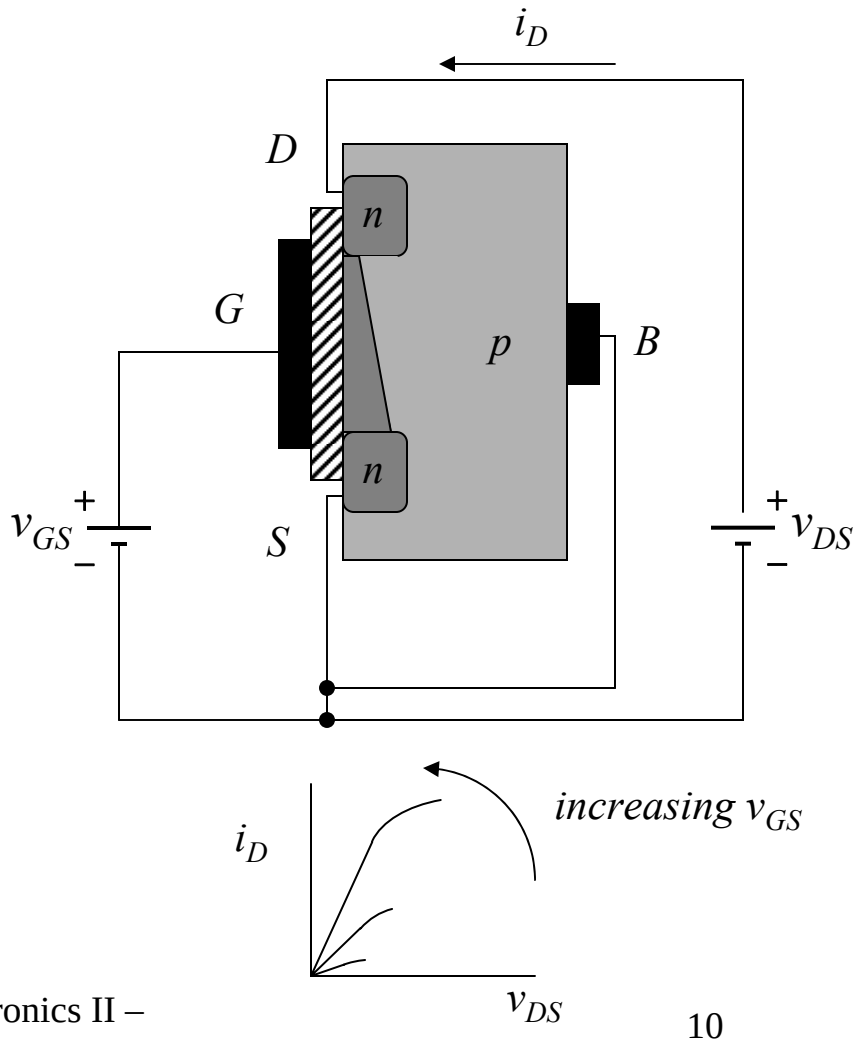
Modes of the NMOS
Triode Region (Continued)

- Since the drain is more positive than the source, the voltage difference between the channel and the gate varies along the channel from drain to source.
- As v_{DS} is further increased, this channel voltage profile causes a tapering of the channel thickness. $v_{GD} \neq v_{GS}$
- This tapering causes the resistance of the channel to increase (as v_{DS} increases) and, thereby, reduces the rate of increase of i_D.
- Furthermore, it can be shown that

$$i_D = K[2(v_{GS} - V_{to})v_{DS} - v_{DS}^2]$$

$$K = (\frac{W}{L})(\frac{KP}{2}) = (\frac{W}{L})(\frac{\mu_n C_{ox}}{2})$$

- To summarize: $v_{GS} \geq V_{to}$ and $v_{DS} < v_{GS} - V_{to}$

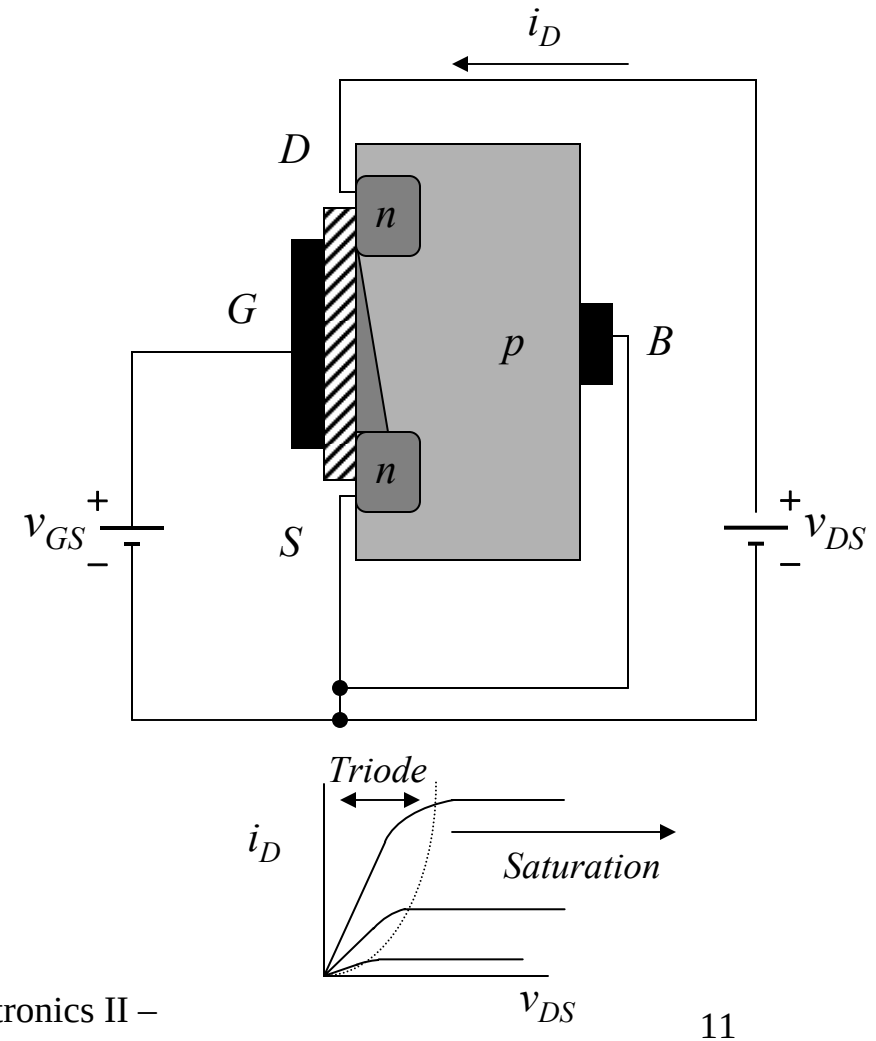


Modes of the NMOS Saturation

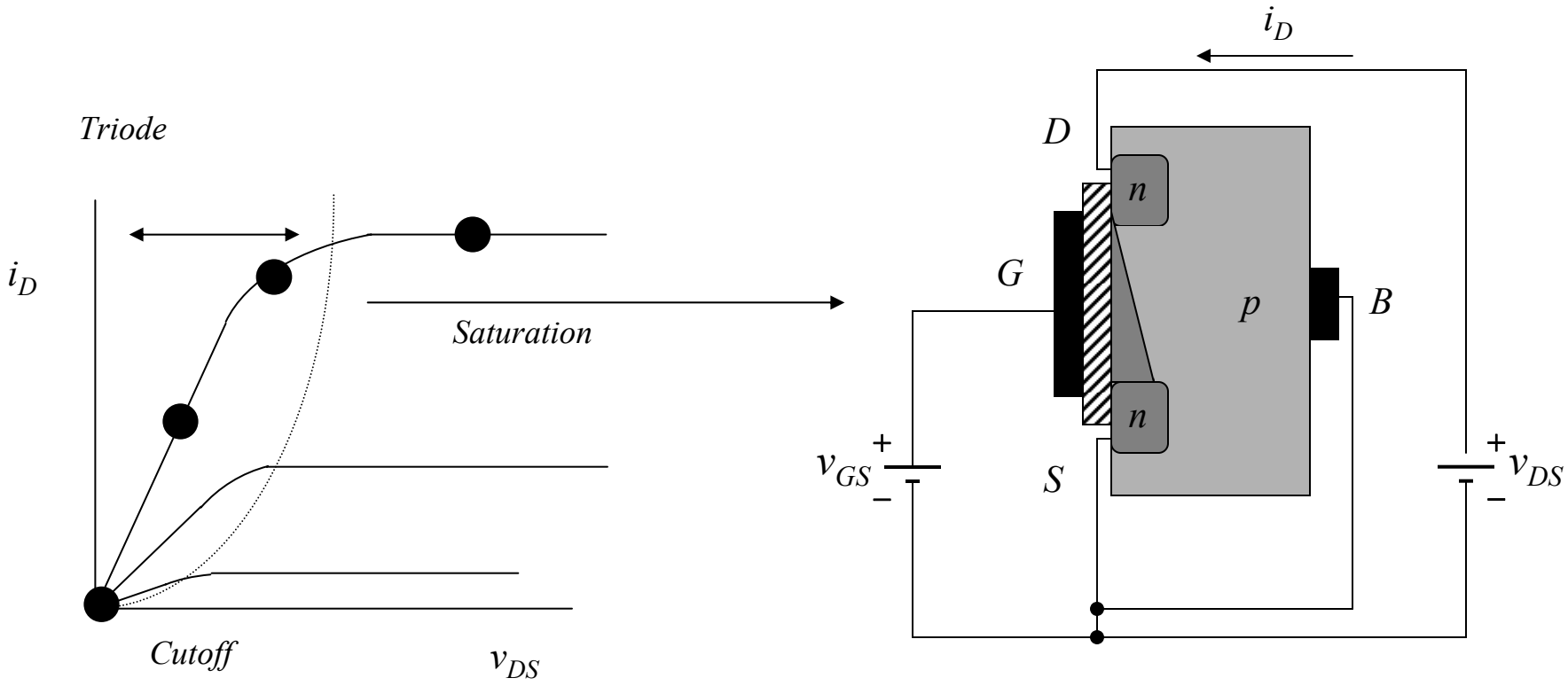
- As v_{DS} continues to increase, the voltage profile continues to taper. When the gate to channel voltage at the drain, v_{GD}, approaches V_{to}, the thickness of the channel at the drain is (virtually) zero. (Note that although the channel thickness is virtually zero, current flow is not cutoff since it is needed to support the channel voltage profile.)
- This phenomenon limits the amount of drain current (i.e., i_D is saturated) and causes i_D to be independent of v_{DS}
- Furthermore, it can be shown that

$$i_D = K(v_{GS} - V_{to})^2$$

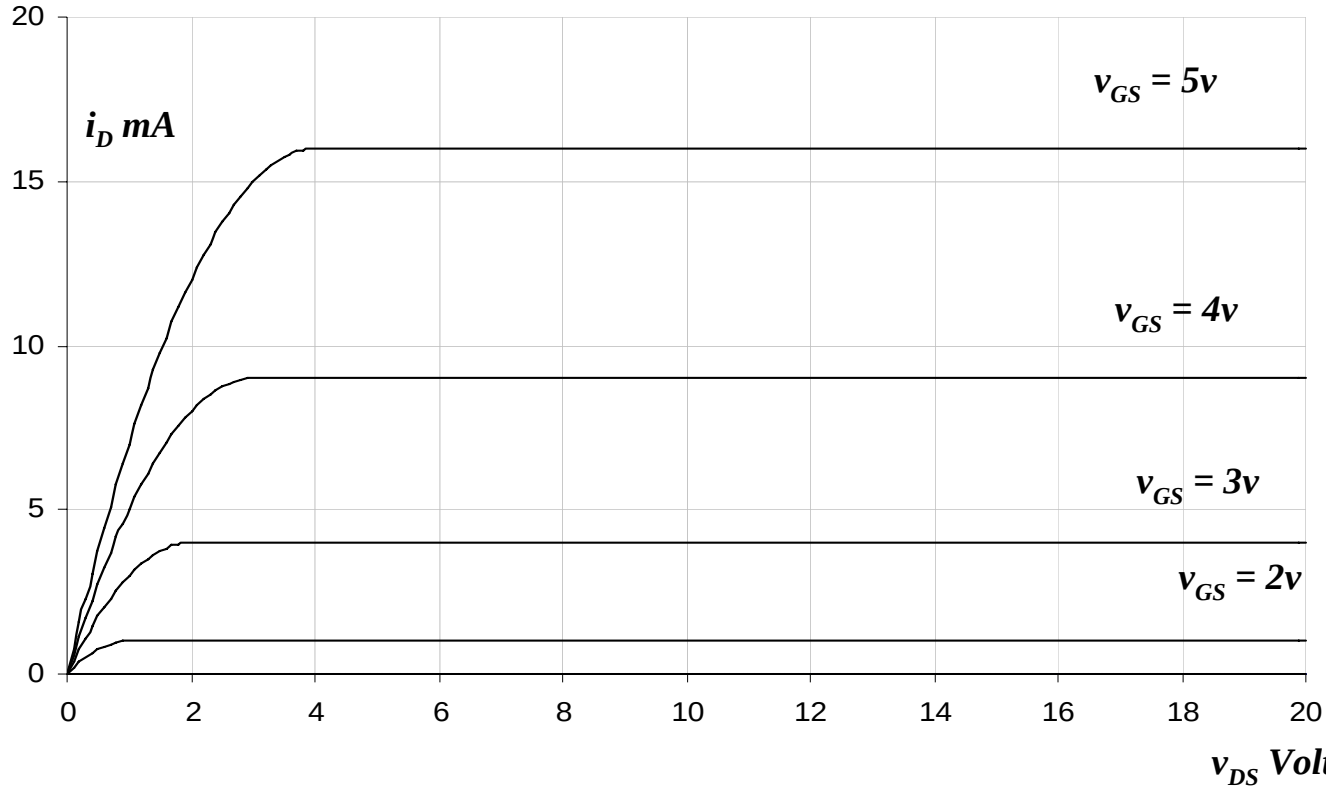
- Summarize: $v_{GS} \geq V_{to}$ and $v_{DS} \geq v_{GS} - V_{to}$



Modes of the NMOS



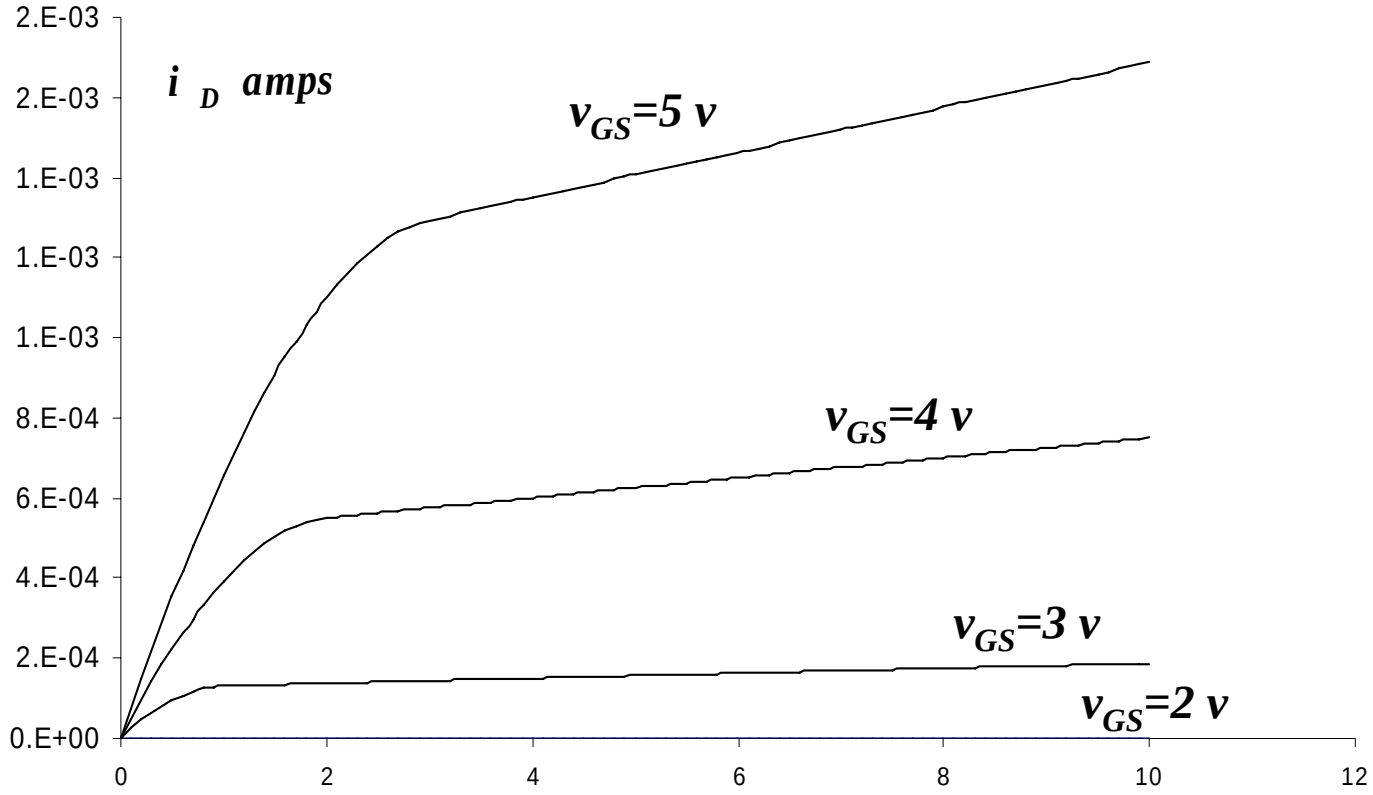
NMOS Characteristics



Note that $V_{to} = 1$

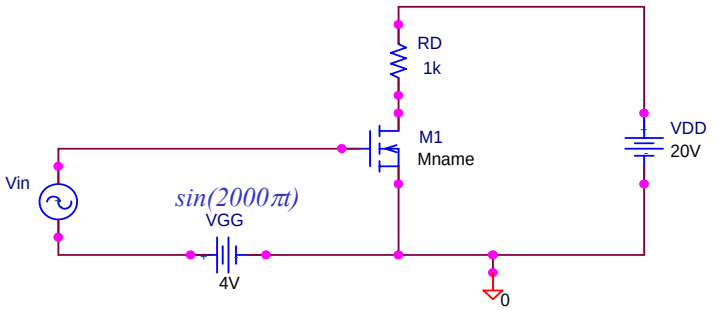
Note that for NMOS devices with short channel lengths, a tilt may exist due to the modulation of the channel length by the depletion region surrounding the drain.

NMOS Characteristics with Channel Length Modulation due to depletion region at the drain which mostly effects shorter channel lengths



Note that V_{to} = 2

Load Line of a NMOS Amplifier

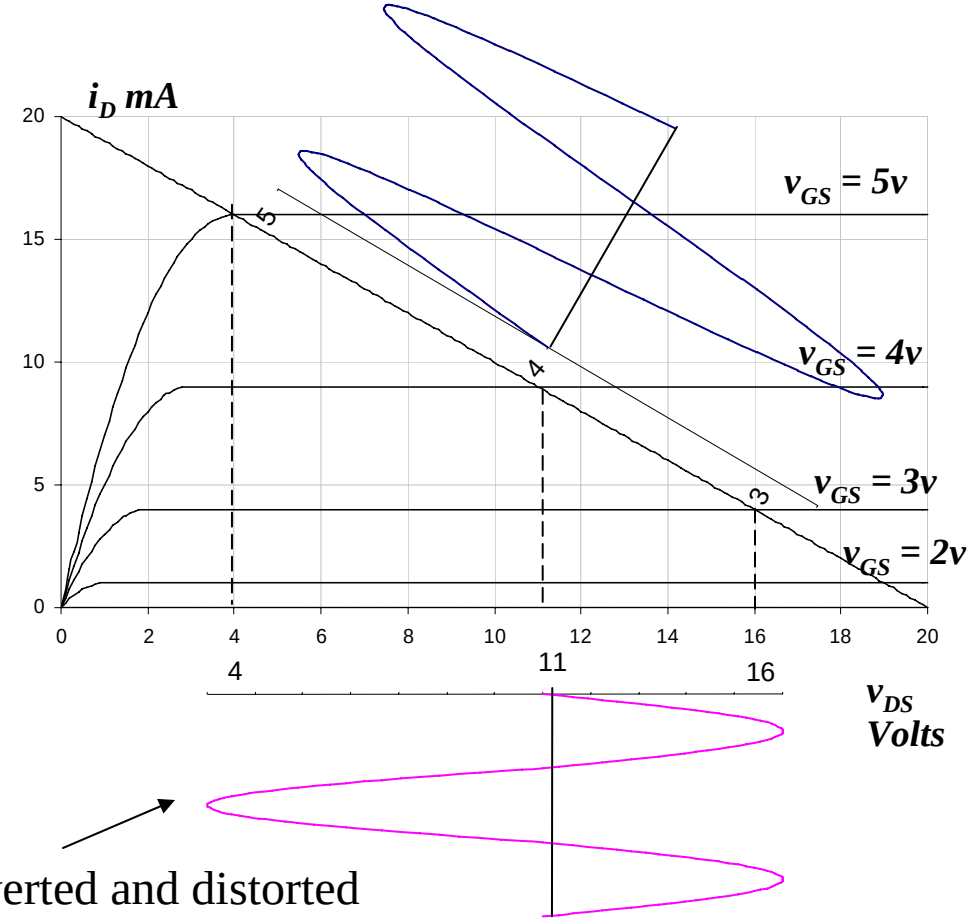


Gate Circuit

$$v_{GS} = v_{in}(t) + VGG$$
$$= \sin(2000\pi t) + 4$$

Drain Circuit

$$VDD = i_D RD + v_{DS}$$
$$20 = i_D 1000 + v_{DS}$$



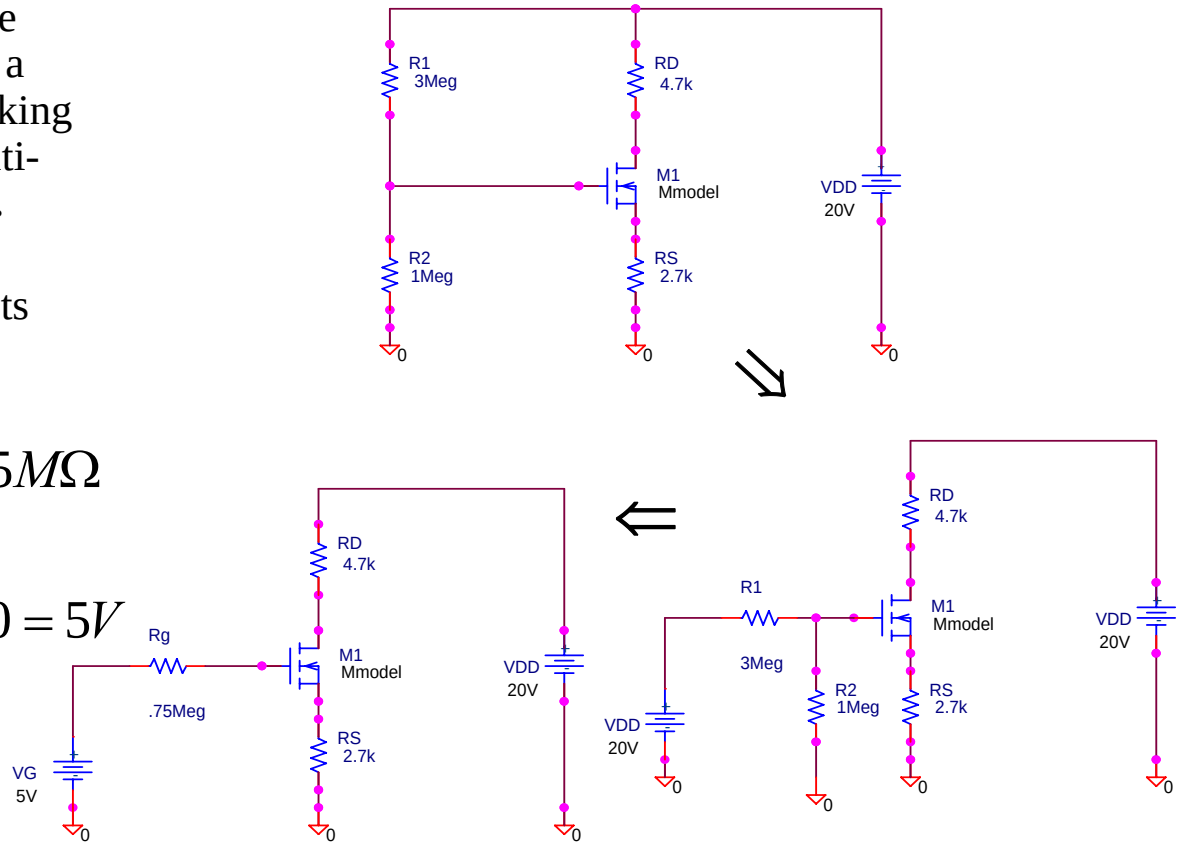
Inverted and distorted

Self-Bias NMOS Circuit

- This type of design allows the biasing of an amplifier using a single DC voltage source making amenable to be used in a multi-staged RC coupled amplifier**.**
- To analysis this circuit, let's replace the gate circuit with its Thevenin's equivalent.

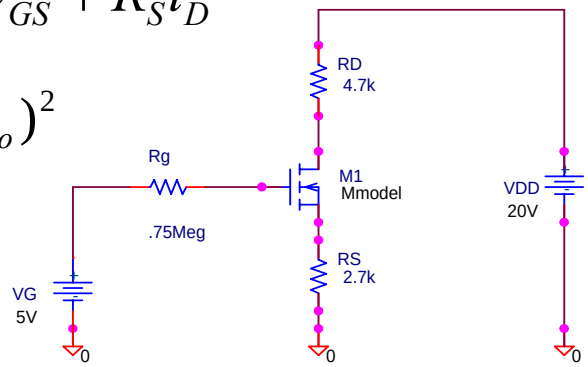
$$Rg = \frac{R_1 R_2}{R_1 + R_2} = \frac{3 \times 1}{3+1} = .75M\Omega$$

$$VG = \frac{R_2}{R_1 + R_2} VDD = \frac{1}{4} 20 = 5V$$



Self-Bias NMOS Circuit (Continued)

- Now the equation for the gate loop is: $VG = v_{GS} + R_S i_D$
- Assuming that the FET is to be designed in the saturation region, we have: $i_D = K(v_{GS} - V_{to})^2$
- Assuming $KP=50\mu A/V^2$, $V_{to}=2\ V$, $L=10\mu m$, & $W=400\mu m$; then $K=1mA/V^2$
- We can solve this equation graphically or analytically:



$$VG = v_{GS} + R_S K(v_{GS} - V_{to})^2 + i_{GS} R_g$$

SINCE NO CURRENT FLOWS IN THE GATE:

$$VG = v_{GS} + R_S K(v_{GS} - V_{to})^2$$

$$KR_S v_{GS}^{\ 2} + (1 - 2R_S K V_{to}) v_{GS} + R_S K V_{to}^{\ 2} - VG = 0$$

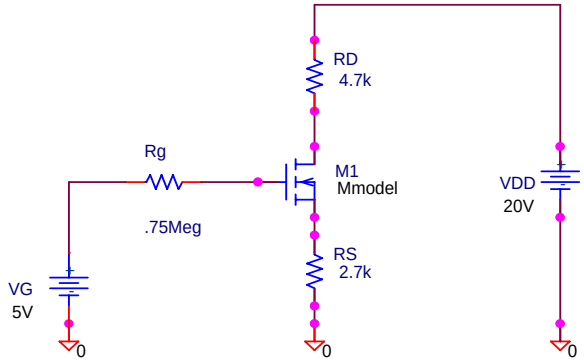
$$v_{GS}^{\ 2} + \left(\frac{1}{KR_S} - 2V_{to}\right) v_{GS} + V_{to}^{\ 2} - \frac{VG}{R_S K} = 0$$

$$v_{GS}^{\ 2} + \left(\frac{1}{2.7} - 4\right) v_{GS} + 4 - \frac{5}{2.7} = 0$$

$$v_{GS}^{\ 2} - (3.62963) v_{GS} + 2.148148 = 0$$

Self-Bias NMOS Circuit (Continued)

- Roots are v_{GS}=*2.885051, 0.744579*
- Choose v_{GS}=*2.885051* since $V_{GS} > V_{to}$=*2*
- $$I_{DQ} = K(v_{GS} - V_{to})^2 = (.885051)^2$$
$$= .78332ma$$
$$VDD = V_{DSQ} + I_{DQ}(RD + RS)$$
$$V_{DSQ} = 20 - .78332(7.4) = 14.203$$



Homework

- NMOS Transistors
  - Problems: 5.3, 5.4, 5.6
- Load-line Analysis
  - Problems: 5.14-19
- Bias Circuits
  - Problems: 5.21, 5.23