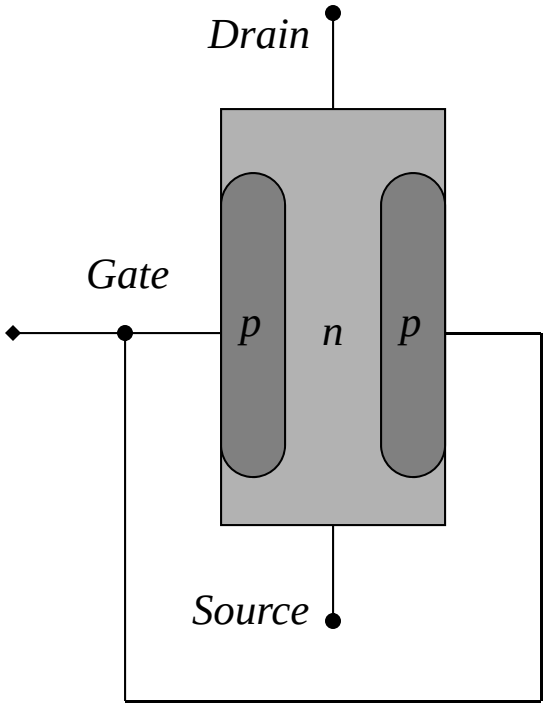
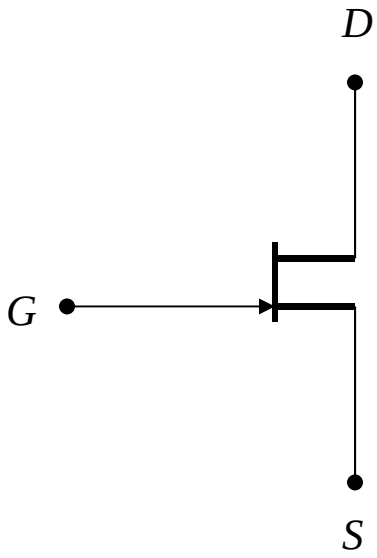
Junction FETs

Lesson #5

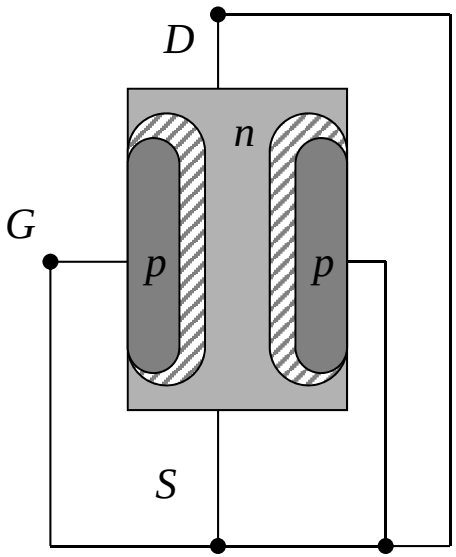
Section 5.7

n-channel Junction FET

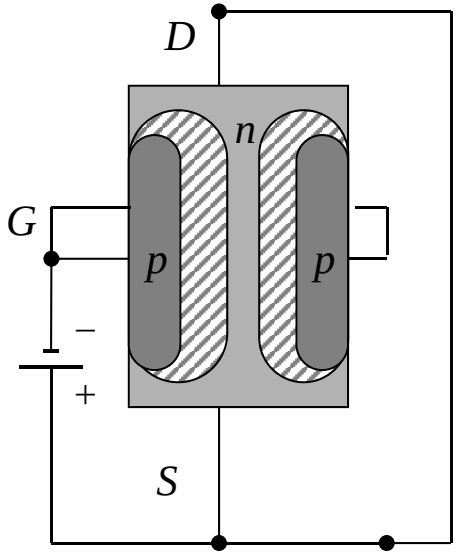




N-channel JFET Gate Bias

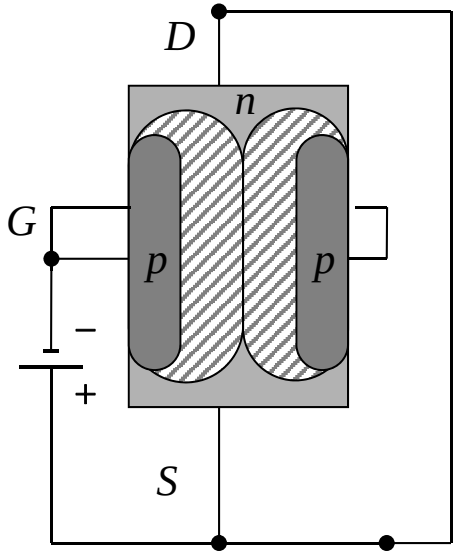


Zero Bias and depletion layer is thin and conduction channel exists from drain to source



$0 > v_{GS} > V_{to}$

Small bias results in larger depletion layer and smaller channel

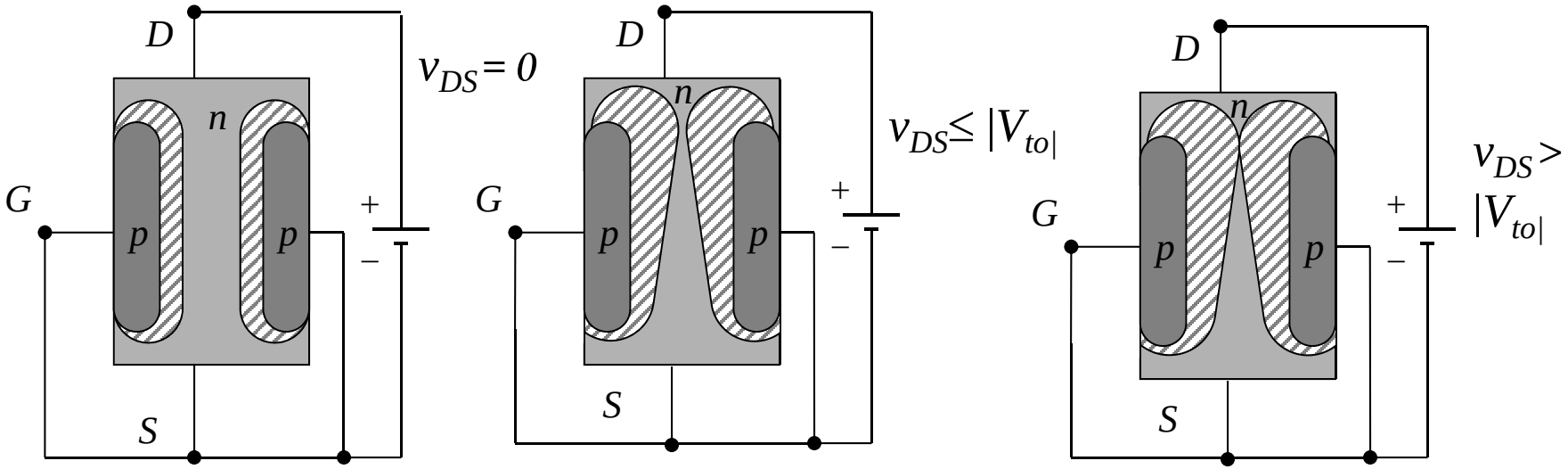


$v_{GS} \leq V_{to}$

Larger bias > pinch-off voltage, V_{to}, creates overlapping depletion layer and no conductive path from drain to source

Cutoff Region

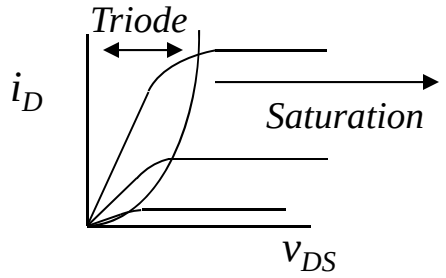
n-channel JFET Operation



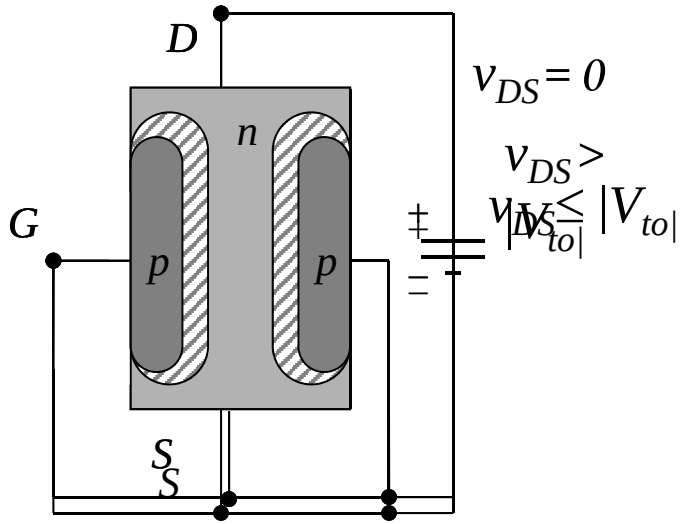
I_D=0 **Triode Region** **Saturation Region**

With $v_{GS}=0$, we increase v_{DS} and enter the Triode Region. As a result I_D increases and is proportional to v_{DS}. As v_{DS} increases further, the depletion region between drain and gate grows (with a larger area nearer the drain) and adds more resistance in the channel by narrowing its width. Thus, the rate of drain current increase slows down with increasing v_{DS}. As v_{DS} reaches the pinch-off voltage, V_{t0}, the drain current, I_D saturates (i.e., the FET is in the Saturation Region).

With $v_{GS}<0$, the same phenomenon occurs as v_{DS} is increased. However, the non-zero value of v_{GS} increases the resistance in the channel due to a large depletion layer and therefore, values of I_D are smaller both in the Triode and Saturation regions.



n-channel JFET Operation



Triode Region

Saturation Region

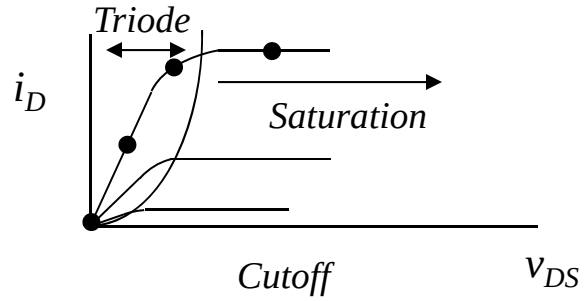
As v_{DS} increases, i_D increases and JFET enters the "Triode Region" Increasing v_{DS} increases the potential

While v_{DS} increases, the depletion region also grows with a larger area at the drain.

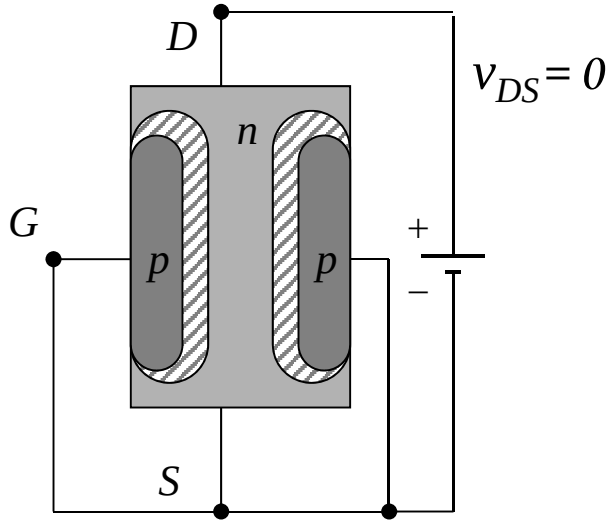
The depletion region increases as v_{DS} increases. Proportional the depletion region is

As a result, the channel resistance increases and increases in I_D are reduced.

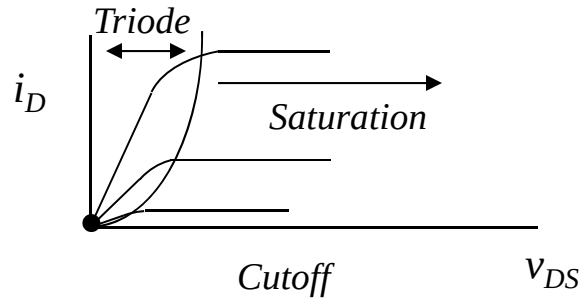
"pinched off" and I_D does not increase any further (i.e., I_D is saturated).



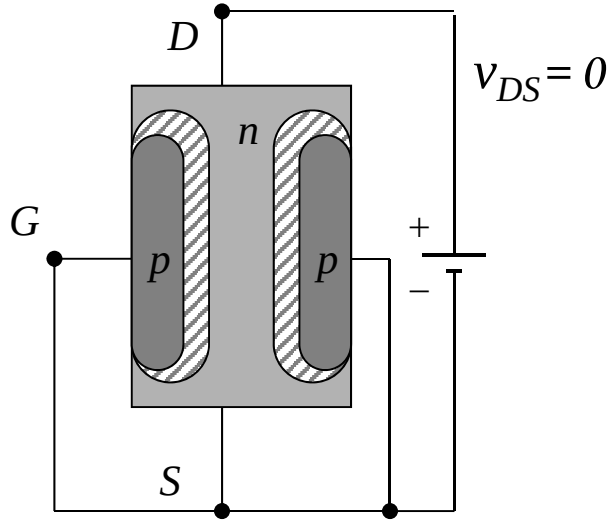
n-channel JFET Operation



As v_{DS} increase I_D increases and JFET enters the Triode Region.

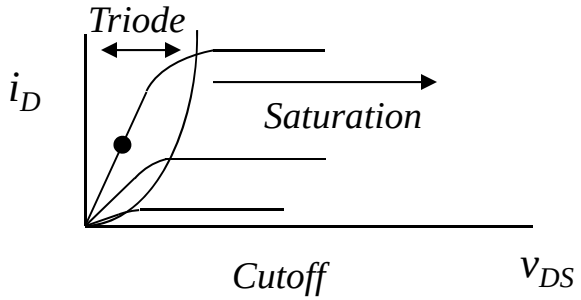


n-channel JFET Operation

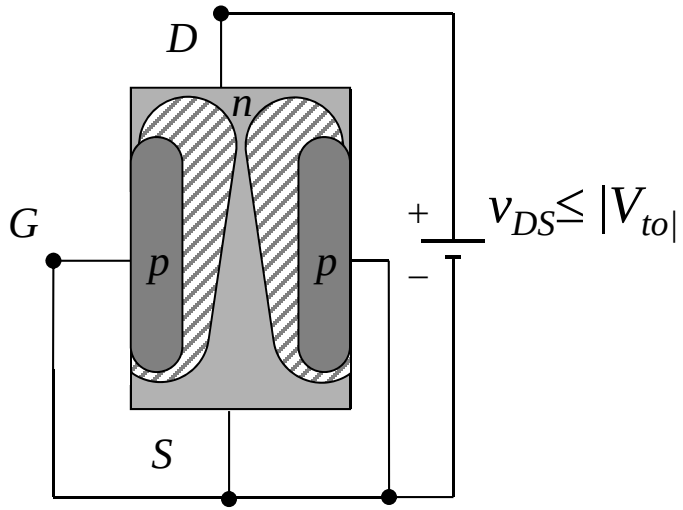


Triode Region

Because the channel is "wide", I_D is proportional to v_{DS}.

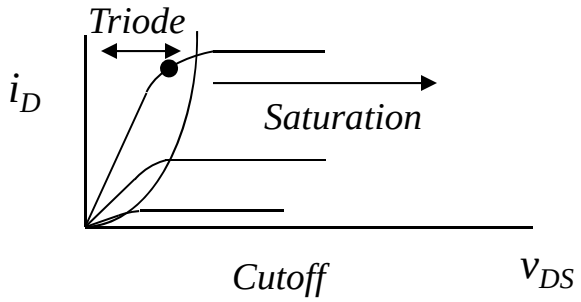


n-channel JFET Operation

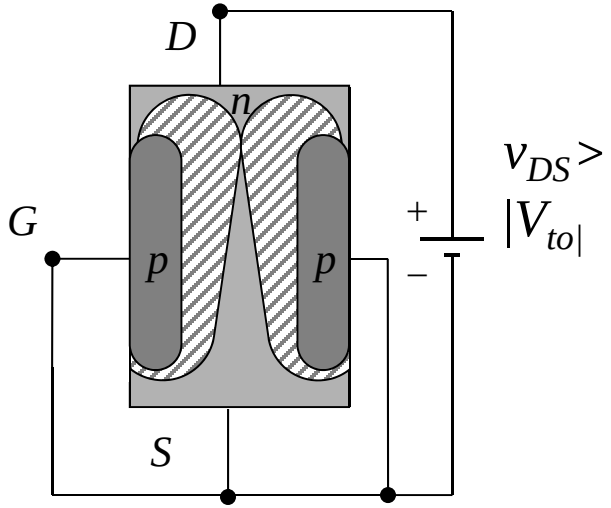


Triode Region

While v_{DS} increases, the depletion region also grows with a larger area at the drain. As a result, the channel resistance increases and increases in I_D are reduced.

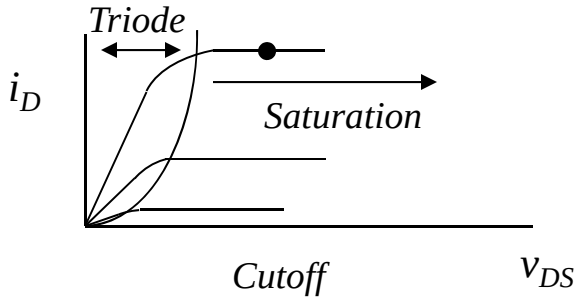


n-channel JFET Operation

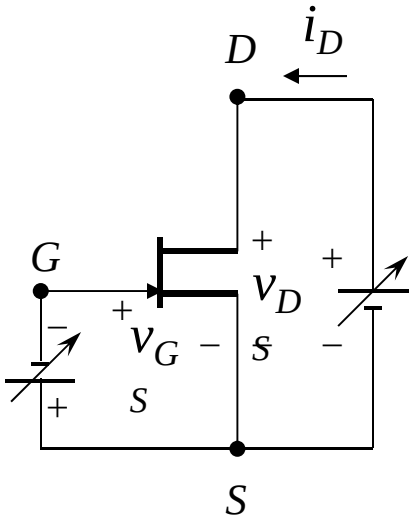


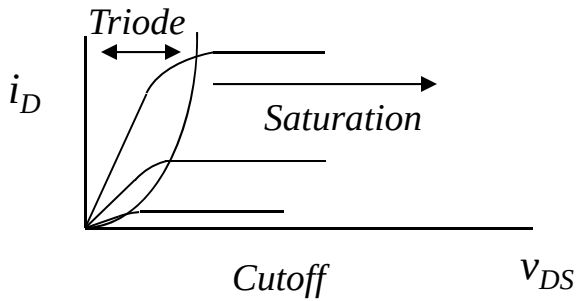
Saturation Region

The depletion region increases as v_{DS} increases. As a result, the depletion region is "pinched off" and I_D does not increase any further (i.e., I_D is saturated).

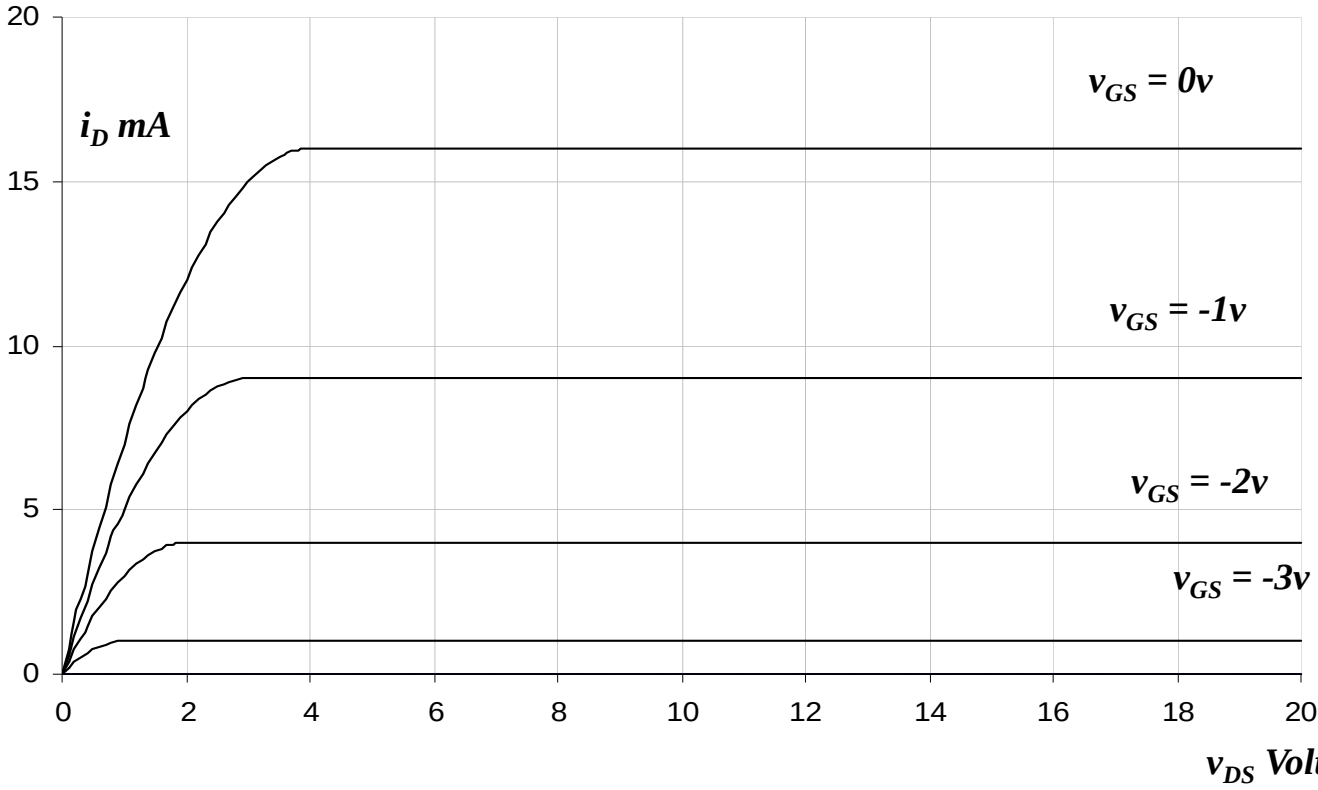


n-channel JFET Operation





JFET Characteristics

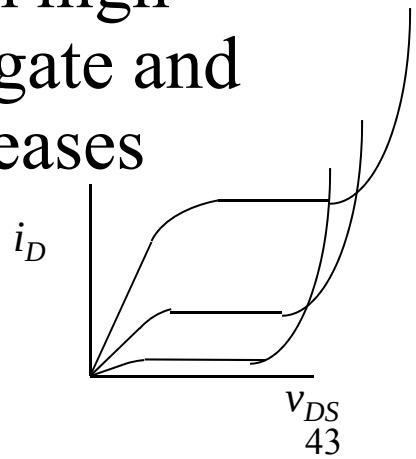


Note that V_{to} = -4

Note that for NMOS devices with short channel lengths, a tilt may exist due to the modulation of the channel length by the depletion region surrounding the drain.

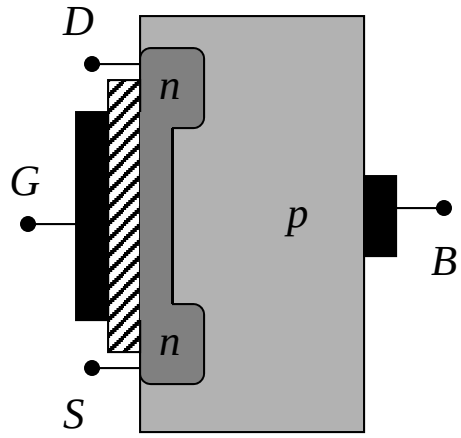
Regions of the JFET

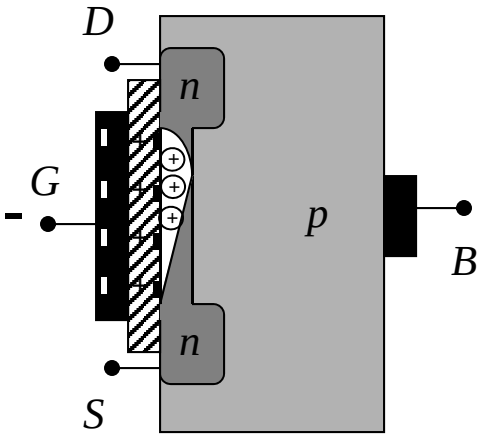
- Cutoff: $v_{GS} < V_{to}$, $i_D = 0$
- Triode: $v_{GS} \geq V_{to}$, $0 \leq v_{DS} < v_{GS} - V_{to}$, $i_D = K[2(v_{GS}-V_{to})v_{DS}-v_{DS}^2]$
- Saturation: $v_{GS} \geq V_{to}$ and $v_{DS} \geq v_{GS} - V_{to}$, $i_D = K(v_{GS}-V_{to})^2$
  - Manufacturer's parameter: Zero-Bias Saturation Current which is the drain current at saturation when $v_{GS} = 0$: $I_{DSS} = KV_{to}^2$
- Breakdown: this region is associated with high values of v_{DS} when the junction between gate and drain breaks down and drain current increases very rapidly.



Other FETs

- **Depletion MOSFET**: similar in characteristics to a JFET but looks like an enhancement mode MOSFET with a channel constructed between drain and source. The difference in operation between this device and a JFET is that, in addition to operating with negative voltages, the gate can be operated with a positive voltage (and run in an enhancement mode).
- ***p*-channel FETs:** for each the FETs we have discussed we can replace the channel with p doped material and the voltage polarities and currents are reversed.
- See Table 5.1 in your text for a summary of the various FET types and their parameters.





Homework

- JFETs
  - Problems: 5.56, 5.57, 5.65