Digital Logic Circuits

Lesson #7
Logic Gate Design Specifications
Section 6.2

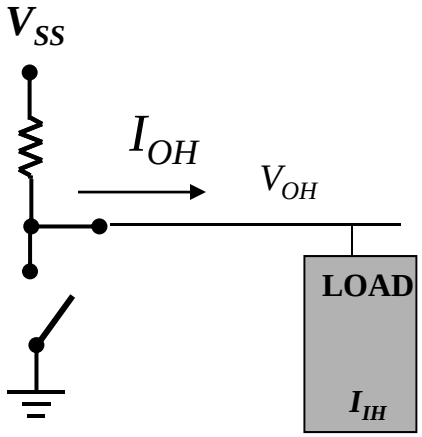
Electrical Specification for Logic Devices (Logic Gates)

- Logic (Voltage) Levels
- Logic Polarity
- Logic Detection
- Noise Margins
- Logic (Current) Levels
- Design Loading
- Power Considerations
  - Static vs. Dynamic
- Propagation Characteristics
  - Rise and Fall Times
  - Delay
- Glitches

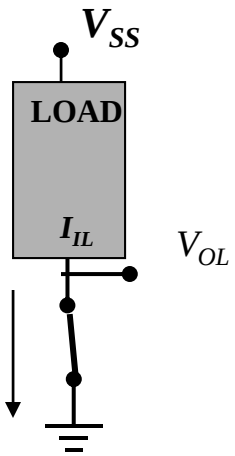
Logic Levels and Polarity

- Logic Ranges
  - For a given logic family, there is a range of output voltage which represents a logic 1 and another range which represents a logic 0
  - Example: TTL
    - Logic 1 can be between 3.0 V and 5.0 V (Switch Open)
    - Logic 0 can be between 0.0 V and 0.5 V (Switch Closed)

- Logic 1: Output High



- Logic 0: Output Low

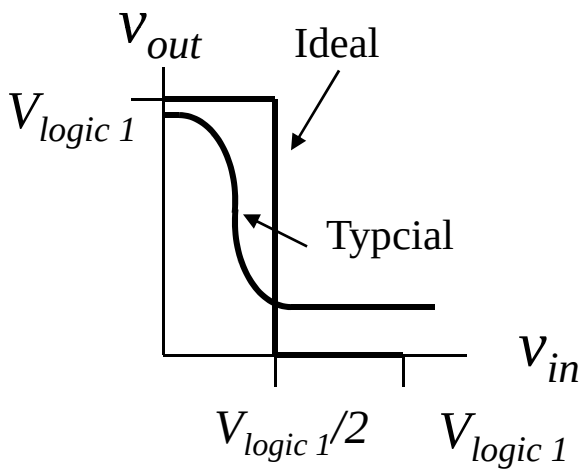


Logic Levels and Polarity

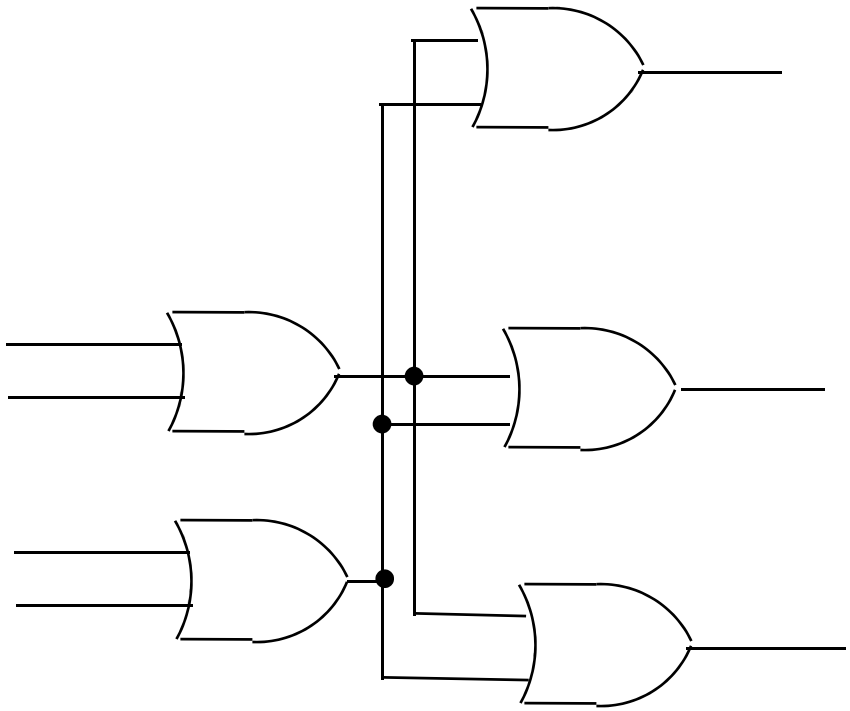
- Polarity of the Logic
  - When logic 1 is associated with a higher amplitude and logic 0 is associated with a lower amplitude, positive logic.
  - When logic 1 is associated with a lower amplitude and logic 0 is associated with a higher amplitude, negative logic.

Device Detection and Noise Margins

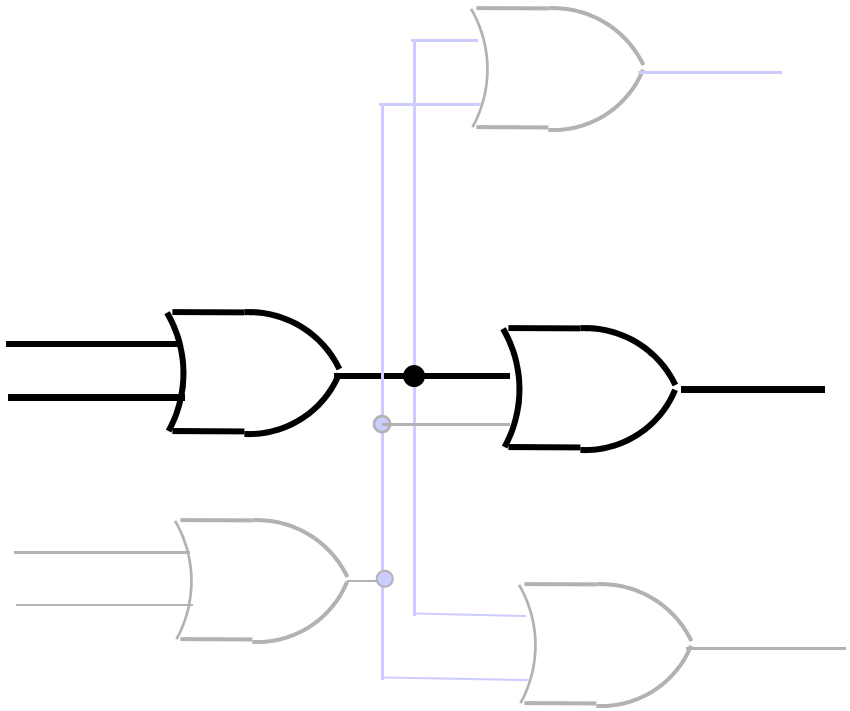
- Transfer characteristics of gates
  - Example: An inverter



Device Detection and Noise Margins

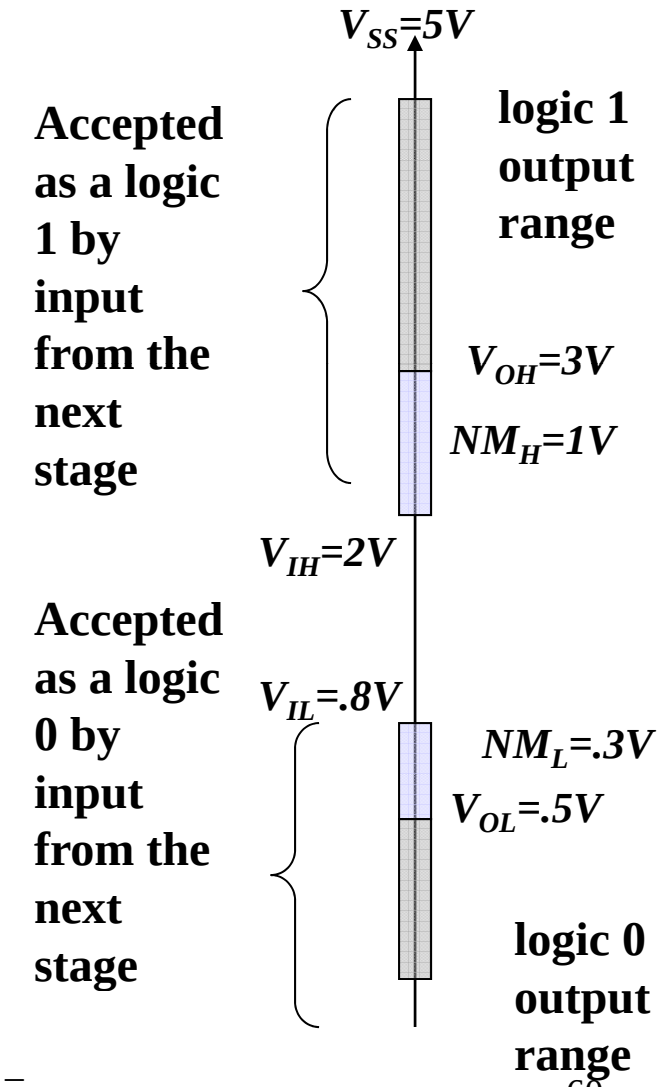


Device Detection and Noise Margins



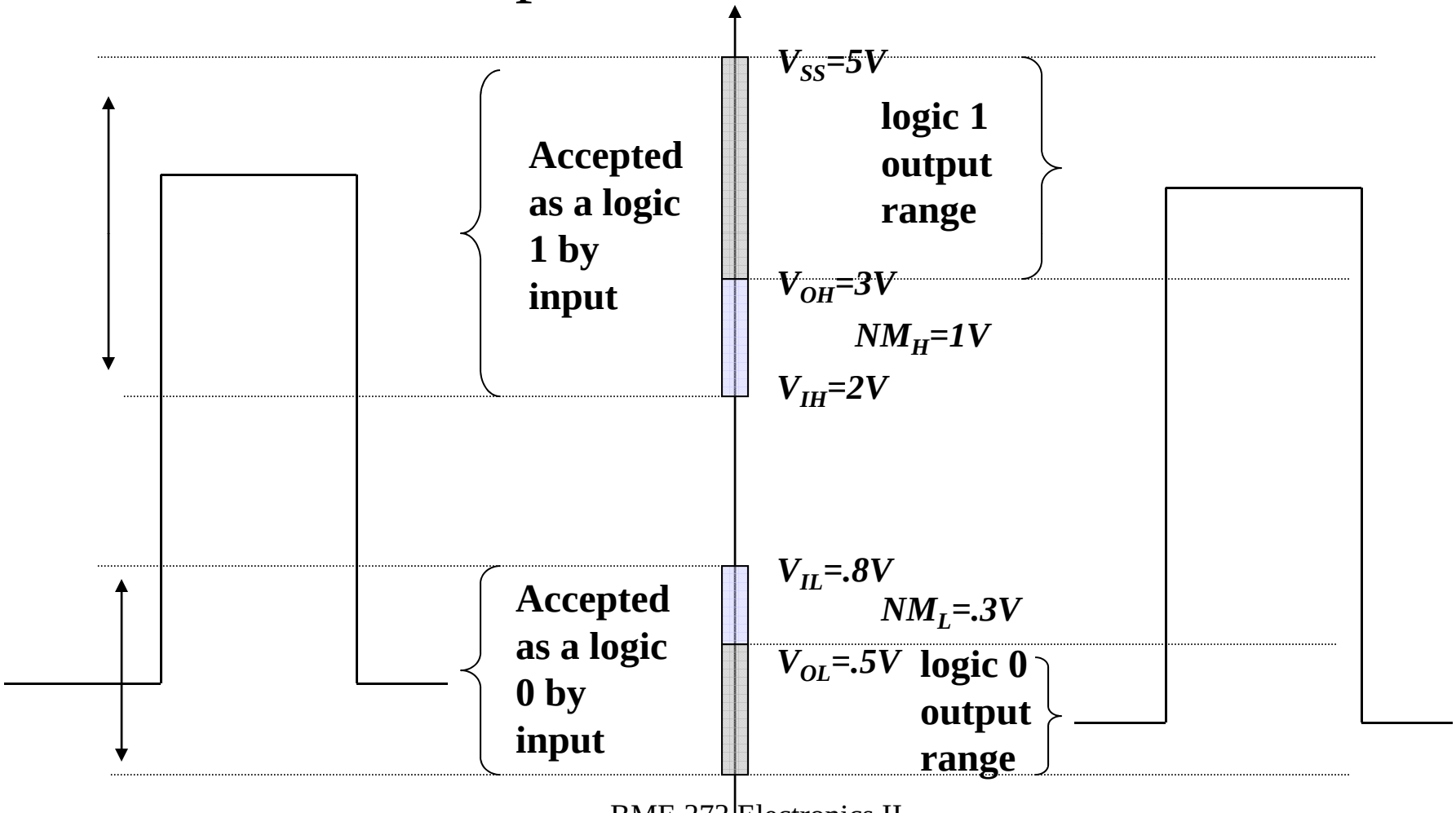
Device Detection and Noise Margins

- Noise Margins
  - To reduce the negative affects of noise which may cause the circuit to falsely report the logic level, the voltage levels of a logic 1 and logic 0 should be as far apart as possible
  - There gates are specified in terms of the following parameters
    - V_{IL} is the highest input to be accepted as a logic 0
    - V_{IH} is the lowest input to be accepted as a logic 1
    - V_{OL} is the highest output produced for a logic 0
    - V_{OH} is the lowest output produced for a logic 1
  - To assure that the downstream gates interrupt the data correctly, we define:
    - a logic 1 noise margin: $NM_H = V_{OH} - V_{IH}$
    - a logic 0 noise margin: $NM_L = V_{1L} - V_{OL}$



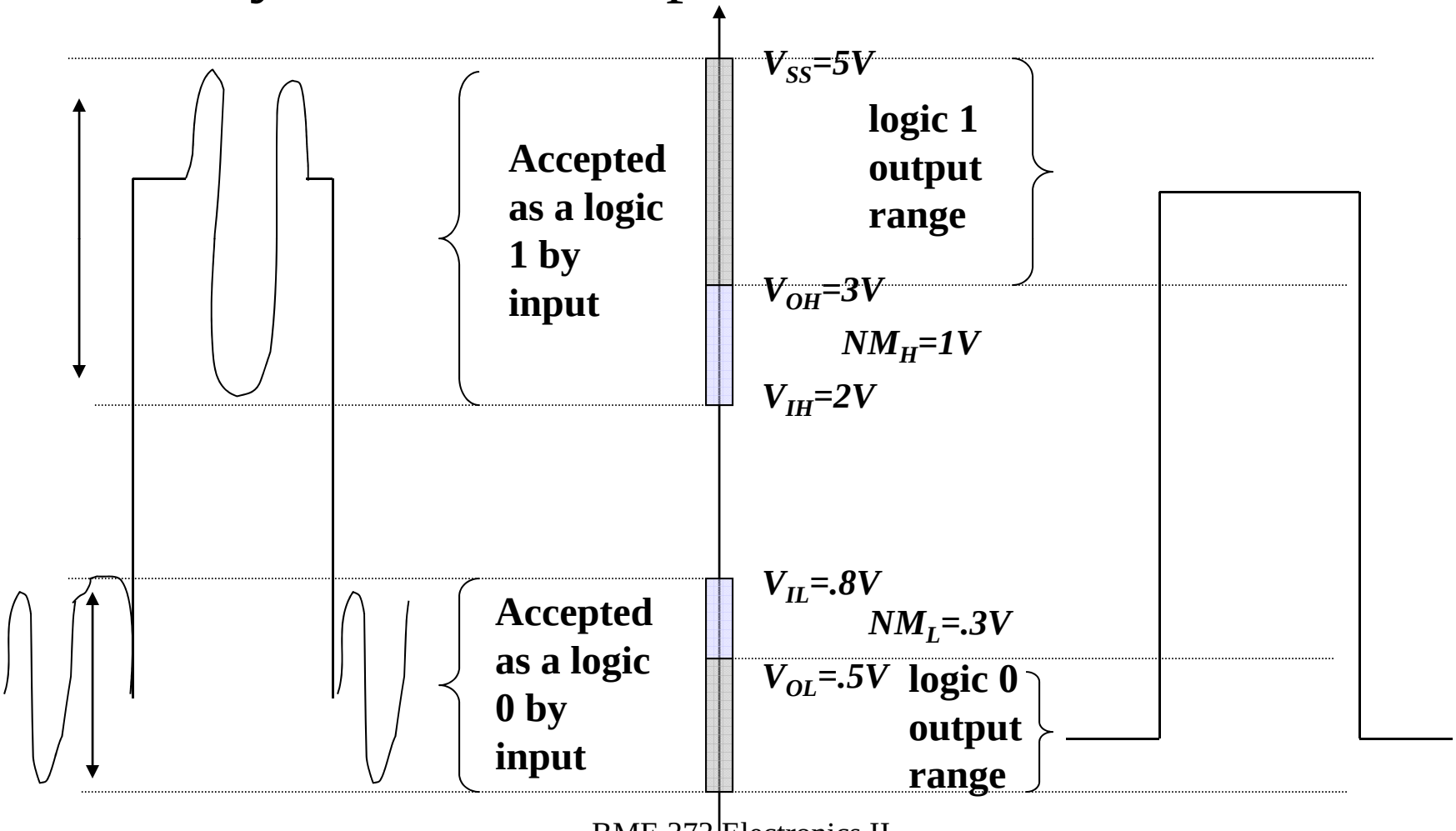
Device Detection and Noise Margins

- Noise Free Operation



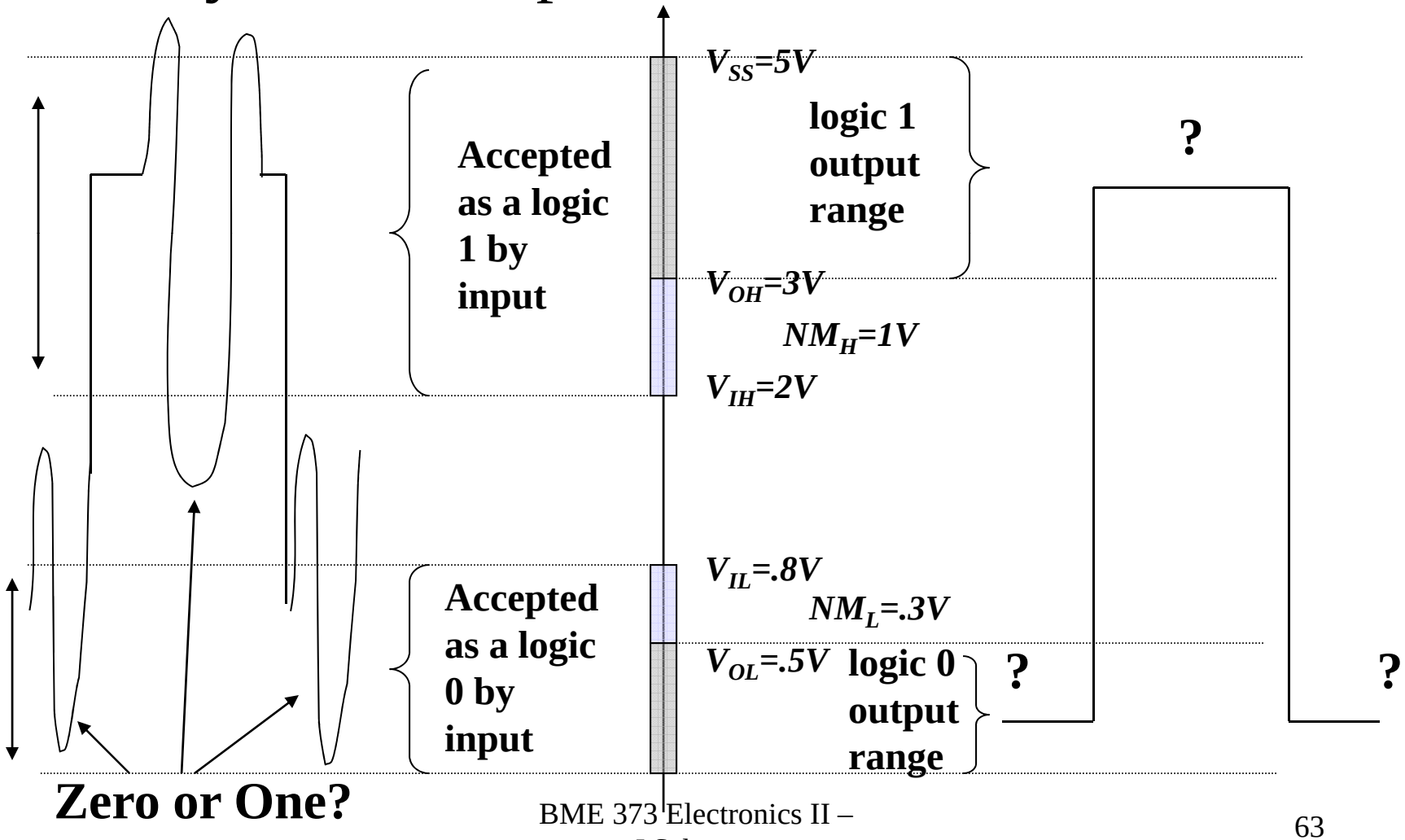
Device Detection and Noise Margins

- Noisy Error Free Operation



Device Detection and Noise Margins

- Noisy Errored Operation

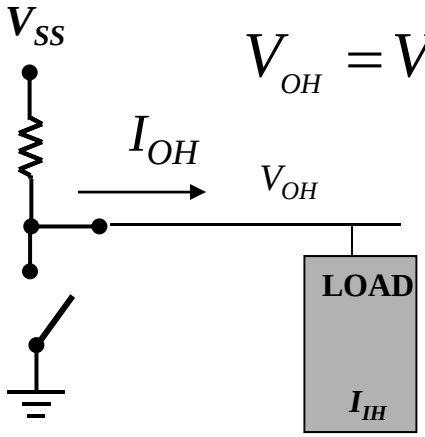


Device Current Levels and Design Loading

- Input Currents
  - The maximum input current to support a logic 0 (1) is I_{IL} (I_{IH})
- Output Currents
  - The output current supplied by the device (sourced) when the output is high is denoted by I_{OH}.
    - If more current is required then the output voltage may fall below V_{OH} due to a larger drop across the output resistance of the device.
  - The output current supported by the device (sinked) when the output is low is denoted by I_{OL}
    - If more current is required then the output voltage may rise above V_{OL} as the operating point moves up the characteristic curves to support the addition current

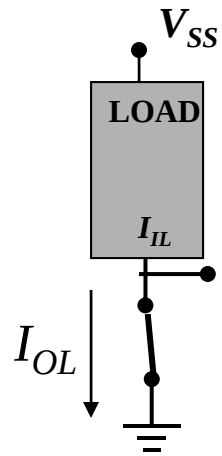
- Sourcing: Output High

$$V_{OH} = V_{SS} - I_{OH} R_D$$

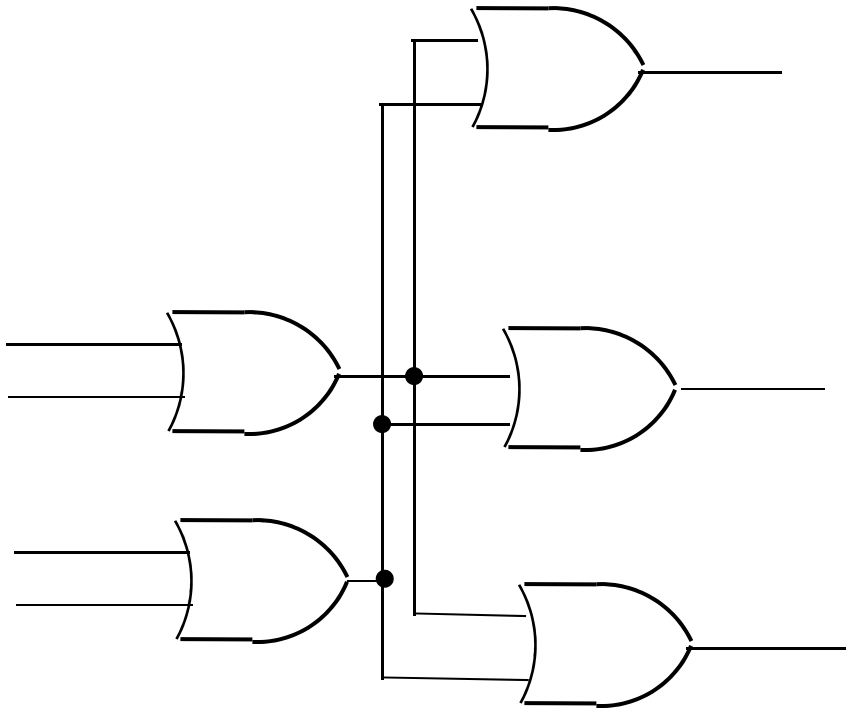


- Sinking: Output Low

$$V_{OL} = I_{OL} Z_{OUT}$$



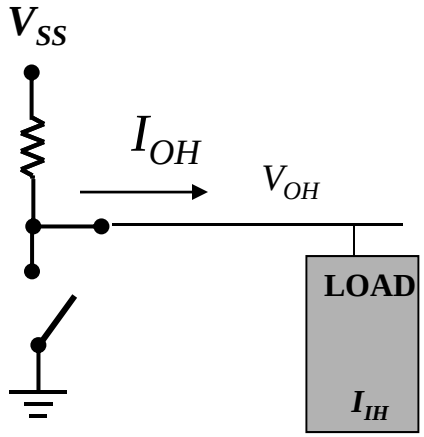
Fan Out



Device Current Levels and Design Loading

- Fan Out
  - Since a device may drive more than one gate, the maximum number of gates which can be driven (fan out) needs to be established and from the current perspective:
    - For a Logic 0 (Low), the fan out should be less than $|I_{OL}/ I_{IL}|$
    - For a Logic 1 (High), the fan out should be less than $|I_{OH}/ I_{IH}|$
    - Maximum fan out is the smaller of these two.
  - In addition, the input of a gate presents a capacitive load to the driving gate. Since we will want these circuits to switch fast then limiting the fan out is required (the larger the capacitive load the slower the switching).

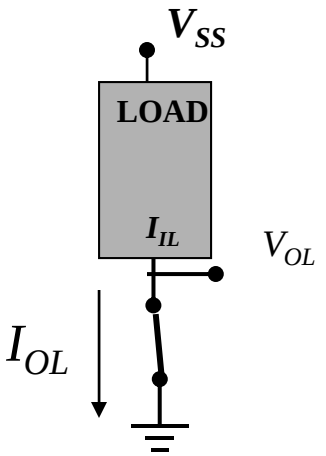
- Sourcing: Output High



N devices

$=I_{OH}/ I_{IH}$

- Sinking: Output Low

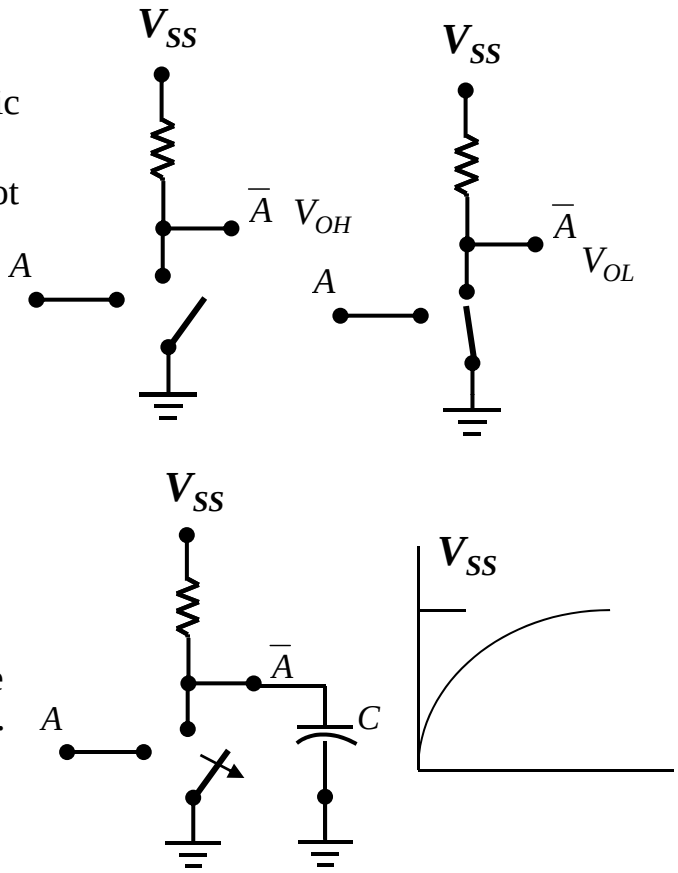


N devices

$=I_{OL}/ I_{IL}$

Device Power Considerations

- Static or Quiescent Power
  - This is power consumed after the device has reached a logic 0 or logic 1.
  - In general, when a device is in a high state, the device is not conducting (i.e., open) and the output is equal to the V_{OH} (i.e., the supply voltage). In this case, no power is consumed.
  - However, when a device is in a low state, the device is conducting (i.e., closed) and the output is equal to the V_{OL}. In this case, there is (static) power being consumed.
  - Therefore, when designed ICs we need to understand the requirements for the power supply and temperature characteristics of the devices.
- Dynamic Power Dissipation
  - Since the fan out load on a gate has a significant capacitive component, a non-zero switching time will be experienced. During this period the device will dissipated power.
  - The power dissipated for a device being switch at a frequency *f* is given below and is highly dependent on *f*.

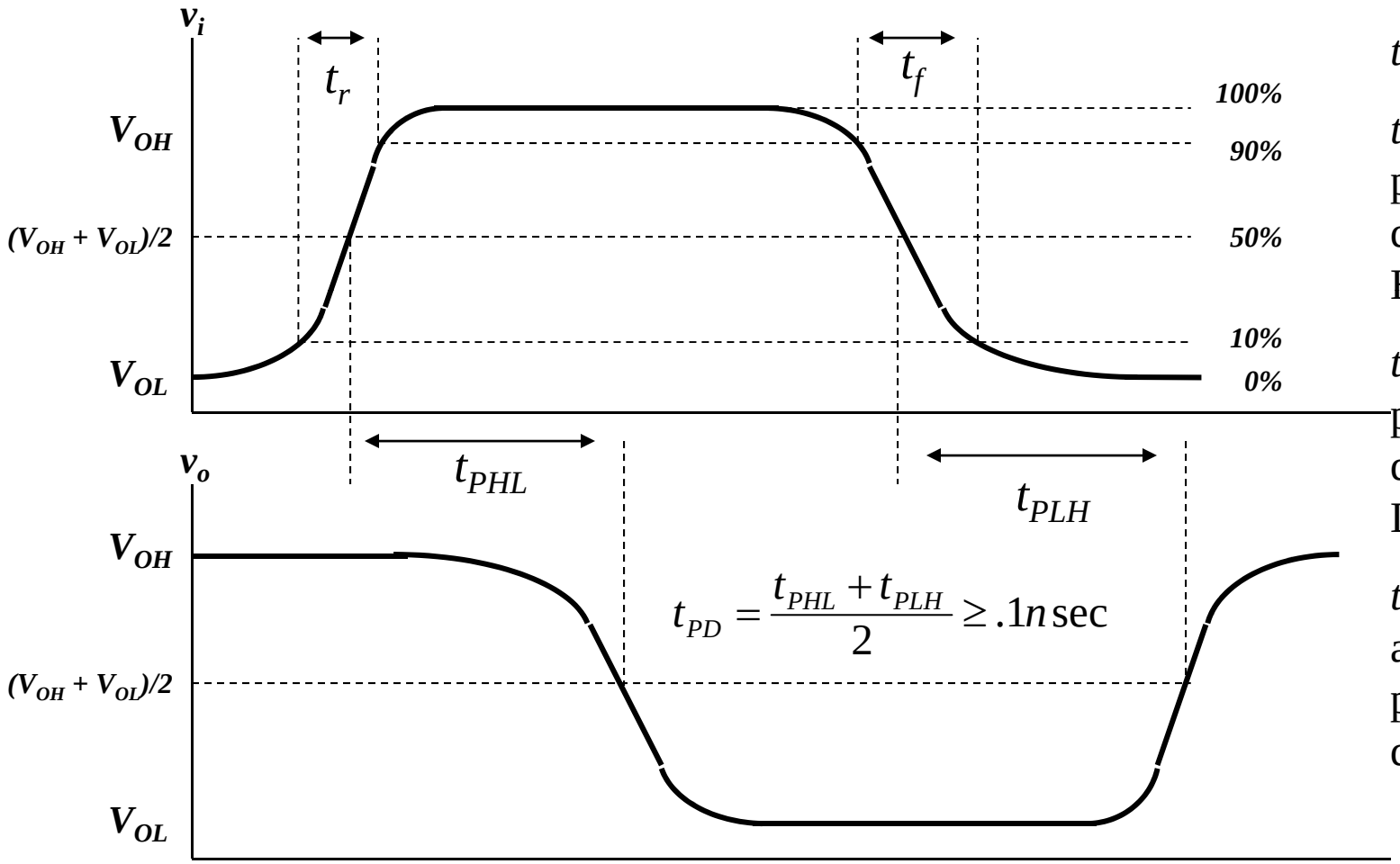


$Q = CV_{SS}$ is the charge on the capacitance when high is reached

$E = QV_{SS} = CV_{SS}^{\ 2}$ is the energy needed to achieve the high state as well as released well switching to the low state

$P = fCV_{SS}^{\ 2}$ is the power dissipated during the switching periods

Propagation Delay



t_r = rise time

t_f = fall time

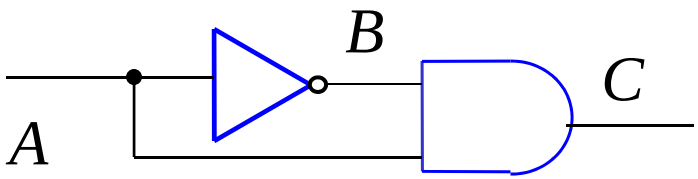
t_{PHL} = propagation delay from High to Low

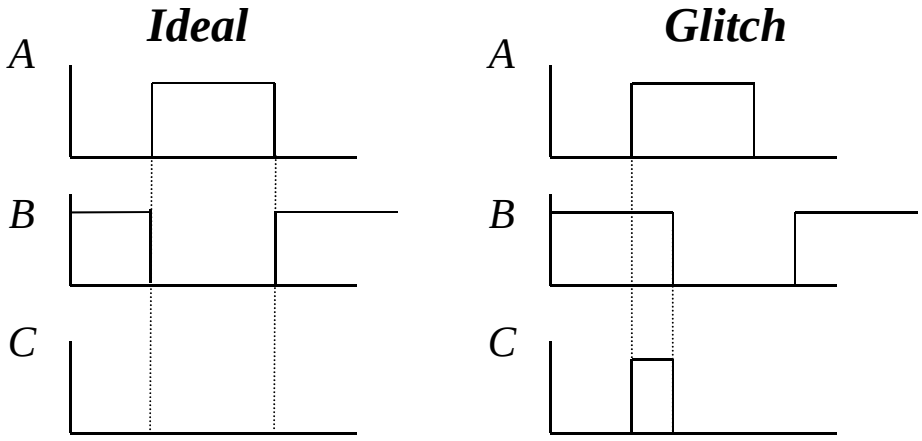
t_{PLH} = propagation delay from Low to High

t_{PD} = average propagation delay

Speed-Power Product and Glitches

- Since we would like to minimize both power and propagation delay, a figure of merit known as the speed-power product which equals product of the power dissipation per gate and propagation delay.
  - Depends on the fan out, capacitive loading and frequency of operation.
- Due to non-zero propagation delay, unusual non-wanted effects (glitches) can occur.





Homework

- Electrical Specs for Logic Gates
  - Problems: 6.12-20