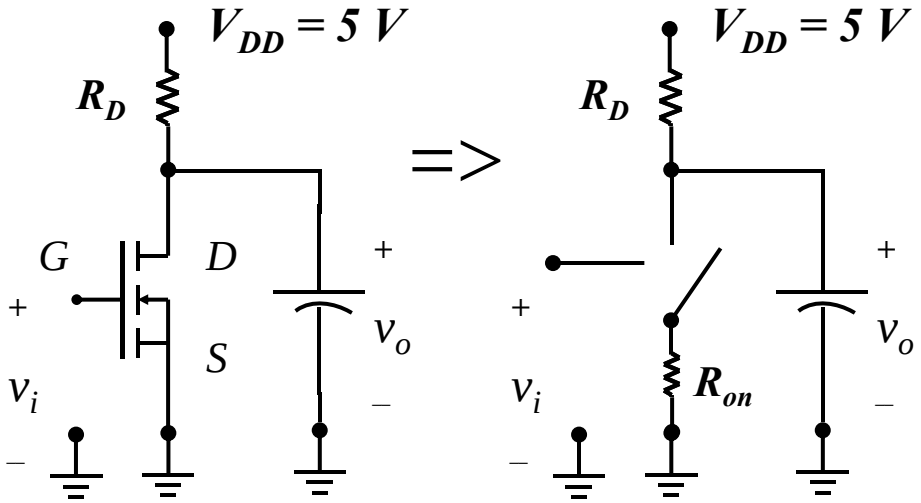
*Digital Logic Circuits*

Lesson #8

FET Gates

Sections 6.3-9

# Resistor-Pull-up NMOS Inverter




Let's find $R_{on}$ and the pull up resistor to make the static power in the low output state to *0.25 mW.* Assume $V_{to}$*=1 V,* $KP=50\mu A/V^2$, $V_{OL}$*=.5 V,* $V_{OH}=V_{DD}=5$ *V*

$$P_{static} = 0.25\times10^{-3} = I_{DS}V_{DD}$$

$$I_{DS} = \frac{0.25\times10^{-3}}{5} = 50\mu A$$

$$I_{DS} = \frac{V_{DD}}{R_{on}+R_D} = \frac{5}{R_{on}+R_D} = 50\mu A$$

$$R_{on}+R_D = \frac{5}{50\times10^{-6}} = 100k\Omega$$

$$R_{on} = \frac{V_{OL}}{V_{DD}}(R_D + R_{on})$$

$$= \frac{.5}{5}100\times10^{3} = 10k\Omega$$

$$K = \frac{1}{2R_{on}(v_i - V_{to})}$$

$$= 12.5\mu A/V^2$$

$$R_D = 90k\Omega$$

Where $R_{on}$ represents the resistance of the NMOS device when the device is on.

$$V_{OH} = V_{DD} = 5V$$

$$V_{OL} = V_{DD}\frac{R_{on}}{R_{on}+R_D}$$

$$v_{GS} = v_i$$

$$v_{DS} = v_o$$

When $v_o$ is close to zero then FET is in the Triode mode, recall:

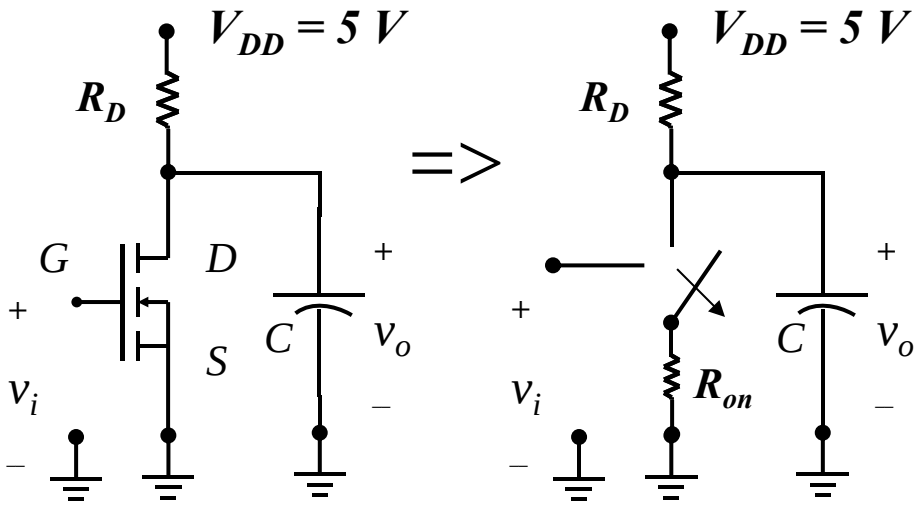
$$i_{DS} = K[2(v_{GS}-V_{to})v_{DS} - v_{DS}^{\ 2}] \approx K[2(v_{GS}-V_{to})v_{DS}]$$

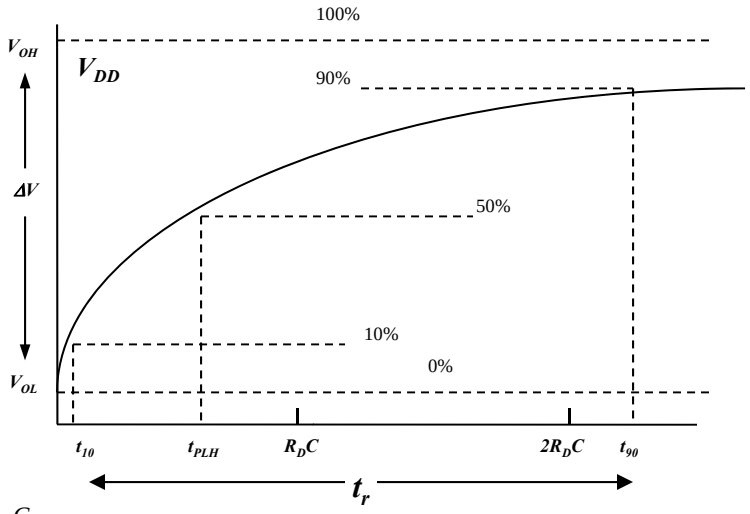
$$K = \left(\frac{W}{L}\right)\frac{KP}{2}$$

$$R_{on} = \frac{v_{DS}}{i_{DS}} = \frac{v_{DS}}{K[2(v_{GS}-V_{to})v_{DS}]} = \frac{1}{K[2(v_{GS}-V_{to})]}$$

To make $R_{on}$ small, we need to design the FET to have a large $K$.

# *Dynamic Response of the Resistor-Pull-up NMOS Inverter Low to High Transition*




$$v_O(t) = V_{OH} - (V_{OH} - V_{OL})e^{-t/R_DC} = V_{OH} - \Delta V e^{-t/R_DC}$$

$$v_O(t_{10}) = V_{OL} + .1\Delta V = V_{OH} - \Delta V e^{-t_{10}/R_DC}$$

$$V_{OL} - V_{OH} + .1\Delta V = .1\Delta V - \Delta V = -.9\Delta V = -\Delta V e^{-t_{10}/R_DC}$$

$$t_{10} = -R_DC\ln(.9) = .1054R_DC$$

$$t_{90} = -R_DC\ln(.1) = 2.3025R_DC$$

$$t_r = 2.2R_DC$$

$$t_{PLH} = -R_DC\ln(.5) = 0.6931R_DC$$

The $R_DC$ time constant determines the parameters associated with the transition from Low to High, e.g. the rise time.

We then say that the capacitor charges to $V_{OH}$ through the pull up resistor $R_D$

# *Calculation of $v_o(t)$*

Using Kirchoff's Current Law at the output node, $v_o(t)$:

$$C\frac{dv_o(t)}{dt}+0=\frac{V_{DD}-v_o(t)}{R}$$

$$C\frac{dv_o(t)}{dt}+\frac{v_o(t)}{R}=\frac{V_{DD}}{R}=\frac{V_{OH}}{R}$$

Let's assume:

$$v_o(t)=A_1e^{-\alpha t}+A_2$$

$$\therefore \dot{v}_o(t)=-\alpha A_1e^{-\alpha t}$$

$$-\alpha A_1e^{-\alpha t}C+\frac{A_1e^{-\alpha t}+A_2}{R}=\frac{V_{OH}}{R}$$

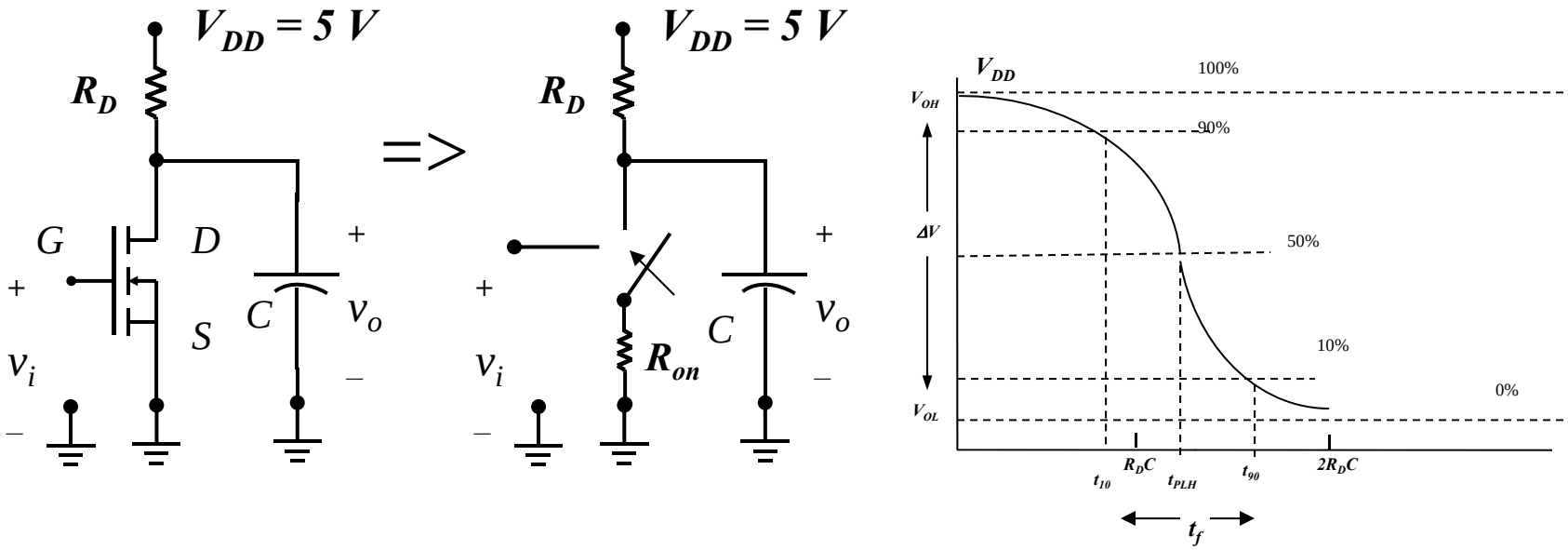
$$\therefore \alpha=\frac{1}{RC};A_2=V_{OH}$$

Since $v_o(0)=V_{OL}$

$$v_o(0)=A_1+V_{OH}=V_{OL};A_1=-(V_{OH}-V_{OL})$$

$$v_o(t)=-(V_{OH}-V_{OL})e^{-t/RC}+V_{OH}$$

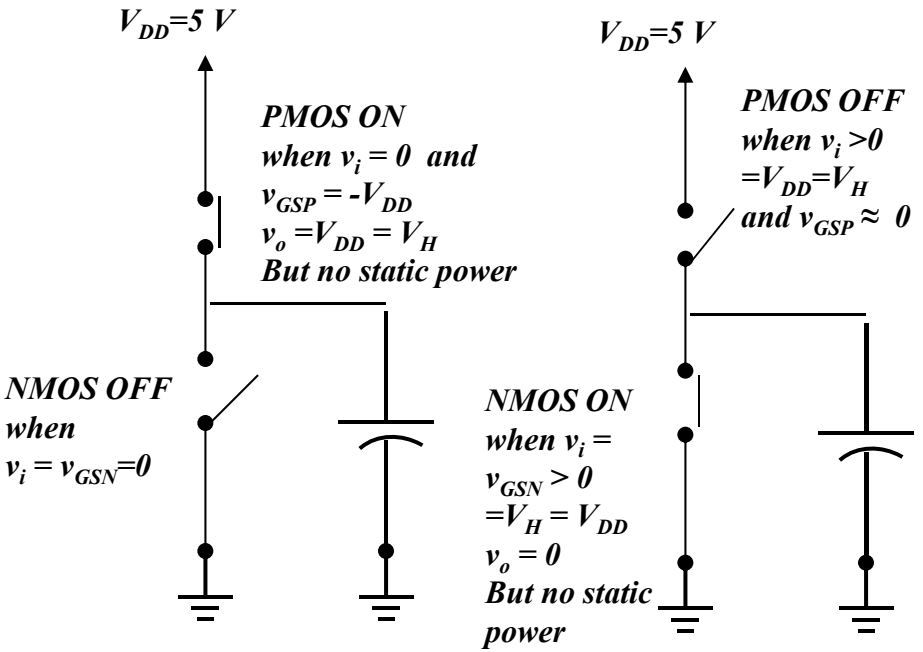
# *Dynamic Response of the Resistor-Pull-up NMOS Inverter High to Low Transition*

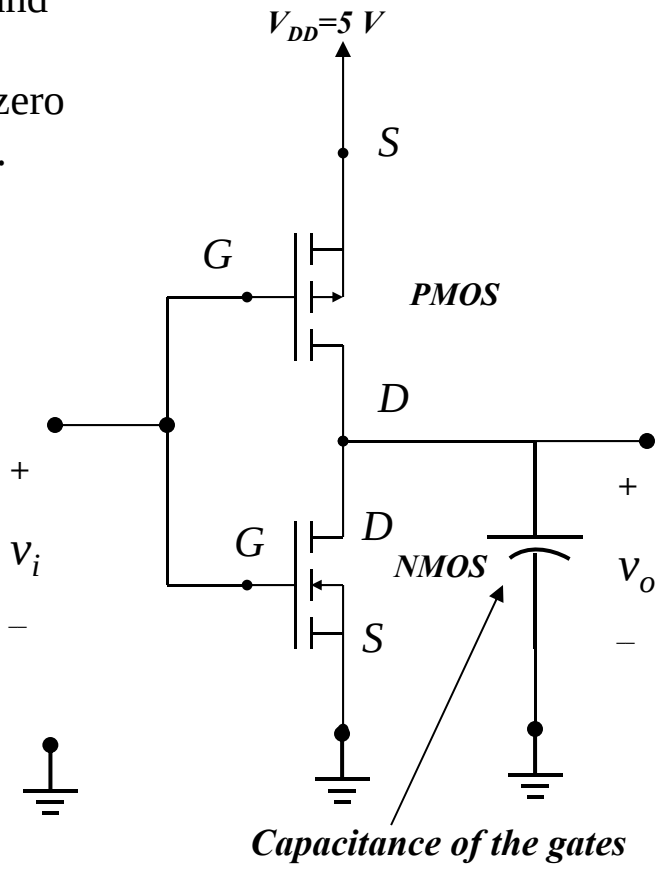



In this case, the capacitor discharges through the parallel combination of $R_D$ and $R_{on}$. However, since $R_{on} < R_D$, the fall time from High to Low is usually shorter than the rise time from Low to High. In our example, $R_D = 90k$ and $R_{on} = 10k$ and the time constant for Low to High = 10kC while the time constant for High to Low is 9KC which yields 10% faster fall time than rise time. However, the overall performance is governed by the slowest time.

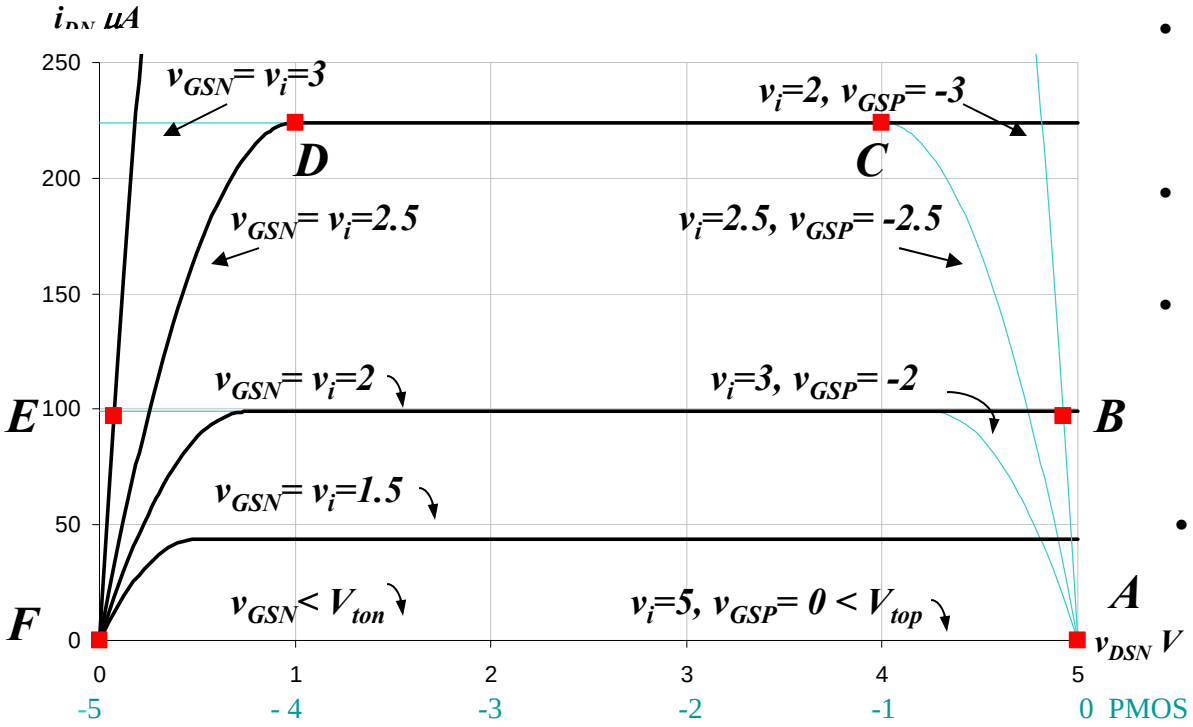
# *Complementary MOS CMOS*

- Taking NMOS (*n*-channel) and PMOS (*p*-channel) and using them in a complementary fashion (same characteristics) such that the static power is always zero (there will, of course, be dynamic power dissipated).
- Note that $V_{GSP} = v_i - V_{DD}$ and $V_{GSN} = v_i$



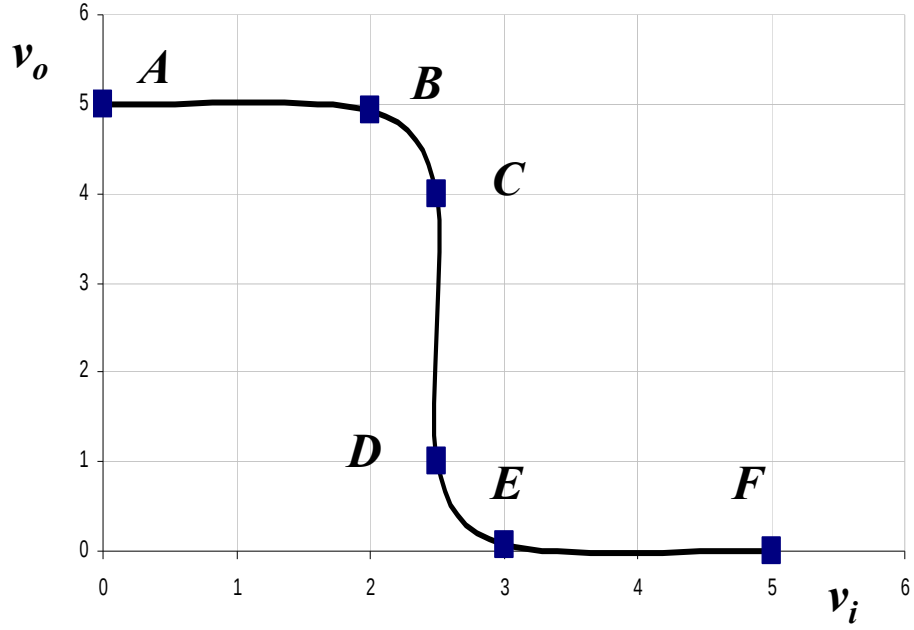
# *Graphical Analysis*



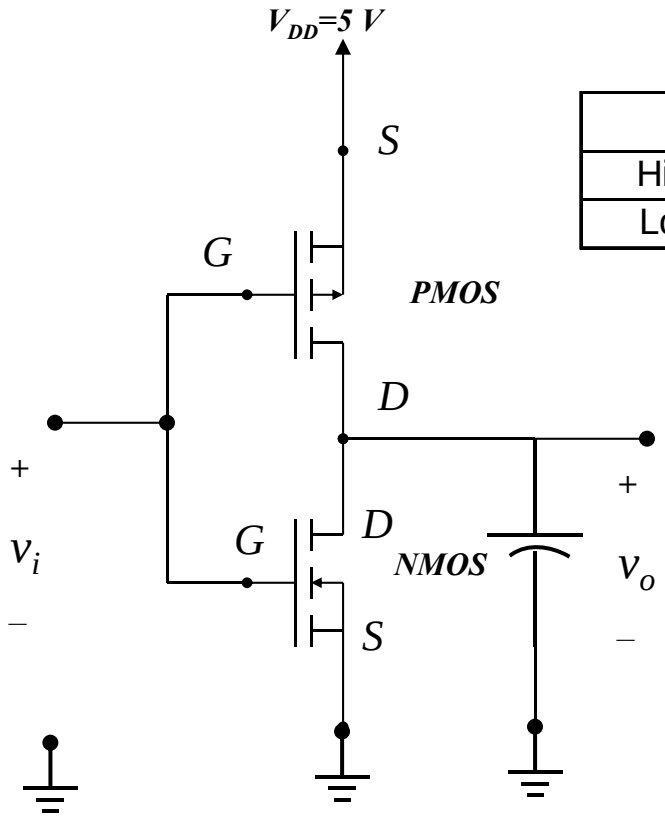

- For CMOS, the load line of the NMOS is the characteristic curves of the PMOS.
- Let view the operation as $v_i$ goes from *0* to *5 V*
- Point A: $v_i$=*0*, the NMOS is cutoff since $v_i = v_{GSN} < V_{ton}$; the PMOS is conducting since $v_{GSP} = v_i - V_{DD} = -V_{DD}$
- Point B: $v_i$=*2* and is the intersection of $v_{GSN}$ = *2* and $v_{GSP}$ = **-3** where the NMOS is in saturation and the PMOS is in the triode region.
- Points C through D: $v_i$=*2.5* and is the intersection of $v_{GSN}$ = *2.5* and $v_{GSP}$ = **-3** where the NMOS and the PMOS are both in saturation.
- Point E $v_i$=*3* and is the intersection of $v_{GSN}$ = *3* and $v_{GSP}$ = **-2** where the NMOS is in the triode region and the PMOS is in the saturation region.
- Point F: $v_i$=*5*, the NMOS is conducting but the PMOS is cutoff since $v_{GSP} < V_{top} = v_i - V_{DD} = 0$

# *Transfer Characteristics*

- These characteristics approach the ideal characteristics we discuss previously.
- For $v_i < V_{ton}$, $v_o = V_{DD}$
- For $v_i > V_{DD} - |V_{top}|$, $v_o = 0$
- The transfer characteristics fall abruptly at $v_i = V_{DD}/2$

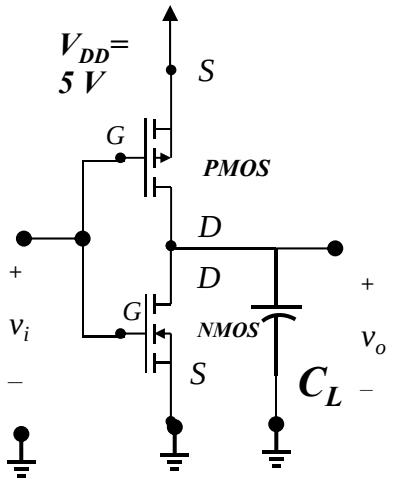


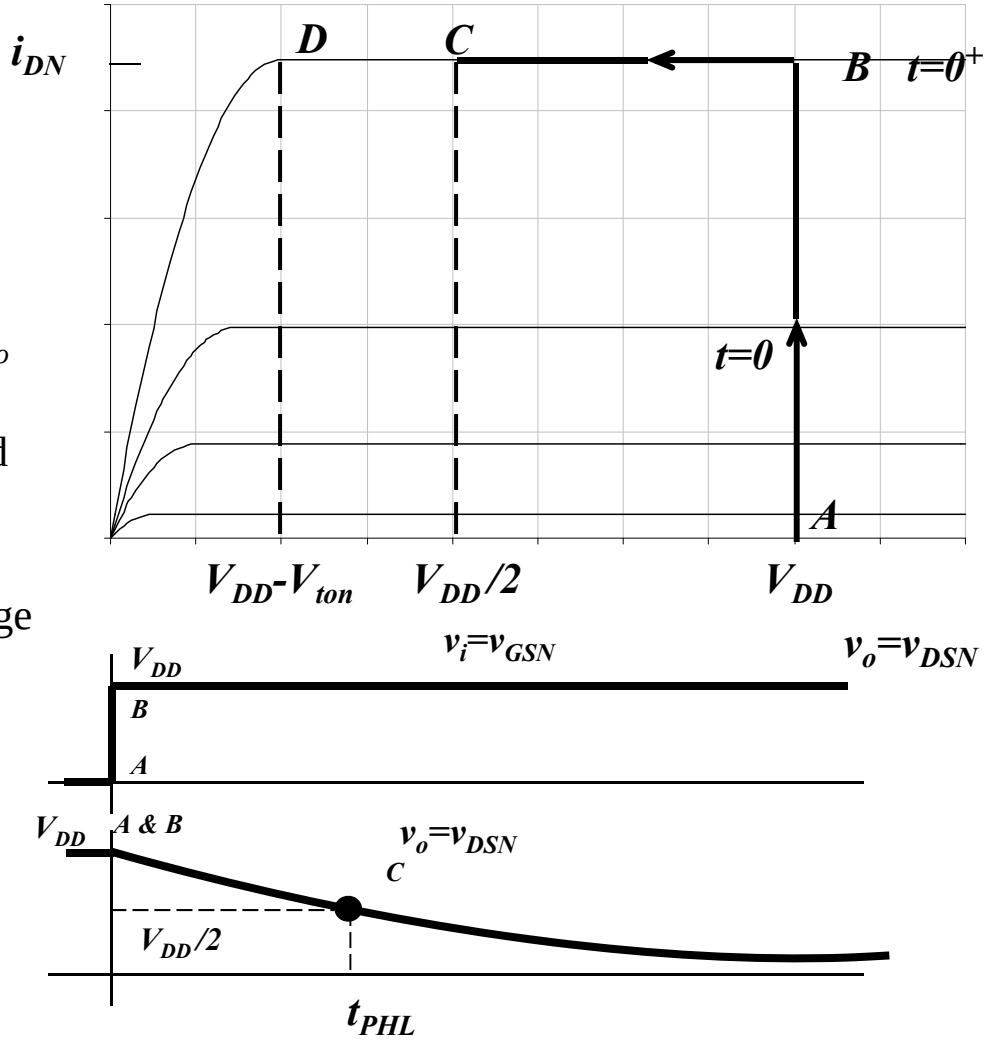
# *CMOS Inverter Truth Table*




| $v_i$ | | NMOS | PMOS | $v_o$ | |
|---|---|---|---|---|---|
| High | 1 | ON | OFF | Low | 0 |
| Low | 0 | OFF | ON | High | 1 |

# Propagation Delay




- At *t=0-* (just before the switch, $v_i = 0$ and $v_o = V_{DD}$. (Point A)
- At *t=0*, $v_i$ switches from LOW to HIGH and the NMOS goes ON and the PMOS goes OFF. (Transition from Point A to B)
- Because the voltage across $C_L$ can not change instantly, at $t=0+$ $v_o=V_{DD}$ and $C_L$ *begins to* discharge through the NMOS at

$$i_{DN} = \left(\frac{W}{L}\right)\frac{KP_n}{2}(V_{DD} - V_{ton})^2$$

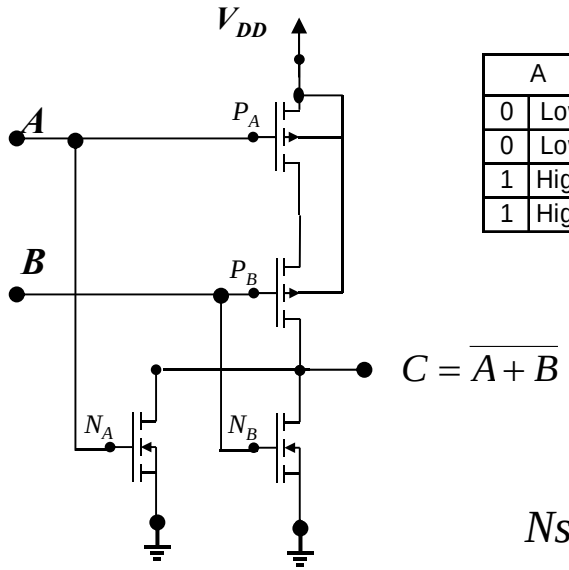
- Assuming that $V_{DD}/2$, the $t_{PHL}$ point, then

$$t_{PHL} \approx \frac{C_L \Delta V}{i_{DN}} = \frac{C_L (V_{DD}/2)}{(W/L)_n (KP_n/2)(V_{DD} - V_{ton})^2}$$

$$t_{PLH} = \frac{C_L (V_{DD}/2)}{(W/L)_p (KP_p/2)(V_{DD} - |V_{top}|)^2}$$

# *CMOS NOR and NAND GATES*

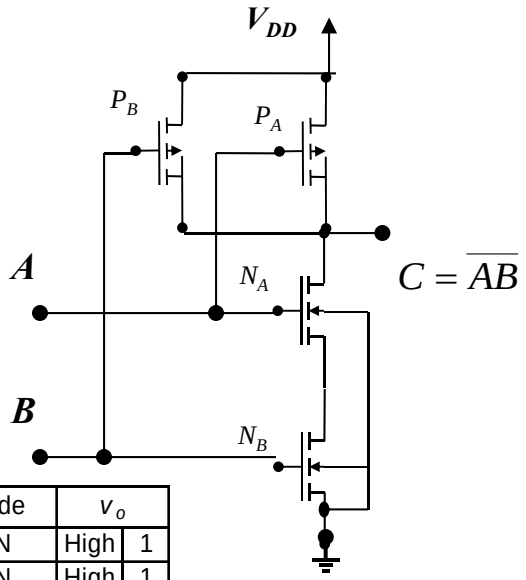
## NOR Gate




| A | | B | | NA | PA | NB | PB | Nside | Pside | $v_o$ | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | Low | 0 | Low | OFF | ON | OFF | ON | OFF | ON | High | 1 |
| 0 | Low | 1 | High | OFF | ON | ON | OFF | ON | OFF | Low | 0 |
| 1 | High | 0 | Low | ON | OFF | OFF | ON | ON | OFF | Low | 0 |
| 1 | High | 1 | High | ON | OFF | ON | OFF | ON | OFF | Low | 0 |

$$Nside = NA + NB$$

$$Pside = PA \bullet PB$$




$$Nside = NA \bullet NB$$

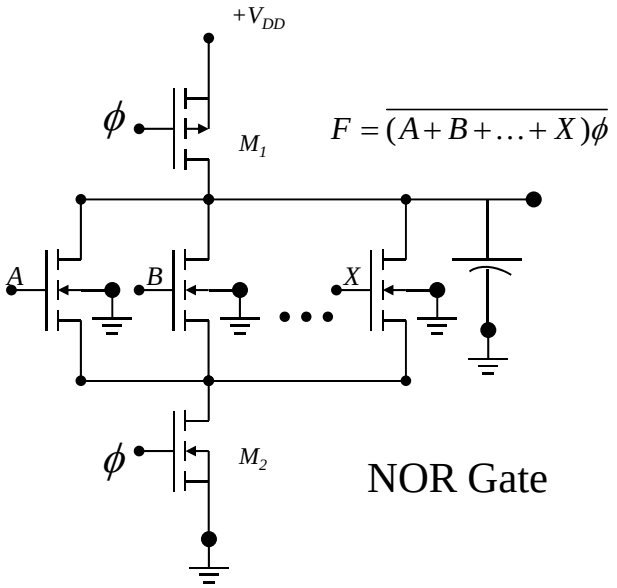
$$Pside = PA + PB$$

## NAND Gate

| A | | B | | NA | PA | NB | PB | Nside | Pside | $v_o$ | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | Low | 0 | Low | OFF | ON | OFF | ON | OFF | ON | High | 1 |
| 0 | Low | 1 | High | OFF | ON | ON | OFF | OFF | ON | High | 1 |
| 1 | High | 0 | Low | ON | OFF | OFF | ON | OFF | ON | High | 1 |
| 1 | High | 1 | High | ON | OFF | ON | OFF | ON | OFF | Low | 0 |

# *Dynamic Logic*

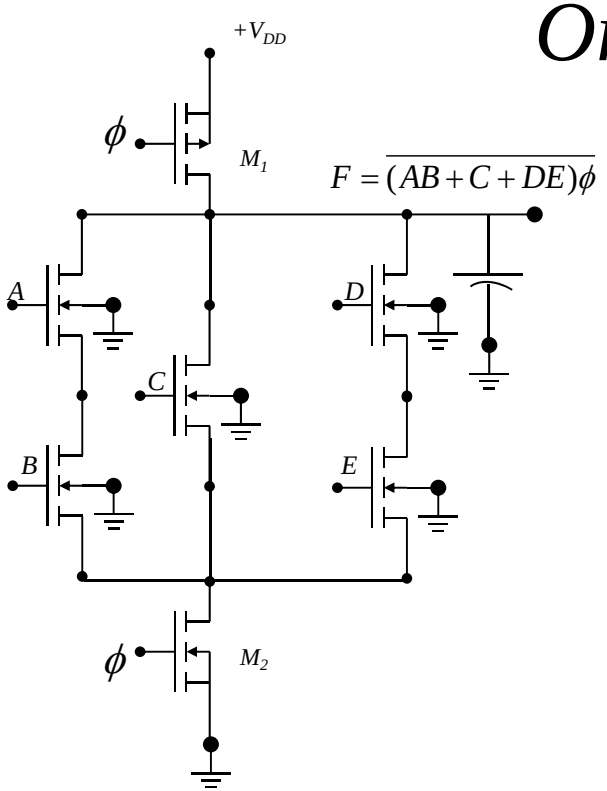
- In this circuit, only when the clock, $\phi$, is high will the output be dependent on the inputs, *A*, *B*, …*X*.
- When $\phi$ is low, M1 is ON, M2 is OFF and capacitor will be charged to VDD.
- When $\phi$ is high, M1 is OFF, M2 is ON, and the capacitor will discharge through the NMOS transistors provided that at least on of the inputs is ON.




NOR Gate

| A | | B | | X | | φ | | NA | NB | NX | Nφ | Pφ | Nside | Pside | $v_o$ | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | Low | 0 | Low | 0 | Low | 0 | Low | OFF | OFF | OFF | OFF | ON | OFF | ON | High | 1 |
| 0 | Low | 0 | Low | 1 | High | 0 | Low | OFF | OFF | ON | OFF | ON | OFF | ON | High | 1 |
| 0 | Low | 1 | High | 0 | Low | 0 | Low | OFF | ON | OFF | OFF | ON | OFF | ON | High | 1 |
| 0 | Low | 1 | High | 1 | High | 0 | Low | OFF | ON | ON | OFF | ON | OFF | ON | High | 1 |
| 1 | High | 0 | Low | 0 | Low | 0 | Low | ON | OFF | OFF | OFF | ON | OFF | ON | High | 1 |
| 1 | High | 0 | Low | 1 | High | 0 | Low | ON | OFF | ON | OFF | ON | OFF | ON | High | 1 |
| 1 | High | 1 | High | 0 | Low | 0 | Low | ON | ON | OFF | OFF | ON | OFF | ON | High | 1 |
| 1 | High | 1 | High | 1 | High | 0 | Low | ON | ON | ON | OFF | ON | OFF | ON | High | 1 |
| 0 | Low | 0 | Low | 0 | Low | 1 | High | OFF | OFF | OFF | ON | OFF | OFF | OFF | High | 1 |
| 0 | Low | 0 | Low | 1 | High | 1 | High | OFF | OFF | ON | ON | OFF | ON | OFF | Low | 0 |
| 0 | Low | 1 | High | 0 | Low | 1 | High | OFF | ON | OFF | ON | OFF | ON | OFF | Low | 0 |
| 0 | Low | 1 | High | 1 | High | 1 | High | OFF | ON | ON | ON | OFF | ON | OFF | Low | 0 |
| 1 | High | 0 | Low | 0 | Low | 1 | High | ON | OFF | OFF | ON | OFF | ON | OFF | Low | 0 |
| 1 | High | 0 | Low | 1 | High | 1 | High | ON | OFF | ON | ON | OFF | ON | OFF | Low | 0 |
| 1 | High | 1 | High | 0 | Low | 1 | High | ON | ON | OFF | ON | OFF | ON | OFF | Low | 0 |
| 1 | High | 1 | High | 1 | High | 1 | High | ON | ON | ON | ON | OFF | ON | OFF | Low | 0 |

# *One More Example*




- Using this design, we can design other logic functions.

| | | | | | | | | A | B | C | D | E | P | N | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $\phi$ | A | B | C | D | E | M2 | M1 | NA | NB | NC | NC | NE | (NA*NB+NC+ND*NE)M2 | M1 | F | |
| 1 | 0 | 0 | 0 | 0 | 0 | ON | OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF | ON | 1 |
| 1 | 0 | 0 | 0 | 0 | 1 | ON | OFF | OFF | OFF | OFF | OFF | ON | OFF | OFF | ON | 1 |
| 1 | 0 | 0 | 0 | 1 | 0 | ON | OFF | OFF | OFF | OFF | OFF | ON | OFF | OFF | ON | 1 |
| 1 | 0 | 0 | 0 | 1 | 1 | ON | OFF | OFF | OFF | OFF | OFF | ON | ON | OFF | OFF | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 | ON | OFF | OFF | OFF | OFF | ON | OFF | OFF | ON | OFF | 0 |
| 1 | 0 | 0 | 1 | 0 | 1 | ON | OFF | OFF | OFF | OFF | ON | OFF | ON | ON | OFF | 0 |
| 1 | 0 | 0 | 1 | 1 | 0 | ON | OFF | OFF | OFF | OFF | ON | ON | OFF | ON | OFF | 0 |
| 1 | 0 | 0 | 1 | 1 | 1 | ON | OFF | OFF | OFF | OFF | ON | ON | ON | ON | OFF | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 | ON | OFF | OFF | ON | OFF | OFF | OFF | OFF | OFF | ON | 1 |
| 1 | 0 | 1 | 0 | 0 | 1 | ON | OFF | OFF | ON | OFF | OFF | ON | OFF | OFF | ON | 1 |
| 1 | 0 | 1 | 0 | 1 | 0 | ON | OFF | OFF | ON | OFF | ON | OFF | OFF | OFF | ON | 1 |
| 1 | 0 | 1 | 0 | 1 | 1 | ON | OFF | OFF | ON | OFF | ON | ON | ON | OFF | OFF | 0 |
| 1 | 0 | 1 | 1 | 0 | 0 | ON | OFF | OFF | ON | ON | OFF | OFF | ON | OFF | OFF | 0 |
| 1 | 0 | 1 | 1 | 0 | 1 | ON | OFF | OFF | ON | ON | OFF | ON | ON | OFF | OFF | 0 |
| 1 | 0 | 1 | 1 | 1 | 0 | ON | OFF | OFF | ON | ON | ON | OFF | ON | OFF | OFF | 0 |
| 1 | 0 | 1 | 1 | 1 | 1 | ON | OFF | OFF | ON | ON | ON | ON | ON | OFF | OFF | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | ON | OFF | ON | OFF | OFF | OFF | OFF | OFF | OFF | ON | 1 |
| 1 | 1 | 0 | 0 | 0 | 1 | ON | OFF | ON | OFF | OFF | OFF | ON | OFF | OFF | ON | 1 |
| 1 | 1 | 0 | 0 | 1 | 0 | ON | OFF | ON | OFF | OFF | ON | OFF | OFF | OFF | ON | 1 |
| 1 | 1 | 0 | 0 | 1 | 1 | ON | OFF | ON | OFF | OFF | ON | ON | ON | OFF | OFF | 0 |
| 1 | 1 | 0 | 1 | 0 | 0 | ON | OFF | ON | OFF | ON | OFF | OFF | ON | OFF | OFF | 0 |
| 1 | 1 | 0 | 1 | 0 | 1 | ON | OFF | ON | OFF | ON | OFF | ON | ON | OFF | OFF | 0 |
| 1 | 1 | 0 | 1 | 1 | 0 | ON | OFF | ON | OFF | ON | ON | OFF | ON | OFF | OFF | 0 |
| 1 | 1 | 0 | 1 | 1 | 1 | ON | OFF | ON | OFF | ON | ON | ON | ON | OFF | OFF | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 | ON | OFF | ON | ON | OFF | OFF | OFF | ON | OFF | OFF | 0 |
| 1 | 1 | 1 | 0 | 0 | 1 | ON | OFF | ON | ON | OFF | OFF | ON | ON | OFF | OFF | 0 |
| 1 | 1 | 1 | 0 | 1 | 0 | ON | OFF | ON | ON | OFF | ON | OFF | ON | OFF | OFF | 0 |
| 1 | 1 | 1 | 0 | 1 | 1 | ON | OFF | ON | ON | OFF | ON | ON | ON | OFF | OFF | 0 |
| 1 | 1 | 1 | 1 | 0 | 0 | ON | OFF | ON | ON | ON | OFF | OFF | ON | OFF | OFF | 0 |
| 1 | 1 | 1 | 1 | 0 | 1 | ON | OFF | ON | ON | ON | OFF | ON | ON | OFF | OFF | 0 |
| 1 | 1 | 1 | 1 | 1 | 0 | ON | OFF | ON | ON | ON | ON | OFF | ON | OFF | OFF | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | ON | OFF | ON | ON | ON | ON | ON | ON | OFF | OFF | 0 |

# *Homework*

- Resistor-Pull-Up NMOS Inverter
  - Problem: 6.32
- Dynamic Response
  - Problem: 6.40
- CMOS Inverter
  - Problems: 6.48-6.50
- Propagation Delay
  - Problem: 6.58
- CMOS Gates
  - Problems: 6.69-6.70, 6.71-73