ASIC for SDD-Based X-Ray Spectrometers

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***Abstract*—We present an application-specific integrated circuit (ASIC) for high-resolution x-ray spectrometers (XRS). The ASIC reads out signals from pixelated silicon drift detectors (SDDs). The pixel does not have an integrated field effect transistor (FET); rather, readout is accomplished by wire-bonding the anodes to the inputs of the ASIC. The ASIC dissipates 32 mW, and offers 16 channels of low-noise charge amplification, high-order shaping with baseline stabilization, discrimination, a novel pile-up rejector, and peak detection with an analog memory. The readout is sparse and based on custom low-power tristatable low-voltage differential signaling (LPT-LVDS). A unit of 64 SDD pixels, read out by four ASICs, covers an area of 12.8 cm^2 and dissipates with the sensor biased about 15 $\mathrm{mW/cm}^2$. As a tile-based system, the 64-pixel units cover a large detection area. Our preliminary measurements at $-44^{\circ}\mathrm{C}$ show a FWHM of 145 eV at the 5.9 keV peak of a $^{55}\mathrm{Fe}$ source, and less than 80 eV on a test-pulse line at 200 eV.**

***Index Terms*—ASIC, charge sharing, high rate, LVDS, PUR, SDD.**

I. Introduction

THE work discussed here is part of a joint effort between the Marshall Space Flight Center and Brookhaven National Laboratory to develop a prototype high-resolution x-ray spectrometer (XRS) for measuring the abundances of light elements fluoresced by ambient radiation. The intended use of the XRS is for elemental mapping of planets surfaces during space explorations [1]. We are developing two versions: the first, with a large sensitive area, is suitable for orbit around the moon [2], [3]; the second, a more radiation-resistant, high-rate version, to serve in extreme environments, such as that of Jupiter and Europa [4]. The first version requires a detection area of 500 cm^2 and an energy resolution better than 100 eV at 280 eV, with a power budget of 20 $\mathrm{mW/cm}^2$. The second version has similar energy-resolution requirements, but must sustain high rates (up to 1 $\mathrm{Mcps/cm}^2$) with a more relaxed power budget, and an order-of-magnitude lower detection area. Detector cooling, not encompassed in the power budget, is assured for operations down to $-40^{\circ}\mathrm{C}$.

The stringent requirements on the detector area, resolution, rate, and power suggest either using standard silicon diodes with high pixelation (a pixel area of few hundred $\mu\mathrm{m}^2$) and bump-bonded front-end electronics, or employing silicon drift detectors (SDDs) [5], [6] with moderate pixelation (a pixel area of few tens of mm^2) and wire-bonded front-end electronics. As discussed in [7], the latter was adopted since more attractive in terms of resolution, interconnects, and charge sharing.

Other research groups reported promising results in terms of rate and resolution with pixelated SDDs with the input transistor (e.g., junction field effect transistor, JFET) integrated with each pixel [8]–[13]. However, integrating the FET imposes an additional technological challenge, might impose a lower limit in the power dissipation (some mW in the JFET itself), and requires somewhat higher complexity in the front-end electronics and interconnects to achieve the required stability, especially at high count rates [14]–[20].

In our SDD the drift field in the pixel is provided by the electrode structures on the pixelated side of the detector, opposite to the entrance side. The largest area of the pixel is covered by a spiral of implanted rectified junction. The current flowing in the rectifying implant of the spiral generates a field very close to the optimal drift field described in [21]. Spirals with several different pitches were tested in the previous version of the spiral SDDs. The current design is based on the maximal number of turns of the spiral [22]. This design leads the spiral with the highest electric resistance and the lowest power dissipation. An optimized entrance window covers the energy range down to 282 eV, corresponding to the Carbon spectral line [23], [24]. The area of each pixel is 20 mm^2, and the power dissipated by the rectifying spiral is about 1 mW. The 100 $\mu\mathrm{m}$ anode, characterized by a capacitance of few tens of fF, is located at the center of the pixel, and is directly wire-bonded to the input of a low-noise Application Specific Integrated Circuit (ASIC) fabricated in a commercial 0.25 $\mu\mathrm{m}$ CMOS technology. The SDD sensors tested here were fabricated at KETEK, GmbH.

We recently reported our first prototype XRS based on a 14-pixel array and a 14-channel ASIC [7]. That prototype achieved a resolution of 172 eV FWHM at the $^{55}\mathrm{Fe}$ 6 keV line, covering an area of 2.24 cm^2 with a dissipation of 23 $\mathrm{mW/cm}^2$. We present here a new XRS prototype comprising 64 pixels connected to four 16-channel ASICs. In Section II we present our 64-pixel XRS prototype. In Section III we introduce a more recent version designed for high rate operation, which implements our novel pile-up rejector.

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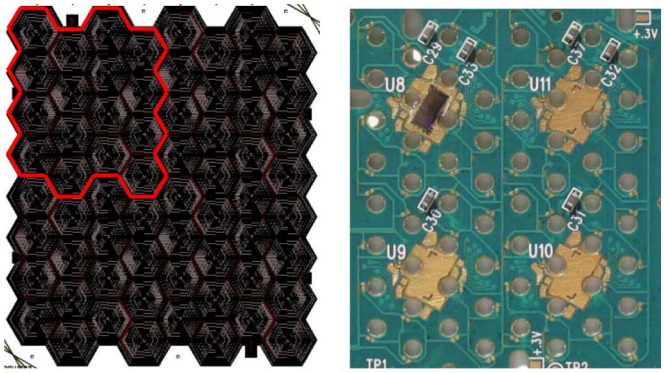
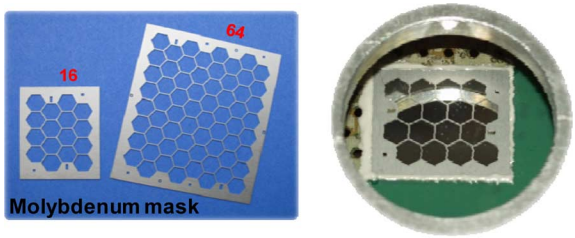


(a) (b)

Fig. 1. (a) Layout of a unit of 64 20 mm^2 SDD pixels, covering an area of 12.8 cm^2; and, (b) photo of the interposer with one of the four ASICs mounted. Each ASICs, sited at a 30 degree angle, reads out an array of 4×4 pixels (red line). The holes for wire-bonding the ASIC inputs to the SDD anodes are shown.



(a) (b)

Fig. 2. (a) Molybdenum masks for the 16- and 64-pixel versions, and, (b) mask mounted on a 16-pixel version used in some measurements reported here.

II. 64-Pixel XRS Prototype

In this section, we introduce our 64-pixel XRS prototype, discuss the ASIC and interconnect architectures, and present some experimental results.

A. Architecture

Fig. 1(a) shows the layout of a SDD unit, composed of 64 hexagonal pixels, each 20 mm^2 in area. The central anodes of each of the four groups of 16 pixels are wire-bonded to the 16 inputs of one of four ASICs though holes in an interposer (see Figs. 1(b) and 13). The interposer also provides wire bond pads for the remaining interconnections for biasing, configuring, and reading out the ASIC, and for biasing the sensor. The SDD unit, covering an area of 12.8 cm^2, dissipates less than 15 $\mathrm{mW/cm}^2$ (10 $\mathrm{mW/cm}^2$ from the electronics, the rest from the sensor), and is designed to be tiled over a large area.

Fig. 2 depicts the molybdenum mask we sited at the entrance side of the sensor, opposite to the pixelated side. Its purpose is to prevent ionizing radiation from reaching the sensor along the edges of the pixels, thus reducing charge sharing between pixels, and consequently, increasing the peak-to-background ratio. The thickness and the width between pixels of the molybdenum mask are 125 μm and 240 μm respectively.

Fig. 3 is a block diagram of the ASIC. It has 16 front-end channels, multiplexers, common bias-circuitry, registers, DACs, control and readout logic, and a temperature sensor. Each channel has a MOS-only [7] dual-stage charge amplifier

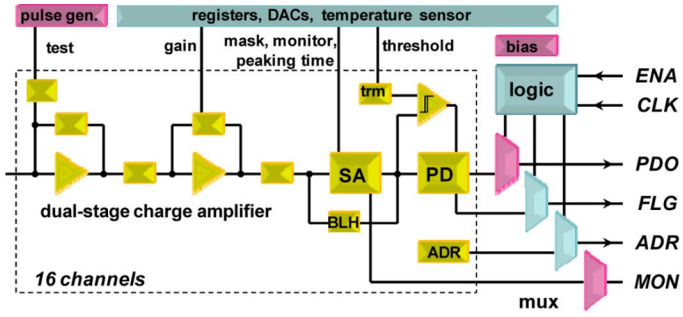


Fig. 3. Block diagram of the 16-channel ASIC.

with adaptive reset [25] providing a charge gain 1551 or 775.5. The amplifier input MOSFET operates with a drain current of 200 μA and it is optimized for an input capacitance of 200 fF [26]. The charge amplifier is followed by a 5th order shaper (SA) [27] with adjustable peaking time (0.5-, 1-, 2-, 4-μs), and the output baseline is stabilized with a band-gap-referenced Baseline Holder (BLH) circuit [28]. The overall voltage/charge gain is adjustable to 2.6 and 5.2 V/fC.

A low-hysteresis comparator with multiple-firing suppression [29] discriminates events, with a threshold controlled by a 10-bit DAC common to all channels, and a 3-bit DAC in each channel for equalization. The above-threshold events are processed by a multi-phase peak detector (PD) with an analog memory [29], [30]. A flag (FLG), released after a first peak is found, indicates that one (or more) successful acquisition is ready to be read out. At each clock (CLK) the peak amplitude (PDO) and the address (ADR) of all the events above threshold are made sequentially available at the dedicated outputs, thus providing sparsification. The ASICs can be read out per column with an automatic token-passing scheme, similar to the one we described in [31], and with a edge-based digital signal for chip selection.

Each channel also implements a pixel leakage current measurement circuit. The leakage current, multiplied by the gain of the charge amplifier, is absorbed by the BLH to maintain the output baseline at a constant voltage. A current source, controlled by the BLH and proportional to the leakage current, is converted into a voltage and it is made available by multiplexing through the analog monitor. The gain of this leakage current measurement circuit is about 1 mV/pA. A temperature sensor is also integrated with a gain of about 5.5 $\mathrm{mV/°C}$.

For the digital interface, we developed a custom, low-power, tristatable low-voltage differential signaling (LPT-LVDS) wherein the output requires a 2 kΩ termination and a driving current of 150 μA, and which dissipates 700 μW and 200 μW, respectively, in the transmitter and receiver. The settling time is 10 ns with a 10 pF capacitive load. Fig. 4(a) shows the non-tristatable case, while Fig. 4(b) shows the tristatable one, used for the flag (FLG) signal, which several chips can share. With an area of 2.2×4.7 mm^2 the ASIC dissipates 32 mW (1.7 mW/channel plus 5 mW for shared circuits).

B. Experimental Results

Whilst our original XRS prototype gave encouraging results [7], we identified two issues. First, the gain was about 20% lower

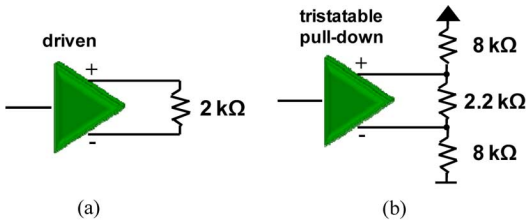


Fig. 4. Low-power differential transmitters: (a) driven, and, (b) tristatable with pull-down resistors. Each transmitter, when active, dissipates 700 μW to drive the 2 kΩ off-chip resistor.

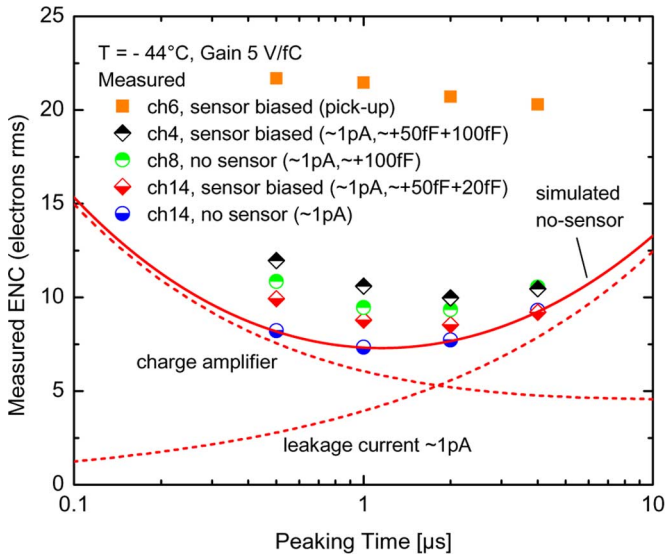


Fig. 5. Equivalent Noise Charge (ENC) versus peaking time measured for different channels with input floating and connected to the SDD pixel anodes. The simulated ENC and its contributions, assuming no sensor and a leakage current of 1 pA, are also shown.

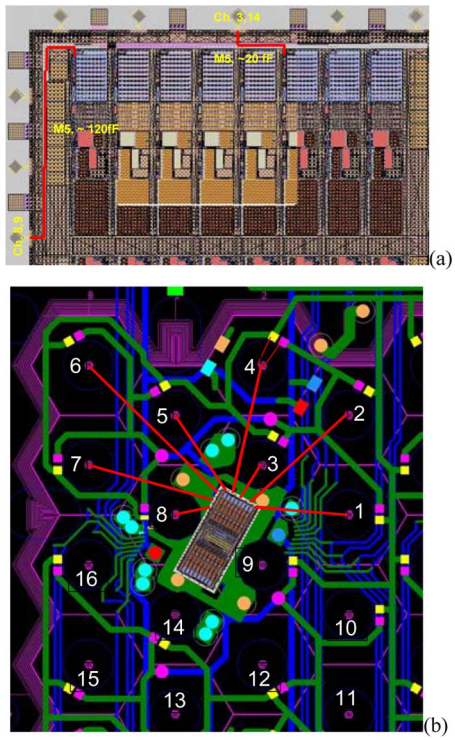


Fig. 6. Details of the layout illustrating (a) the on-chip interconnection between the input of the channel and its bonding pad (lines in red for two extreme cases), and, (b) the wire bond interconnection between the ASIC bonding pads and the SDD anodes for different pixels (lines in red).

than the design value, due to parasitic capacitance between the input node and the internal gain node of the front-end amplifier, so affecting pole-zero cancellation, and eventually, the resolution of the front-end at high rate. Second, the stability of the peak detection [32] and its noise contribution were of concern; both affected the resolution of the system and its ability to discriminate low amplitudes. These issues were resolved in the present XRS prototype. A third minor issue was more recently found, consisting of a small decrease in gain at low temperature. The decrease is due to the compression of the gate-source voltage of the MOSFETs used as feedback capacitors (see [7, Fig. 7]), which reduces the charge amplifier loop gain. This issue has been addressed in a further ASIC revision, now being fabricated.

Fig. 5 shows the Equivalent Noise Charge (ENC) measured at $T = -44°\mathrm{C}$ on some channels with the input floating and connected to the anode of the biased SDD pixel. Fig. 6(a) explains the difference between the two floating channels 14 and 8, due to the on-chip parasitic capacitance from the interconnection line between the input of the channel and its bonding pad. A difference of about 100 fF was extracted, corresponding to about 10 fF/100 μm. Fig. 6(b) explains the difference between channels 14 and 4 when connected to the SDD anodes, due to the parasitic capacitance of the wire bond. An increase of about 80fF was extracted, corresponding to about 10 fF/mm. The side channels (channel 6 plotted in Fig. 5, plus channels 7, 16, 15, and 2, 1, 10, 11, as in Fig. 6(b)) exhibited considerable pick-up from the noise on the LVDS lines connected directly to our DAQ integrated in the computer; pick-up was present also when the LVDS signals were inactive. The coupling was between the input wire bonds and portions of the digital traces flowing either below them or close to the holes (see Figs. 1(b) and 13). In the latter case, the coupling also was through lines routed in an inner layer of the interposer.

Fig. 7 plots the ENC against the injected charge measured using the internal pulse generator and test capacitor (~ 30 fF) with the input connected to the SDD anode. The inset depicts the corresponding spectral lines. The progressive increase with input charge of up to 8 e^- at 2,700 e^- (≈ 10 keV) is caused by the discharge process in the feedback MOSFET of the charge amplifier [25]. The test capacitor contributes to the ENC with about 2.5 $\mathrm{e}^-\mathrm{rms}$, and the pulse generator with about 3.5 $\mathrm{e}^-\mathrm{rms}$. This gives an electronic resolution of about 10 $\mathrm{e}^-\mathrm{rms}$ at 1 μs peaking time, in line with the results shown in Fig. 5.

Fig. 8 plots the ^{55}Fe spectrum measured at a peaking time of 1 μs and a rate of about 1 kcps, and compares it to one acquired by routing the analog monitor to a commercial Multichannel Analyzer (MCA). A FWHM of about 153 eV was measured at the 5.9 keV $\mathrm{Mn}_{k\alpha}$ spectral line, which corresponds to an electronic resolution (once subtracted statistics with Fano) of about 11.5 $\mathrm{e}^-\mathrm{rms}$ at the 0.26 fC ($\sim 1,630$ e^-) input charge. Assuming a contribution from the discharge of the feedback MOSFET of about 5 $\mathrm{e}^-\mathrm{rms}$,we can expect a resolution of about 85 eV FWHM (10 $\mathrm{e}^-\mathrm{rms}$) at low energies. A peak-background ratio

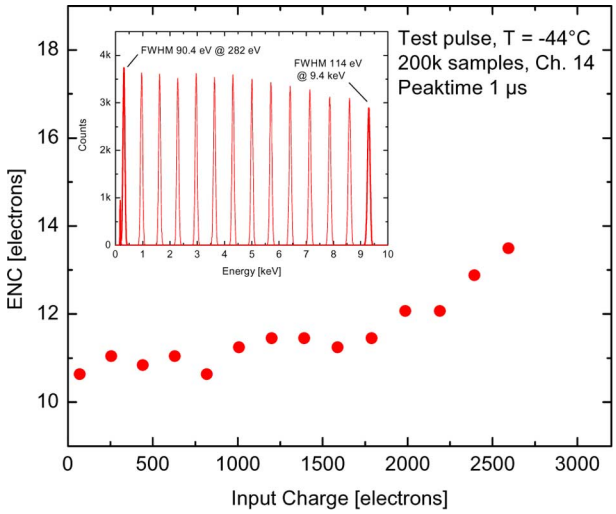


Fig. 7. Measured ENC versus injected charge and corresponding spectral measurements for 1 μs peaking time.

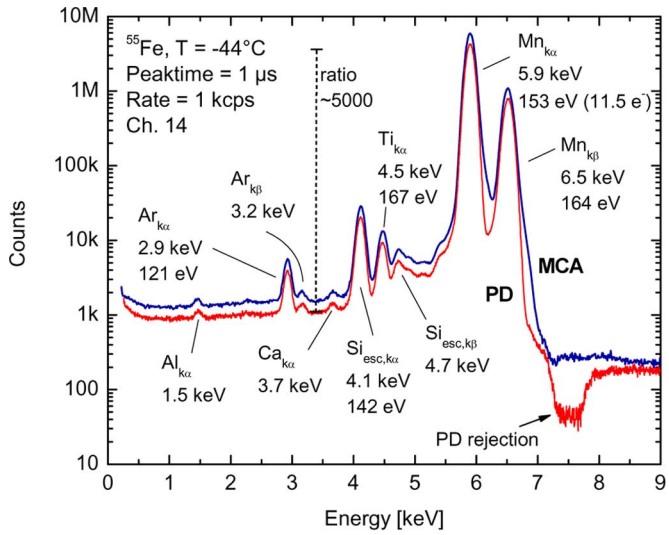


Fig. 8. Spectrum from a ^{55}Fe source (red) compared with one measured by feeding the shaper output through an analog monitor to a commercial Multichannel Analyzer MCA (blue).

of about 5000 also is apparent. This considerable improvement over that of our original version (about 300 [7]) is mainly due to reducing charge-shared events with the molybdenum mask (see Fig. 2).

Comparing the two spectra highlights their differences at the right side of the two main spectral lines $\mathrm{Mn}_{k\alpha}$ and $\mathrm{Mn}_{k\beta}$: some pile-up rejection occurs when employing the internal multi-phase peak detector [30]. This phenomenon is explained by examining the two cases of pile-up in Fig. 9. In the first case (a) the peak detector (PD) that is sensitive only to the first change in slope, detects and stores the first peak, while the MCA detects the highest peak in a fixed time-window. It results that the PD properly processes the first peak and rejects the second, highest peak while the MCA doesn't. As the delay between the two pulses declines, we enter the second case (b) where lacking the first peak, both the PD and the MCA perform

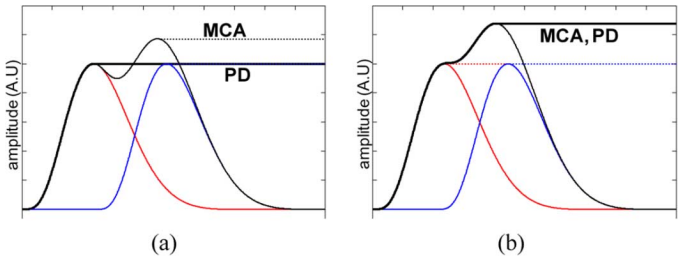


Fig. 9. Comparison (a) between the responses of a multi-phase peak detector (PD), sensitive to the first change in slope, and (b) a multi-channel analyzer (MCA), sensitive to the highest peak in a given time window, for two different cases of pile up. The red and blue are the two single pulses, with peak voltages represented with dashed lines. The black line is the resulting piled-up pulse: the peak voltages processed by the PD and MCA are marked.

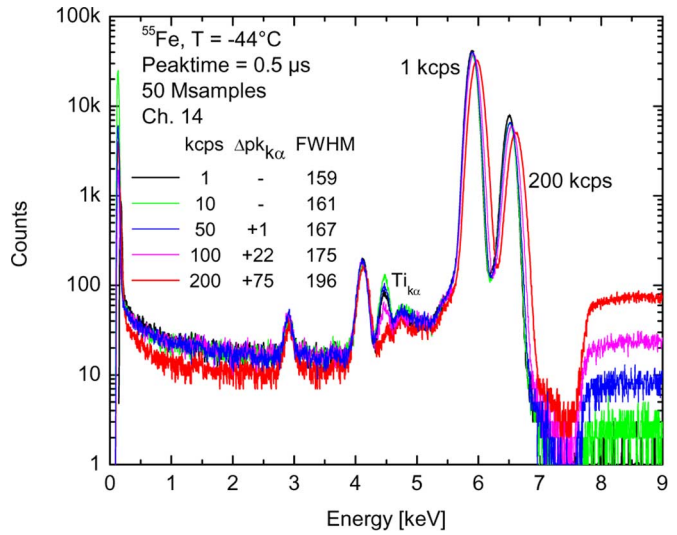


Fig. 10. Spectra from a ^{55}Fe source with rate variable from 1 to 200 kcps. The shift $\Delta pk_{k\alpha}$ of the $Mn_{k\alpha}$ line and the resolution are in eV.

identically. The sharper spectral lines and the deep region at their right side correspond to those events from case (a) of Fig. 9, while the further right region where the spectra adopt a similar behavior corresponds to events from case (b).

Fig. 10 shows some ^{55}Fe spectral measurements at a peaking time of 0.5 μs for input rates ranging from 1 to 200 kcps. The two main spectral lines $\mathrm{Mn}_{k\alpha}$ and $\mathrm{Mn}_{k\beta}$ exhibit a shift and broadening at high count rates [33], along with a relative decrease of background events at low energies. This behavior is explained as illustrated in Fig. 11 showing two cases of pile up between a low-amplitude and a high-amplitude event; independent of the sequence, the low-amplitude event is lost and contributes a small amount to the high-amplitude one. Considering the stable baseline afforded by the Baseline Holder [28], the pile-up entails a loss of low-amplitude events and a broadening and shift of high-amplitude events.

III. XRS Prototype With Pile-Up Rejection

In this section, we describe a more recent version of the XRS prototype, which includes our new concept for an analog pile-up rejector, and we discuss some preliminary experimental results.

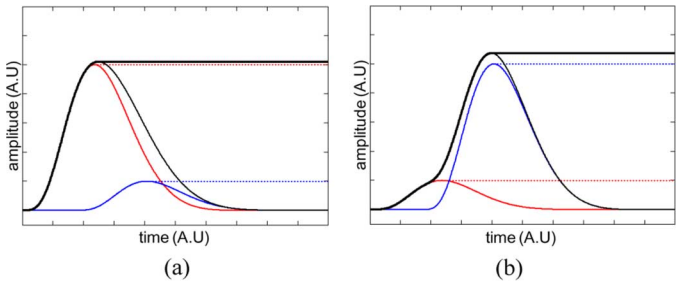


Fig. 11. Examples of pile-up between a low-amplitude and an high-amplitude event. Independent of the sequence, the low-amplitude event is lost and contributes a small amount to the high-amplitude one.

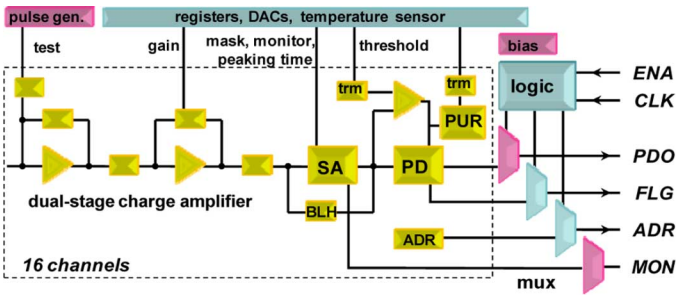


Fig. 12. Block diagram of the new version of the ASIC.

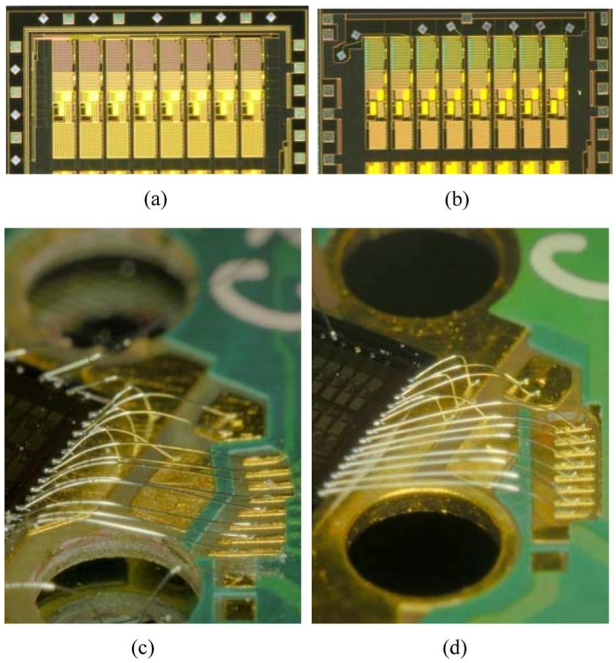


Fig. 13. Some recent improvements: details of placing the pads and routing the inputs of eight channels for (a) previous version, and, (b) new version; details of the holes and shielding the digital lines for (c) previous version, and, (d) new version.

A. Architecture

Most improvements made in this new prototype aimed at reducing the parasitic capacitance and pick-up at the charge sensitive input nodes (see Figs. 5 and 6), and at improving the system's rate capability. The ASIC block diagram is shown in Fig. 12. The high-order shaper has now a peaking time adjustable to 0.25-, 0.5-, 1-, and 2-μs, a factor of 2 smaller the previous version. The area, 2.1×4.6 mm^2, is slightly smaller and the power dissipation is the same (about 2 mW per channel). Another major improvement consists of the pile-up rejector (PUR), discussed in the Section III-B.

To reduce the parasitic capacitance at the inputs, we optimized the placement of the input bonding pads and the routing of the interconnections between the input of the channel and its bonding pad (Fig. 13(a) and (b)). Other improvements, shown in Fig. 13(c), consisted of shielding the input nodes from the digital lines flowing in the interposer. We implemented two solutions: (i) Gold-plating the holes for input interconnections, and, (ii) hiding the digital lines in an inner layer and exposing those for wire bonding only when they were close to the ASIC. These details are visible when comparing the bottom (gold-plated holes) and right (inner hidden lines) of Fig. 13(c) and (d). The interposer was also equipped with buffers for all LVDS signals, and with on-board Analog-to-Digital Converters (ADCs) to improve throughput by reducing the settling time of the analog signals and to improve the analog signal by reducing the signal path.

With these optimizations, we observed improvements in the ENC. Fig. 14 plots the ENC measured for some channels without and with the sensor. Channels 14 and 8, respectively, are characterized by the shortest and longest on-chip interconnections between the input of the channel and its bonding pad.

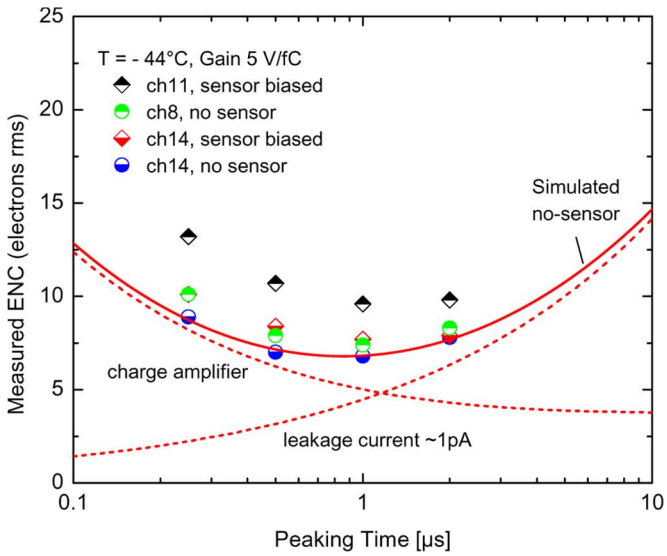


Fig. 14. ENC versus peaking time measured with the new version for different channels with input floating and connected to the SDD pixel anodes. The simulated ENC and its contributions, assuming no sensor and a leakage current of 1 pA, are also shown.

We note that the increase in ENC is smaller than in the previous version (see Fig. 5) demonstrating the effectiveness of our on-chip optimization. Channels 14 and 11, respectively, have the shortest and longest wire-bond connection from the ASIC input pad to the SDD anode (see Fig. 6(b)). Furthermore, channel 11 that, with channel 6, constitutes the worst case in terms of capacitance and exposure to pick-up, can achieve at 1 μs peaking time a sub-10 electrons ENC, corresponding to a FWHM of about 85 eV for low-energy spectral lines.

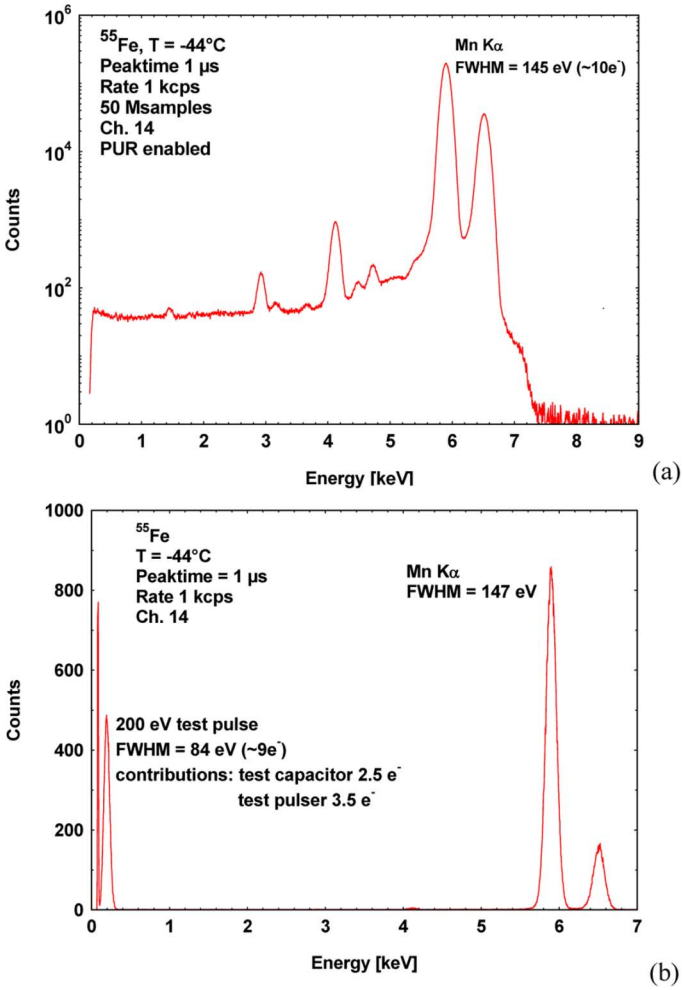


Fig. 15. Spectra from a ^{55}Fe source measured with the new prototype without, and (b) with a test pulse.

In Fig. 15 we show spectral measurements at a low rate (about 1kcps) from channel 14 with a ^{55}Fe source. We measured a resolution of 145 eV FWHM at the $\mathrm{Mn}_{k\alpha}$ line (Fig. 15(a)) corresponding to an electronic resolution of about 10 $\mathrm{e^-rms}$. Taking into account the contribution from the discharge of the feedback MOSFET, a resolution of about 70 eV FWHM (8 $\mathrm{e^-rms}$) can be expected at low energies. This result was confirmed by adding a test pulse with amplitude equivalent to an energy of 200 eV, as illustrated in Fig. 15(b). A resolution of 84 eV FWHM was measured which, after subtracting the contributions from the 30 fF test capacitor (about 3.5 $\mathrm{e^-rms}$) and the pulse generator (about 2.5 $\mathrm{e^-rms}$), corresponds to 70 eV FWHM on a 200eV spectral line.

Fig. 16 is an overview of the ^{55}Fe spectral measurements for all 16 channels. A resolution of 152 eV FWHM $\pm$ 5% was measured on the $\mathrm{Mn}_{k\alpha}$ line. Considering the noise from the discharge in the feedback MOSFET of the charge amplifier, this corresponds to an electronic noise of about 84 eV FWHM $\pm$ 4 eV at low energies. We noted an increase in background at low energy for all pixels along the edge, possibly signifying an increase in the charge-sharing region. This clearly warrants further investigation.

Fig. 16. Overview of ^{55}Fe spectral measurements on all 16 channels. A resolution of 152 eV FWHM $\pm$ 5% was measured on the $\mathrm{Mn}_{k\alpha}$ line. Considering the noise from the discharge in the feedback MOSFET of the charge amplifier, this corresponds to about 84 eV FWHM $\pm$ 4 eV at low energies.

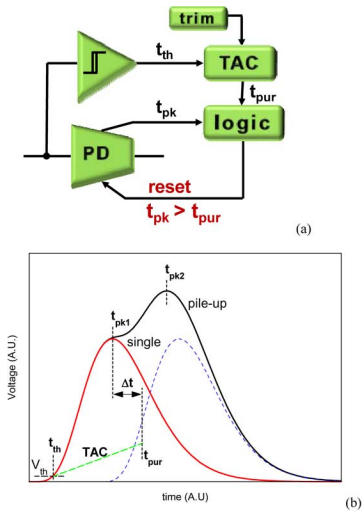


Fig. 17. (a) Block diagram, and (b) graph illustrating the operation of the pile-up rejector (PUR) implemented in the ASIC. A single- and a piled-up-pulse are shown, along with the timing of the discriminator (threshold crossing, t_{th}) and peak detector (peak time, t_{pk}).

B. Pile-Up Rejection

When comparing the spectrum in Fig. 15 with the one in Fig. 8 (previous version), along with the improvement in resolution, we see a substantial suppression of the piled-up events in the former, characterized by amplitudes higher than the two main ^{55}Fe peaks $\mathrm{Mn}_{k\alpha}$ and $\mathrm{Mn}_{k\beta}$. The spectrum was measured with the pile-up rejector enabled (PUR in Fig. 12). Fig. 17(a) and (b) are a scheme and a graph illustrating the operation of the PUR. The only circuits added to the previous electronics are the Time-to-Amplitude converter (TAC), the logic, and the trimmer to adjust the TAC duration.

The PUR employs timing signals from the discriminator at threshold crossing, t_{th}, and from the peak detector at the peaking time t_{pk}. A timing window is defined, based on a time-to-amplitude converter (TAC) that starts at $t = t_{\mathrm{th}}$ and,

making use of a Schmitt trigger, stops at $t = t_{\rm pur}$. The timing window is adjusted so that the peaking time t_{pk} of single pulses occurs before $t_{\rm pur}$, i.e., $\Delta t > 0$ in Fig. 17(b).

When a peak is detected, the logic compares the timing signals t_{pk} and $t_{\rm pur}$. If $t_{pk} \leq t_{\rm pur}$ (single case in Fig. 17) the pulse is accepted and the channel-event indicator (Flag) is released to start the readout process; however, if $t_{pk} > t_{\rm pur}$ (pile-up case in Fig. 17) the pulse is rejected and the logic resets the channel for a new acquisition. The choice of Δt is critical for ensuring the proper operation and efficiency of the PUR; it must account for the time jitter and the time walk associated with the timing signals $t_{\rm th}$ and t_{pk}. The time jitter $\sigma t_{\rm th}$ of $t_{\rm th}$ is approximated as

$$\sigma t_{\rm th} \approx \left. \frac{\sigma_V}{\frac{{\rm dV}}{{\rm dt}}} \right|_{V=V_{\rm th}} \tag{1}$$

where σ_V is the rms voltage noise, and dV/dt is the slope of the signal calculated at the crossing of the threshold voltage $V_{\rm th}$. Depending on the type and order of the shaper, simple equations or moderately simple numeric calculations can generate $\sigma t_{\rm th}$. The time jitter σt_{pk} of t_{pk} can be estimated as

$$\sigma t_{pk} \approx \frac{\sigma_V \tau_p \lambda_p}{-\rho_p} \tag{2}$$

where τ_p is the peaking time (1% to peak), and the two coefficients λ_p and ρ_p depend, respectively, on the type and order of the shaper [29], [34]. In our case of a 5th order shaper with complex conjugate poles, the corresponding values of the two coefficients are 1.58 and 3.65 [29].

Concerning the time walk, for the peaking time t_{pk} it can be assumed to be a first order independent of the peak's amplitude [35], while for threshold crossing, it depends again on the type and order of the shaper, and it can be obtained from simple equations or moderately simple numeric calculations.

Fig. 18 displays typical curves for $\sigma t_{\rm th}$ and σt_{pk}, normalized to the peaking time τ_p, as functions of the peak amplitude normalized to the full scale V_{fs}.; $V_{\rm th}$ and σ_V are assumed to be 1% and 0.3% of V_{fs}, respectively. In the same Fig. 3, $\sigma t_{\rm tot}$ is plotted where $\sigma t_{\rm tot}$ is the quadratic sum of $\sigma t_{\rm th}$ and σt_{pd}, assuming no correlation as the worst case. It readily is observed that to ensure negligible rejection of valid single pulses, Δt should exceed 3 $\sigma t_{\rm tot}$, which rises as the peak amplitude declines. This figure also illustrates the time walk Δt_w associated with the threshold crossing, that also increases as the peak amplitude drops. On the one hand, the trend of the time walk lowers the efficiency of the pile-up rejector at low amplitudes. On the other hand, since the time walk exceeds the 3 $\sigma t_{\rm tot}$, it prevents the loss of valid events over a wide range of amplitudes when small values of Δt are chosen (e. g., $\Delta t \approx 0.05\tau_p$).

In the case shown in Fig. 18, we chose a value of $\Delta t \approx 0.05\tau_p$ (5% of the peaking time). Due to the time walk, the efficiency of the PUR decreases with the peak amplitude, but no single events are lost due to time jitter. This outcome is quantified by simulating the single-energy spectral lines for different amplitudes.

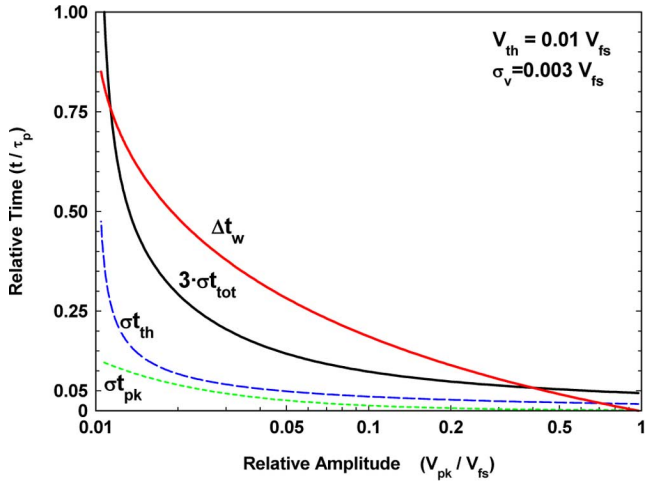


Fig. 18. Typical curves of $\sigma t_{\rm th}$ and σt_{pd}, 3 $\sigma t_{\rm tot}$, and Δt_w, normalized to the peaking time τ_p, as function of the relative peak amplitude.

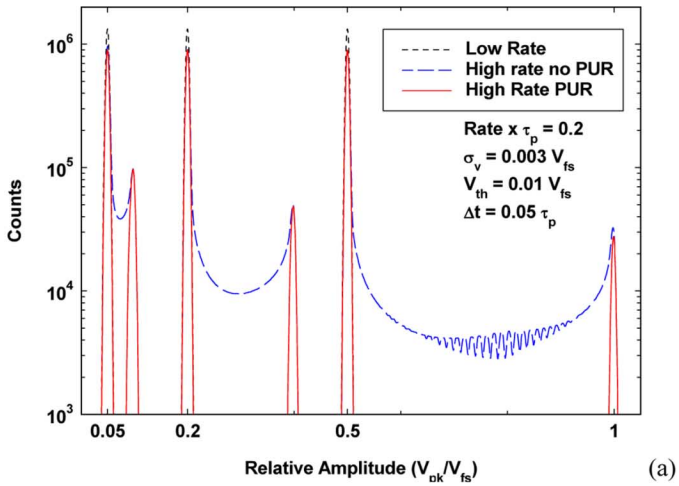


Fig. 19. (a) Simulated spectral lines for different peak amplitudes at low- and high-rate without and with PUR, and (b) PUR efficiency $\varepsilon_{\rm PUR}$ versus relative peak amplitude.

Thus, in Fig. 19(a) the spectrum for three different relative amplitudes 0.05, 0.1, and 0.5 is shown for the low rate and the high rate $({\rm rate} \times \tau_p = 0.2)$ with and without PUR. The values of $V_{\rm th}$ and σ_V, respectively, are assumed as 1% and 0.3% of V_{fs},

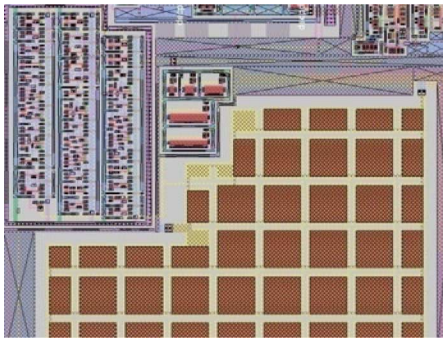


Fig. 20. Layout of the PUR circuit integrated in the ASIC channel, size $90 \times 100\ \mu\mathrm{m}^2$.

and a value of $\Delta t \approx 0.05\tau_p$ is chosen for the PUR. The plots show the effectiveness of the PUR in rejecting events in the region between the main line and the double-amplitude line.

As a measure of the efficiency $\varepsilon_{\mathrm{PUR}}$ of the PUR, we can adopt the ratio of the FWHM of the main spectral line with respect to the FWHM_2 of the corresponding double-amplitude line as follows:

$$\varepsilon_{\mathrm{PUR}} = \sqrt{2}\frac{\mathrm{FWHM}}{\mathrm{FWHM}_2}. \tag{3}$$

It is noted that any PUR, including the ideal case, fails to discriminate and reject events that are fully superposed. In that case the pulse results from the superposition of two individual non-correlated x-ray events. The corresponding FWHM_2 is a factor $\sqrt{2}$ larger than the FWHM of the main line. Hence the coefficient $\sqrt{2}$ in (3); in the ideal noiseless case $\varepsilon_{\mathrm{PUR}}$ approaches the unity.

Fig. 19(b) shows the PUR efficiency $\varepsilon_{\mathrm{PUR}}$ vs the relative amplitude V_{pk}/V_{fs} and it reveals that the efficiency decreases as the peak amplitude decreases, followed by an increase that arises from the decline in the contribution of the piled-up events to broadening compared with the actual noise. In fact, in contrast to the noise, the contribution of the pile-up to the line broadening drops as the peak amplitude falls.

Finally, from Fig. 19(a) we note that, as expected, the peak-to-valley ratio of the spectrum with pile-up decreases with amplitude, because, at low amplitudes, the same number of pile-up events spreads over a smaller range of amplitudes. So far, we assumed negligible dispersion in the diffusion of the charge collected at the anode of the SDD pixel. In actuality, dispersion increases with the distance of the anode from the interaction point, and was estimated at about 15 ns rms. The corresponding impact on the amplitude and peaking time is about 0.02% and 7.5 ns. To avoid loss of valid single events, the latter value must be added to Δt.

The PUR circuit integrated in the ASIC channel implements a 3-bit trimmer to adjust and optimize the value of Δt. Fig. 20 shows the layout of the PUR, which dissipates less than 1 μW at 200 kcps in an area of $90 \times 100\ \mu\mathrm{m}^2$.

Fig. 21 compares two $^{55}\mathrm{Fe}$ spectra measured at 200 kcps without and with the PUR. The gain was set at 2.6 V/fC, thus extending the energy range to more than 18 keV. The

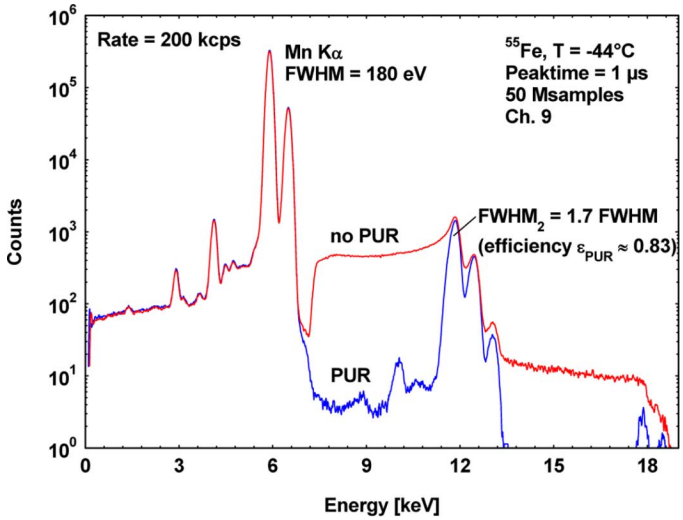


Fig. 21. Spectra from a $^{55}\mathrm{Fe}$ source measured without and with PUR at a rate of 200 kcps, a peaking time of 1 μs, and a gain of 2.6 V/fC.

main-, double-, and triple-lines of $\mathrm{Mn}_{k\alpha}$ and $\mathrm{Mn}_{k\beta}$ and their combinations can be observed. Our measured ratio, $\mathrm{FWHM}_2/\mathrm{FWHM} \approx 1.7$, corresponds to a PUR efficiency $\varepsilon_{\mathrm{PUR}} \approx 0.83$ and is slightly lower than we anticipated from the simulations of Fig. 19. Due to a design error, the trimming range was shifted, and the lowest available value of Δt used in these measurements was higher than the optimum. We resolved this issue in an ASIC revision now being fabricated.

Several pile-up rejection techniques were proposed. Some use digital signal processing, and require fast analog-to-digital conversion (ADC) of the analog signal [33], [36], [37]. These solutions, mostly based on shape discrimination, in principle may offer better rejection performance than ours, and other advantages, like recovering some piled-up pulses by amplitude correction [38]–[40]. However, the power and processing time needed to perform ADC per channel and digital processing currently is prohibitive for all applications requiring either a high density of channels or a limited power budget. Among the analog techniques adopted, the most common uses an additional fast shaper and veto logic to detect and reject pile-up in the main slow shaper [20], [41], [42]. Due to the higher noise and the width of the fast-shaped pulse, efficiency is lower at low amplitudes and for closely spaced pulses, as in our case. The drawback is in the need for additional shaping and discrimination circuits. We note that rejecting pile-up events with an internal reset, transparent to the external readout electronics, also minimizes dead time compared to off-line rejection. Additionally, the proposed technique best uses the already available circuits (the discriminator and the peak detector with the peak-found signal). These are further advantages of our approach compared to other analog techniques [43]–[45] that are characterized by higher complexity or need for additional conversion and off-line processing.

IV. Conclusions and Future Work

We discussed our progress in developing a high-resolution and low-power x-ray spectrometer (XRS) for extra-terrestrial

applications. Our XRS is based on pixelated Silicon Drift Detectors with anodes directly wire-bonded to the inputs of an Application Specific Integrated Circuit (ASIC). The results achieved with our most recent version are within the requirements for some low-rate space missions. Our next version will focus on optimizing performance for high-rate environments, and might be characterized by a more relaxed power budget. We described our novel pile-up rejector that gave encouraging results, while leaving margins for its optimization.

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