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Characterization of space charge layer deep defects in n^+-CdS/p-CdTe solar cells by temperature dependent capacitance spectroscopy

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Temperature Dependent Capacitance Spectroscopy (TDCS) was used to identify carrier trapping defects in thin film n^+-CdS/p-CdTe solar cells, made with evaporated Cu as a primary back contact. By investigating the reverse bias junction capacitance, TDCS allows to identify the energy levels of depletion layer defects. The trap energy levels and trap concentrations were derived from temperature-dependent capacitance spectra. Three distinct deep level traps were observed from the high-temperature ($T > 300$ K) TDCS due to the ionization of impurity centers located in the depletion region of n^+-CdS/p-CdTe junction. The observed levels were also reported by other characterization techniques. TDCS seems to be a much simpler characterization technique for accurate evaluation of deep defects in n^+-CdS/p-CdTe solar cells. © *2013 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4800830]

INTRODUCTION

In today's practical thin film photovoltaic devices various measurement techniques and a number of physical mechanisms are used to interpret the nature of defects. This complicates with the data interpretation and leads to discrepancies in proper identification of shallow and deep trap levels.[1] It is known that an impurity acts as a trap or a generation and recombination (G-R) center depending on the trap energy level E_t, the location of Fermi level in the band gap, the temperature, and the capture cross-section of the impurity/trap. In general, those impurities near the middle of the band gap behave as G-R centers, whereas those near the valence band edge act as acceptors. But in case of CdTe solar cells some of the observed activation energies of dopant levels are non-shallow. The partially ionized dopants, therefore, play the role of both an advantageous dopant as well as a detrimental trap.[2] The consideration of simplified assumptions, which may be completely valid for silicon, may not be accurate in CdTe solar cells.

In addition, the performance of CdTe solar cell is highly influenced by the deep levels as the deep levels control the efficiency and charge transport properties. CdTe is a compound semiconductor involving a large concentration of intrinsic defects, produced during fabrication process. Although significant work has been done about the properties of CdTe and CdS films, there remains a lack of fundamental understanding about the identification of electronics defect states in polycrystalline CdTe.

The main characterization techniques used for study of deep levels in CdTe solar cells are based on Admittance Spectroscopy (AS), Photoluminescence (PL), Photo induced current transient spectroscopy (PICTS), and Deep Level Transient Spectroscopy (DLTS) measurements.[3–15] DLTS characterizes the deep levels by monitoring the transients of junction capacitance. But, for highly resistive materials DLTS is not as useful due to the small junction capacitance and difficulties in injecting free carriers with a voltage pulse. In addition, the transient analysis in DLTS is done through application of a pulse where the pulse width and height was managed to accurately evaluate the CdTe layer. The activation energy, E_a, trap concentration, N_t, and the capture cross-section, σ_∞, can be estimated from the Arrhenius plot, $\ln(T^2/e_p)$ versus $1/T$, where e_p is the hole emission rate. A simpler technique known as temperature dependent capacitance spectroscopy (TDCS) can be employed to estimate all the above parameters to identify the deep level traps.[16] As compared to admittance spectroscopy, which operates in frequency domain, TDCS works in time domain making it a simpler and an easy technique to evaluate defect levels in CdTe solar cells. TDCS has also been effectively used to investigate several high resistive materials with special emphasis for GaAs substrates.[17] In capacitance spectroscopy[18] measurement at low frequency was used such that carriers can fully respond to small signal changes of bias. Since in CdTe, the deep level states exhibit capacitance transients the TDCS method is more effective. Because of its better immunity to noise and surface channel leakage current in TDCS provides accurate results when temperature is varied at a fixed frequency. It was also inferred that the density of defect states is proportional to the temperature derivative of the capacitance.[19]

In this work, CdTe solar cells, fabricated with Cu-evaporated back contacts were characterized to demonstrate the effectiveness of TDCS technique. The temperature dependent C-V characteristic was monitored as a function of time. CdTe solar cells with Cu-evaporated back contacts demonstrated the capacitance peaks at a frequency of 100 kHz indicating the trap charge builds up due to deep levels. After incorporating the temperature dependence of cross-section in

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the activation energy, the observed deep levels were attributed to doubly ionized cadmium vacancies and Cu-related sites identical to reported experimental results[9,12,15,20–27] obtained for deep defects. It is demonstrated that TDCS offers a rapid and convenient means of detecting and characterizing the properties of the deep centers. In addition, we have described the detailed theoretical background of the trap activation energy and temperature dependence of capture cross-sections.

EXPERIMENTAL DETAILS

CdTe solar cells with the area of 0.25 cm^2 were fabricated on 4″ × 4″ commercially-available soda-lime glass substrate coated with SnO_2: F/HRT. Area of the cells was selected for film uniformity and characterization temperature uniformity.[28] The CdS (~80 nm in thickness) was deposited by chemical bath deposition (CBD) at 88 °C using cadmium chloride, thiourea, ammonium acetate and ammonia, and then annealed at 400 °C. The CdTe (12 μm in thickness) was deposited by close-spaced sublimation (CSS) at $T_s = 600$ °C using graphite susceptors and in 10-15 Torr He/O_2.[29,30] The CdTe was then soaked in $CdCl_2$/methanol at 80 °C, followed by a furnace anneal under controlled conditions (380 °C, He/O_2, 300 Torr) in order to improve CdTe structure and minority carrier lifetime. The $CdCl_2$ treatment also appears to promote intermixing of the CdS into the CdTe,[31] and the presence of S in the CdTe may serve to passivate defects. To form the back contact, a nitric-phosphoric (NP) acid etch was used to remove the surface oxide, and a 20 nm of Cu was evaporated. The deposition rate was found to be approximately 7.5 Å per minute. Slow deposition requires very low base pressure in evaporator, so that it does not introduce impurities like O_2 into film. The deposition rate was estimated using a time versus thickness curve that was prepared by measuring film thickness after depositing it on bare glass substrates. Copper evaporation was followed by application of a paste that was prepared by stirring 4 g ZnTe (−140 mesh: Alfa Aesar-44412) with 2 at. % of Cu, −625 mesh powder (Alfa Aesar-41205) into 10 g of conducting graphite paste (Acheson Electrodag 114). The paste is thinned as needed with methyl ethyl ketone (MEK) to prepare the samples. The samples were subjected to annealing in Helium at 160 °C to improve contact quality. The overall process was similar to that described by Rose *et al.*[32] and it is also discussed in Refs. 9 and 33.

Initial current-voltage characteristics under 1 sun illumination (~100 MW/cm^{-2} for filtered xenon lamp) showed J_{sc} and V_{oc} of 20.9 mA/cm^2 and 0.75 V, respectively. It has a fill factor of 54% and efficiency of 7.7%. The device demonstrated the typical characteristic of a CdTe solar cell. The temperature-dependent C-V measurements were carried out in dark by using an Agilent 4284 LCR meter. Sample temperature was varied from 300 K to 363 K with step of 5 K on a micromanipulator probe station. The temperature dependence tests of capacitance (C) vs. time (t) were performed with a fixed frequency of 100 kHz with a 5 mV ac signal. The information about the deep levels in the band gap of CdTe absorber layer was then obtained through TDCS by varying the temperature. A curve tracer was used to obtain a continuous dC/dt spectrum. Most of the measurements were performed, while maintaining a reverse bias at −1 V. Device integrity was observed prior to TDCS measurements by evaluating the dark I-V characteristic.

THEORETICAL BACKGROUND

In CdTe layer, the deep level impurity serves as a Generation-Recombination (G-R) center and both the conduction and valence bands participate in recombination and generation process. As the capacitance of the depletion layer varies as a function of time as the charge response changes with time when voltage is applied. Since the contribution of interface traps to the capacitance already considered the deep level impurities or traps in the semiconductor bulk can respond to capacitance-time profile. The contribution of traps is a complicated function of density and energy level of the traps as well as the sample temperature and frequency of the ac voltage. A potential problem arises for deep-lying dopant atoms not fully ionized at the measurement temperature. Unlike the dopants (phosphorous, arsenic, and boron) in silicon that are ionized completely, some of the deep level impurities in p-type CdTe are only partially ionized in room temperature. Therefore, in the quasi neutral region (qnr), the hole density is no longer equal to N_A in qnr.

The detailed theoretical background of alternating current (ac) capacitance in the n^+-CdS/p-CdTe solar cell diode has been provided by various authors.[34–36] Here, we recall some essential points as applicable to our discussion. The dc bias is set to −1 V and we consider holes as the majority carriers. We further assume that the dielectric relaxation time is smaller (~0.2 ms) compared to the emission time (10 ms or 20 ms) of gap states under the small ac signal.[37] To evaluate the impact of leakage current, reverse leakage current at different temperatures at a reverse bias of −1 V is provided in Table I for CdTe solar cells in the dark condition. The reverse leakage current increases as the temperature increases. The resistance-capacitance delay from the reverse leakage current can be quite small. If we consider the values from Ref. 37, it is estimated to be approximately in the order of 1 ms. Therefore, its impact can be neglected. It is noteworthy that only gap states near the Fermi level can bring changes in their occupancy, and thus bring significant contribution to the capacitance.

The time constant τ can be written as τ_p for holes. The hole emission rate, e_p which is inverse of the time constant can be stated as

TABLE I. Reverse leakage current versus temperature at reverse bias voltage ($V_R = 1$ V).

I_0(A)	Temperature (K)	I_m(A) (10 ms) 100 kHz	I_m(A) (20 ms) 100 kHz
-7.18×10^{-8}	313	7.45×10^{-6}	7.67×10^{-6}
-1.72×10^{-7}	323	8.39×10^{-6}	8.64×10^{-6}
-4.16×10^{-7}	333	9.46×10^{-6}	9.74×10^{-6}
-9.41×10^{-7}	343	11.12×10^{-6}	11.46×10^{-6}
-2.05×10^{-6}	353	13.04×10^{-6}	13.48×10^{-6}

$$e_p(T) = \frac{1}{\tau_p} = N_v(T)\sigma(T)v_{th}(T)\exp\left[-\left(\frac{E_t - E_v}{kT}\right)\right], \quad (1)$$

where τ_p is the time constant at a particular temperature for ionization of a deep trap in the part of the potential barrier where there are no free carriers; this is related to temperature, k is the Boltzmann's constant, E_t is the trap energy level, E_v is the valence band energy, N_v is the effective density of state in the valence band, $\sigma(T)$ is the capture cross section which depends on the temperature, $v_{\rm th}$ is the mean thermal velocity.

The temperature dependent cross-section can be stated as

$$\sigma(T) = \sigma_\infty \exp\left[-\left(\frac{E_\sigma}{kT}\right)\right], \quad (2)$$

where E_σ is the energy contribution from temperature-dependent cross-section and σ_∞ is a constant. Including Eq. (2) in Eq. (1) can be rewritten as

$$e_p(T) = \frac{1}{\tau_p} = N_v(T)\sigma_\infty v_{th}(T)\exp\left[-\left\{\frac{(E_t + E_\sigma) - E_v}{kT}\right\}\right]. \quad (3)$$

The Eq. (3) can be rewritten as

$$e_p(T) = \frac{1}{\tau_p} = N_v(T)\sigma_\infty v_{th}(T)\exp\left[-\left\{\frac{E_a - E_v}{kT}\right\}\right], \quad (4)$$

where $E_a = E_t + E_\sigma$ is the combination of trap energy and trap energy component of cross-section.

In the general case, the capacitance depends on time and temperature; if the temperature dependence is incorporated via the time-constant, the capacitance of an abrupt junction in Schottky diode may be put as

$$C^2(t,\tau) = \frac{q\varepsilon\varepsilon_0\{N_s + N_A{}^-\}}{2(V_{bi} - V)}, \quad (5)$$

where q is the electronic charge, ε is the permittivity of the material; ε_0 is permittivity in free space; N_s is the shallow acceptor concentration; V_{bi} is the built in potential, V is the applied bias voltage, and $N_A{}^-$ is the concentration of an ionized impurity varies as follows:

$$N_A^- = N_A\left[1 - \exp\left(-\frac{t}{\tau}\right)\right]. \quad (6)$$

Including the expression of $N_A{}^-$, Eq. (5) can be rewritten as

$$C^2(t,\tau) = \frac{q\varepsilon\varepsilon_0\left[N_s + N_A\left\{1 - \exp\left(-\frac{t}{\tau}\right)\right\}\right]}{2(V_{bi} - V)}. \quad (7)$$

We differentiate Eq. (7) first with respect to time and then with respect to τ, we get

$$2C\frac{dC}{dt} = \frac{q\varepsilon\varepsilon_0 N_A}{2(V_{bi} - V)}\left(\frac{1}{\tau}\right)\exp\left(-\frac{t}{\tau}\right), \quad (8)$$

$$\frac{\partial}{\partial\tau}\left(C\frac{dC}{dt}\right) = \frac{q\varepsilon\varepsilon_0 N_A}{4(V_{bi} - V)}\left[\left(-\frac{1}{\tau^2} + \frac{t}{\tau^3}\right)\exp\left(-\frac{t}{\tau}\right)\right]. \quad (9)$$

The temperature at which there is the maximum change in capacitance is obtained by equating Eq. (9) to zero, which gives

$$t = t_x = \tau_p. \quad (10)$$

Then by choosing sampling time t_x, we can determine τ_p, the hole time constant, which can be obtained from Eq. (9) corresponding to a definite temperature.

To find the cross-section and trap energy, we can choose temperatures T_{s1} and T_{s2} at time t_1 and t_2, respectively, in Eq. (4) to get two equations

$$\frac{1}{\tau_{p1}} = N_v(T)\sigma_\infty v_{th}(T)\exp\left[-\left(\frac{E_a - E_v}{kT_{s1}}\right)\right] \quad \text{and}$$
$$\frac{1}{\tau_{p2}} = N_v(T)\sigma_\infty v_{th}(T)\exp\left[-\left(\frac{E_a - E_v}{kT_{s2}}\right)\right], \quad (11)$$

whose solution gives E_t and σ_∞, where τ_{p1} and τ_{p2} are the time constants at temperatures T_{s1} and T_{s2}, respectively.

From Eqs. (8) and (10), we get the maximum temperature derivative for the capacitance for a concentration of majority carriers

$$N_A = \frac{4(V_{bi} - V)}{q\varepsilon\varepsilon_0}C_p\tau_p\frac{dC}{d\tau}. \quad (12)$$

The parameters, therefore, can be conveniently estimated from the capacitance change as a function of time when temperature is varied.

RESULTS AND DISCUSSION

Figure 1 shows the change in capacitance at different temperatures as a function of time measured using a 100 kHz signal after the reverse bias (−1 V) applied at time t = 0 ms for CdTe solar cells in the dark condition. As can be seen the capacitance increases and saturates within 10 ms at 300 K. At higher temperatures capacitance increases rapidly in the beginning (∼10 ms) and then slowly increases till 50 ms (range of our measurements). It is clear that the initial charge states of the majority carrier traps are immediately filled by

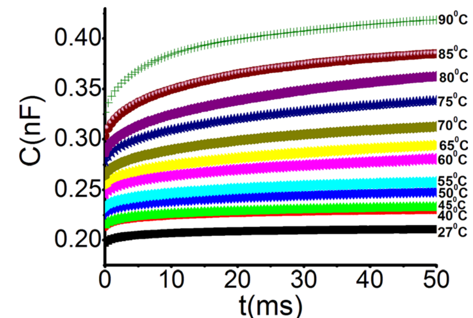

FIG. 1. Time dependence of the capacitance measured at 100 KHz when a reverse bias ($V_r = 1$ V) was applied at time, t = 0 for CdTe solar cells.

the applied reverse bias (-1 V) in the depletion region and tend to detrap with time at that particular temperature thereby changing the capacitance. The energy band diagram of trapping and detrapping is shown in Figure 2 of CdS/CdTe heterojunction. At a reverse bias of 1 V and at $t=0$ traps in the depletion region are completely filled (Figure 2(a) and at $t=\infty$ (50 ms in our case) the device comes to an equilibrium value once the detrapping process ends (Figure 2(b)) shrinking the depletion region width. The capacitance transients are shown in Figure 1.[38] When the device temperature was varied from 300 K to 363 K at a constant frequency under reverse bias, the trapped carriers in the p-type depletion layer were thermally excited out. This led to an increase of junction capacitance with increasing temperature. The change in capacitance was sampled at both 10 ms and 20 ms.

To obtain a spectrum tangents were drawn to the curves at the points corresponding to the chosen times, for instance 10 ms and 20 ms, and the slope dC/dt was plotted as a function of temperature. Then by choosing t we can determine τ_p, which is shown by Eq. (4) that corresponds to a definite temperature. By substituting τ_p into Eq. (11) gives the corresponding values for E_a and σ_∞ with $\tau_{pl}=10$ ms and $\tau_{p2}=20$ ms and the temperatures T_{sl} and T_{s2} corresponding to the peak values in dC/dt. If σ_∞ is known, then E_a can be found from Eq. (4); if on the other hand σ_∞ is unknown, we can choose t successively as equal to τ_{pl} and τ_{p2} to get two equations in Eq. (11) whose solution gives E_a and σ_∞. The concentration of majority carriers N_A is given by Eq. (12), in which C_p corresponds to the maximum slope.

As evident from the TDCS spectrum, with the rate of change of capacitance (Figure 3) as a function of temperature a significant change was observed when $T=T_s$. In other

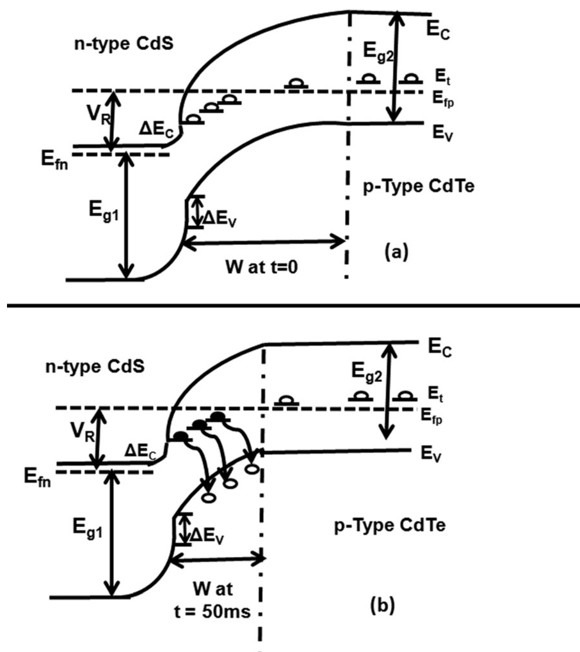

FIG. 2. Energy band diagram of CdTe solar cell for reverse bias conditions (a) at $t=0$, (b) at $t=50$ ms. The symbols represent their usual meanings. ΔE_c and ΔE_v show the discontinuities (offsets) of the conduction and valence bands, respectively, W is the depletion width, V_R is the reverse bias voltage, E_{g1} and E_{g2} are the energy band gaps of CdS and CdTe, respectively, E_{fp} and E_{fn} are the quasi Fermi levels and E_t is the trap energy level.

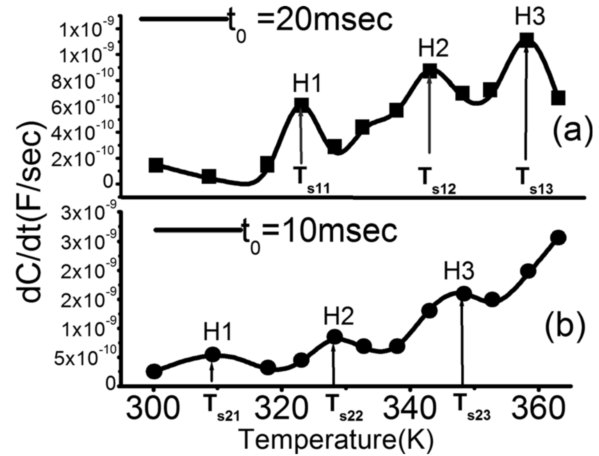

FIG. 3. Rate of change of capacitance measured at different temperatures at 100 KHz in reverse bias ($V_r=1$ V) for CdTe solar cells.

words, when E_f crosses E_t, the TDCS peak amplitude changes with the steady application of reverse bias, since the peak height is proportional to the number of filled/emptied traps. Typically, this requires the use of emptying times for majority carriers (holes) that are high enough to empty most of the traps. In this study, using a time range from 0 ms to 50 ms, a significant change in peak height was observed. The peaks observed at sampling time 20 ms and 10 ms are shown in Figures 3(a) and 3(b), respectively.

The peaks designated as H1, H2, and H3 indicate that the detected traps were completely emptied within 10 ms (Figure 3(b)). For next 10-20 ms, there is a significant change in peak height (Figure 3(a)) for detected traps. Peaks also shifted with time indicating that the traps are of deep intrinsic/impurity defects. Using this approach, three positive signals in TDCS correspond to majority traps were observed. The corresponding values of capture cross-section also suggest that they arise from deep level defects. The peak location of majority traps did not change at reverse bias voltages were increased or decreased.

The activation energy was extracted from the peak from TDCS spectra. The temperature of maximum value dC/dt curve, Ts_{11} for H1 at 10 ms gives the estimate of the thermal activation energy of the majority carrier trap energy levels. The total capacitance change around each T_{s11} and T_{s21} for H1 at 10 ms and 20 ms gives the concentration of carriers trapped at that level. Employing the TDCS measurements at 300 K deep levels can be detected assuming a maximum detectable thermal emission rate due to time constant. Thus, this method demonstrates that the capacitance change due to emptying of majority-carrier traps in the depletion region can be used to characterize the deep levels.

The trap energy level can be simply estimated from TDCS plot of the reverse bias voltage. Each spectrum in TDCS consists of three peaks representing three deep energy traps H1, H2, and H3 (Figure 3). These plots measure activation energy of 0.65 eV for trap H1, 0.52 eV for trap H2, and 0.80 eV for trap H3. The detailed estimated values for the trap levels are listed in Table II.

The defect H1 is attributed to doubly ionized cadmium vacancy (V_{Cd}^{2-}) substitutions with energy level $E_v+0.65$ eV

TABLE II. Temperature dependent values of various parameters determined from C-V characteristics from Figure 3.

Trap level	T_{s1}(K) corr. to peak in dC/dt when t = 10 ms	T_{s2}(K) corr. to peak in dC/dt when t = 20 ms	N_A (cm^{-3})	E_a (eV)	σ_∞ (cm^2)
H1	313	323	1.4×10^{11}	0.65	3×10^{-13}
H2	328	343	2×10^{11}	0.52	1×10^{-15}
H3	348	358	0.3×10^{12}	0.80	4×10^{-12}

and cross-section $(\sigma_t) \sim 3 \times 10^{-13}\,cm^2$. Rakhshani *et al.* detected this trap in CdTe thin-film solar cells by PICTS,[20] with its $\sigma_t \sim 4.8 \times 10^{-13}\,cm^2$. Moreover, Ringel *et al.* also observed the same defect due to $V_{Cd}{}^{2-}$ with $\sigma_t \sim 8.2 \times 10^{-16}$ by DLTS during the annealing process after the $CdCl_2$ dip.[12] Also, this is consistent with V_{Cd} and/or Cl diffusion from the CdTe surface into the bulk as a result of the 400 °C anneal. Since Cl ions are known to be readily form defect complexes with cadmium vacancies to form deep and shallow levels, it is likely that the $E_v + 0.64$ eV trap defects.[21,22]

The H2 seems to be the signature of (trap energy level $E_v + 0.52$ eV and $\sigma_t \sim 1 \times 10^{-15}\,cm^2$) Cu related deep level defect. This is in good agreement with activation energy (494 ± 9) meV determined by Admittance Spectroscopy and also with activation energy (552 ± 10) meV determined by back barrier height, assuming thermionic emission mechanism from current-voltage characteristics.[15] It was shown that the observed peak was a deep level due to Cu and the peak appears when Cu is added to the back contact formation process.[15] Note that the annealed Cu-evaporated back contact with Cu doped ZnTe in carbon conductive paste of CdTe thin-film solar cells are being investigated here. Seymour[27] observed the activation energies 0.52 eV and 0.54 eV with cross-sections $7 \times 10^{-12}\,cm^2$ and $9 \times 10^{-12}\,cm^2$, respectively, by using admittance spectroscopy from a number of CdTe solar cells that were with Cu back contact and $CdCl_2$ treatment similar to ours. It is, therefore, reasonable to assume that $Cu_i{}^{2+}$ is likely to be present in our devices (∼0.55 eV) as Cu was evaporated during back contact formation. We had reported this trap for Cu evaporated samples earlier.[9]

The H3 level with energy value $E_v + 0.80$ eV and $\sigma_t \sim 4 \times 10^{-12}\,cm^2$ obtained in the cells absorber layer was caused by the positive $Cd_i{}^{2+}$ interstitial defects. Since the deep level associated with doubly charged cadmium vacancy was observed, it may be postulated that vacancy formation was suppressed, and the creation of interstitial favored in our devices. Rakhshani and Makdisi[25] have investigated the trap level with activation energy (0.88 eV) and $\sigma_t \sim 1.1 \times 10^{-11}\,cm^2$ in CdTe thin-film solar cells. In an earlier work,[9] we also observed this trap level. In addition, Rakhshani *et al.*[20] verified hole trap with value $E_v + 0.80$ eV and $\sigma_t \sim 3.9 \times 10^{-13}\,cm^2$ by using PICTS. Similarly, studies involving the thermally stimulated conductivity technique[26] revealed that traps in depletion region appeared most frequently in material grown at high Cd pressure.

From the Table II, it was observed that the estimated the carrier concentration in CdTe seems to be lower than the reported in the literature[27] ($N_A = 10^{14}\,cm^{-3}$). Although the multiple dopant states are the most fundamental parameters to be controlled in device processing they make it difficult to determine each state's concentration, and its corresponding doping level. While a high copper impurity concentration was observed ($N_{Cu} = 10^{17}\,cm^{-3}$),[39] a much less hole density was reported (10^{14}-$10^{15}\,cm^{-3}$)[27] for the same samples. Note that published experimental values of p or N_A of thin film CdTe are extracted from C-V measurements. By calculating with Eq. (7) in Ref. 40 and considering $N_V = 1.8 \times 10^{18}\,cm^{-3}$ (Ref. 41), $N_A = 1.6 \times 10^{14}\,cm^{-3}$, $g_A = 4$, and E_A-$E_V = 0.55$ eV (Ref. 15), our estimation of $p = 2.2 \times 10^{11}\,cm^{-3}$ is consistent with experimental value from the calculated data. It also confirms that if Cu is present in interstitial form, p may be few orders lower than the acceptor concentration. Same calculations can be done for doubly ionized vacancy of cadmium. As a result, the band bending at the junction is small due to lower concentration of hole in p-type CdTe solar cell.

We have summarized the reported defect types, activation energy E_a and capture cross-section σ_∞ in Table III along with our data observed from the TDCS technique. Most of the other studies with different techniques revealed that traps related to cadmium vacancy in depletion region appeared most frequently in CdTe material grown at high Cd pressure.[10,13,14,20–22] The deep traps related to copper defects appeared due to excess of copper in the back contact.[9,15,27] It can be seen that TDCS results are compatible to other measurement techniques. Since TDCS is rather a simpler technique it can be employed to quickly identify the deep levels in CdTe Solar cell before more extensive techniques like DLTS are used. While other techniques like J-V-T can be employed to identify the deep level defects minor errors can be introduced due to field driven conduction in addition to trap-assisted conduction. Besides, accurate calculation of defect concentration and capture cross-section may not be possible.[9] Therefore, we believe for quickly evaluation of deep defects TDCS seems to be a more effective tool.

TABLE III. Role of capture cross-section energy of defects compared with other studies in CdTe solar cells. The symbols carry their usual meaning as defined earlier.

	This work (TDCS)		Other techniques (Refs.)	
Trap type	Activation energy, E_a (eV)	Cross-section σ_∞ (cm^{-2})	Activation energy E_a (eV)	Cross-section σ_∞ (cm^{-2})
$V_{cd}{}^{2-}$	0.65	3×10^{-13}	0.63 (DLTS[10])	1.0×10^{-15}
			0.64 (DLTS[12])	8.2×10^{-16}
			0.65 (PICTS[20])	3.0×10^{-13}
			0.64 (DLTS[21,22])	…
$Cu_i{}^{2+}$	0.52	1×10^{-15}	0.57 (J-V-T[9])	…
			0.50 (AS[15])	8.42×10^{-12}
			0.52-0.54 (AS[27])	7–9×10^{-12}
$Cd_i{}^{2+}$	0.80	4×10^{-12}	0.89 (J-V-T[9])	…
			0.75 (DLTS[10])	4.0×10^{-14}
			0.80 (PICTS[20])	3.9×10^{-13}
			0.88 (PICTS[25])	1.1×10^{-11}

CONCLUSIONS

We have presented TDCS measurement at fixed reverse bias to estimate various trap characteristics from plot of temperature-dependent capacitance transients in n^+-CdS/p-CdTe solar cells. We have successfully derived the activation energies with experimentally measured data. By using TDCS method, we can find single or multiple defects. We analyzed three deep level traps using TDCS in CdTe solar cells with a copper-evaporated back contacts. Based on the capture cross-section and a literature surveys, we attributed with $E_t = 0.65$ eV, 0.80 eV is due to singly and doubly ionized Cd vacancy and one trap with $E_t = 0.52$ eV is due to Cu-related deep level. The TDCS method turned out to be superior and fast technique to estimate deep defect characteristics in CdTe solar cells.

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