phys. stat. sol. (a) **129**, 291 (1992)

Subject classification: 73.60 and 85; S10.1

Microelectronics Research Center, Department of Physics, New Jersey Institute of Technology, Newark[1]) *(a) and*
David Sarnoff Research Center, Princeton[2]) *(b)*

Current–Voltage Measurements of Thermally Grown SiO_2 Films on Etched Silicon Surfaces

By

V. V. RAMANA (a), N. M. RAVINDRA (a), and M. F. LEAHY (b)

Experimental results of the current–voltage ($I-U$) measurements of thermally grown thin SiO_2 films on virgin and plasma etched silicon surfaces are reported. The $I-U$ measurements include static $I-U$ and dynamic $I-U$ or time dependent dielectric breakdowns (TDDB). The structures used in this study are Al/Polysilicon/SiO_2/Si/Al capacitors fabricated on n-Si and p-Si substrates. These capacitors, ranging in areas from 0.001 to 0.05 cm^2, were made using various plasma process conditions and etch reactors. Two different processing sequences are presented. The first process uses a sacrificial oxidation step after the initial plasma exposure (grow a thermal oxide, strip the oxide, and regrow an oxide). The second does not include the sacrificial oxidation. A constant current probe technique is used for evaluating the breakdown behavior of MOS capacitors. 1 μA is used as the standard test current for the analysis. Based on preliminary studies for the control samples, the density of defects is found to be $\approx 2\ cm^{-2}$ for the former case and $4\ cm^{-2}$ for the latter one. Overall, the results obtained show that sacrificial oxidation improves oxide integrity, yields higher breakdown fields, and minimizes defect densities.

Experimentelle Ergebnisse von Strom–Spannungs ($I-U$)-Messungen an thermisch gewachsenen dünnen SiO_2-Schichten auf jungfräulichen und plasmageätzten Siliziumoberflächen werden mitgeteilt. Die $I-U$-Messungen schließen statische $I-U$ und dynamische $I-U$ oder zeitabhängigen dielektrischen Durchbruch (TDDB) ein. Die dabei benutzten Strukturen sind Al/Polysilizium/SiO_2/Si/Al-Kondensatoren, mit Flächen von 0,001 bis 0,05 cm^2, die unter verschiedenen Plasmaprozeßbedingungen und Ätzreaktoren hergestellt werden. Zwei verschiedene Prozeßfolgen werden dargestellt. Der erste Prozeß benutzt eine Opferoxydationsstufe nach der Plasmaanfangsexposition (Wachstum eines thermischen Oxids, Oxidbeseitigung und erneutes Wachstum eines Oxids). Der zweite schließt keine Opferoxydation ein. Eine Konstantstromsondentechnik wird für die Bestimmung des Durchbruchsverhaltens der MOS-Kondensatoren benutzt. Es wird 1 μA als Standardsondenstrom für die Analyse verwendet. Auf der Grundlage vorhergehender Untersuchungen für die Kontrollproben wird die Defektdichte zu $\approx 2\ cm^{-2}$ im ersteren und $4\ cm^{-2}$ für den letzteren Prozeß gefunden. Insgesamt zeigen die erhaltenen Ergebnisse, daß Opferoxydation die Oxidbeschaffenheit verbessert, höhere Durchbruchsfelder liefert und die Defektdichten minimiert.

1. Introduction

In the past, the processes applied to semiconductor integrated circuit (IC) fabrication were primarily thermal processes such as oxidation following crystal growth, diffusion, and metallization. Application of plasma discharges to IC fabrication to obtain improved results at reduced substrate temperatures was first attempted in the 1960s. IC fabrication technology

[1]) Newark, NJ 07102, USA.
[2]) CN 5300, Princeton, NJ 08543, USA.

has moved from wet etching to dry etching. Dry etching processes are generally cleaner than wet processes and the yield and reliability of ICs containing micropatterns can be increased.

Today state-of-the-art IC manufacture depends on the mass replication of tightly controlled, micron-sized features in a variety of materials. Plasma etching has become central to this process because it is the only current technology that can do this job efficiently and with high yield [1]. In etching the materials below a resist mask by the traditional wet method, it is difficult to remove the reaction products when the patterns are situated close to each other. Undercutting is also a difficult problem; thus formation of micropatterns is not an easy task with the use of wet-chemical techniques. Use of low-pressure plasma facilitates removal of the reaction products and minimizes the problem of undercutting. It accelerates the etching ions by the electric field induced; this is done, for example, in reactive ion etching (RIE). The key issues pertinent to an etch process are selectivity and anisotropy with minimal damage and contamination. The metal-oxide-semiconductor (MOS) capacitor is most powerful for investigating nearly all the electrical properties of the MOS system. The MOS capacitor is useful in such studies because any change in processing that improves the electrical properties of the MOS capacitor makes the same improvement on the actual device [2]. Thus the simplicity and the versatility of the MOS capacitor can be exploited with confidence for optimizing integrated circuit processing.

2. Experimental Details

MOS capacitors with areas in the range of 0.001 to 0.05 cm^2 were fabricated on boron-doped p-type [100] silicon wafers with 2 Ωcm resistivity (experiment 1). All the wafers except the controls are exposed to various Si-etch plasma treatments. The cleaning procedure consisted of the conventional RCA technique followed by a HF dip and a thorough rinsing with deionized water. The gate oxides are thermally grown at 800 °C on these etched Si surfaces to a thickness of approximately 24 nm. The oxide thickness was measured on several points of the wafer by using an ellipsometer. A 500 nm thick polycrystalline silicon (polysilicon) film was deposited in a chemical vapor deposition system at 600 °C using SiH_4. Subsequent phosphorus diffusion of the polysilicon resulted in a 15 Ω/□ sheet resistivity. A 500 nm thick Al film was deposited on the polysilicon. The backside of the wafer is evaporated with aluminum containing 1% Si for a contact, followed by post-metal anneal for 30 min at 450 °C in forming gas (10% H_2 in N_2).

The fabrication of the second set of n-type capacitors (experiment 2) is similar to experiment 1 and includes some additional steps. In this experiment, the additional step is the sacrificial oxidation, to reduce the possible damage induced to silicon substrate during plasma etching. The gate oxide thickness for this experiment is 25 nm. The fabrication steps of the capacitors are shown in Fig. 1 for experiment 1 and experiment 2. The cross section of the capacitor is shown in Fig. 2a. A schematic of an array of MOS capacitors ranging in the area from 0.001 to 0.05 cm^2 on a silicon wafer is shown in Fig. 2b.

The following electrical measurements have been employed to investigate the effects of plasma etching: dynamic current–voltage (I–U), time dependent dielectric breakdown (TDDB), and static current–voltage (I–U) characteristics.

It is well known that nondestructive measurements such as dynamic current–voltage (I–U) characteristics or TDDB can be satisfactorily carried out by a constant current probe technique. The capacitors were biased with a constant current to accelerate breakdown.

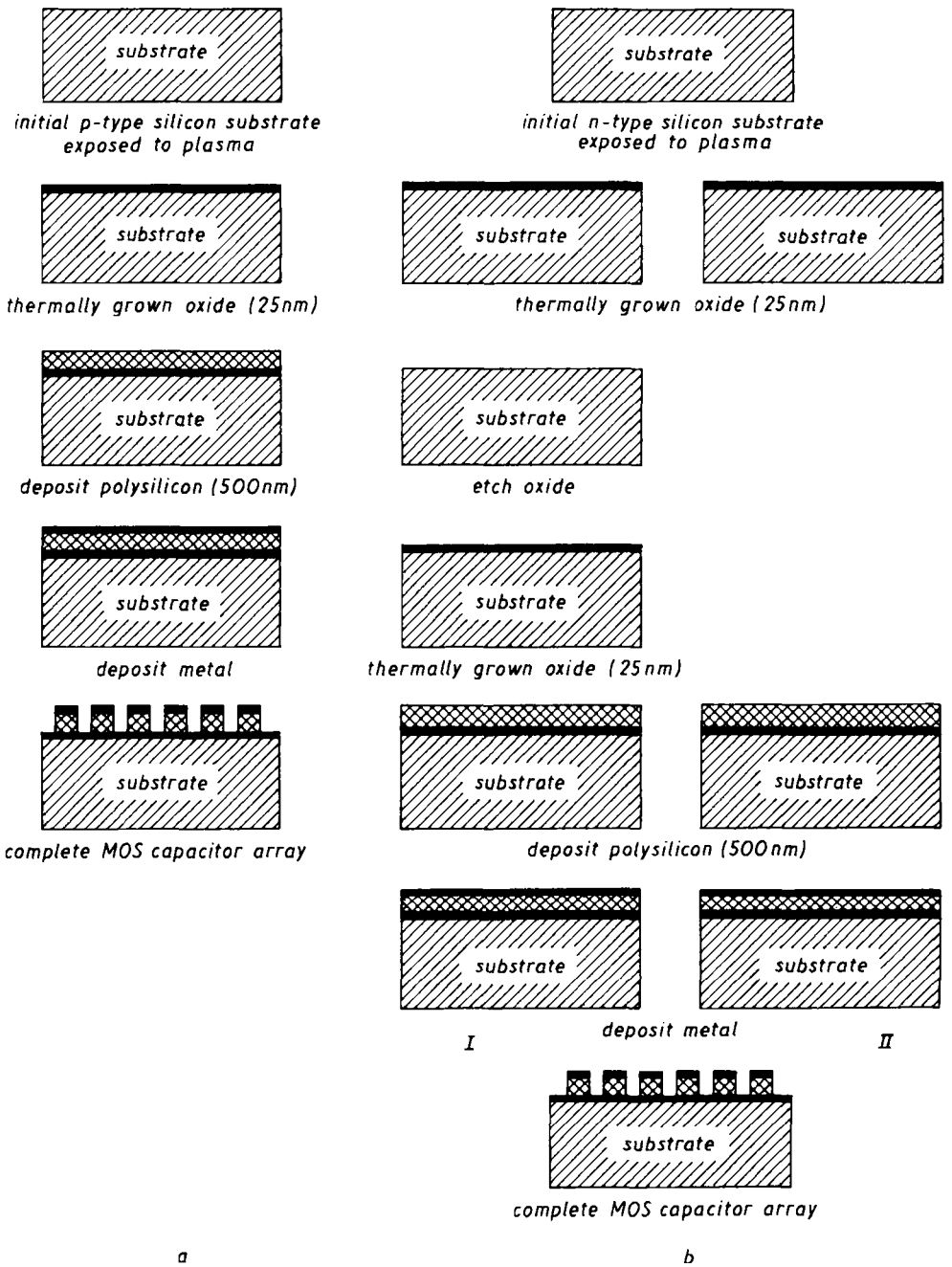

Fig. 1. Fabrication steps. a) Experiment 1, b) experiment 2 (process steps of the capacitor I with sacrificial oxidation, II without sacrificial oxidation)

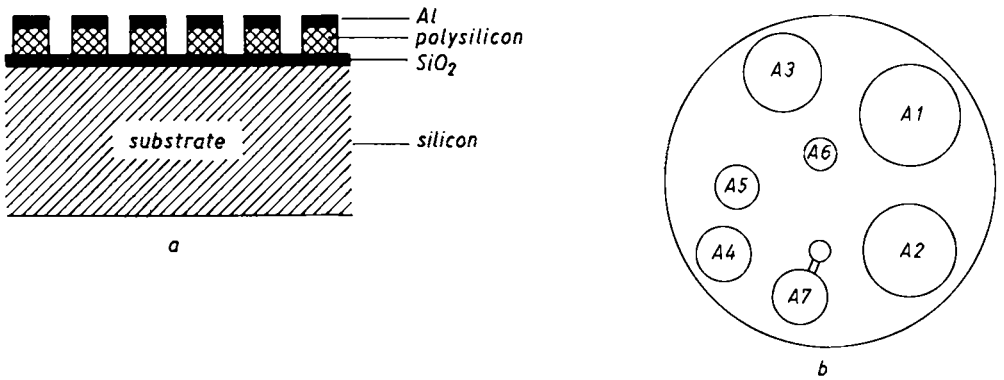

Fig. 2. a) Cross section of the capacitor, b) schematic of an array of capacitors with different areas on a wafer

This technique was first described by Harari [3]. Basically the technique consists of permitting a constant current [4 to 6] into a capacitor until breakdown occurs. The technique is nondestructive because the choice of constant current is limited by the actual Fowler-Nordheim tunneling (FNT) component of the current. This FNT component of the current is a function of the oxide thickness [7]. Contact to the counterelectrode is made by a probe placed directly on top of the capacitor. A 4-inch Si wafer contains approximately 300 capacitors of each area.

Breakdown measurements were performed using a Keithley automatic probe tester. The voltage at which the capacitor breaks down is the breakdown voltage for a test current of 1 μA. A set of capacitors is tested each time and the corresponding breakdown voltages for that set are measured. The test cycle is repeated and complete testing of the 300 sets of capacitors on a wafer can be accomplished in about 90 min. All measurements reported here were carried out at room temperature. In the analysis, percentage good is defined as $\geqq 0.8E_{max}$ where E_{max} is the maximum breakdown field.

The breakdown voltages are recorded for all the MOS structures processed under different conditions and process variables. The defect densities were calculated using the equation [6, 8]

$$\varrho = -\frac{\ln P}{A}, \tag{1}$$

where ϱ is the defect density in cm^{-2}, A the area of a capacitor dot in cm^2, and P the fraction of the number of capacitors with $E \geqq 0.8E_{max}$ or percentage good.

The static I–U measurements were performed using a Keithley 236/237 source measure unit. The technique consists of the application of a ramp voltage to a capacitor until breakdown occurs. The voltage applied is in the range of 0 to 40 V. The contact to the counterelectrodes is made by means of a probe placed directly on top of the capacitor. The breakdown was accompanied by a rapid increase in current across the MOS capacitor.

3. Results and Discussion

The results of the I–U measurements for the experiment 1 under various processing conditions in different reactors are explained below:

1. CF_2Cl_2: In CF_2Cl_2 (Freon 12) plasma for 1, 3, and 10 min, the general trend is that the % good is not systematic with the increase in time of exposure to plasma as shown in

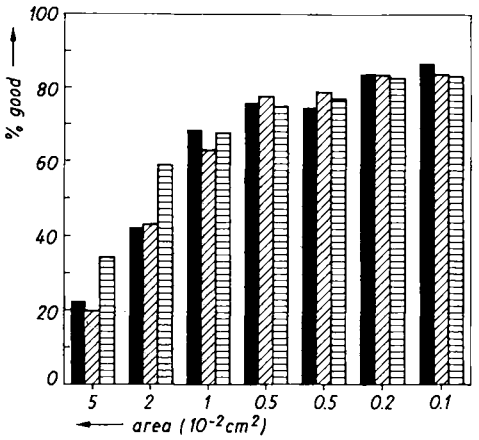

Fig. 3. CF_2Cl_2 plasma for 1 (black columns), 3 (first hatched columns), and 10 min (second hatched columns), experiment 1

Fig. 3. For the largest area capacitor (0.05 cm^2), % good is low which means that the capacitor has large number of defects like pinholes and contaminants.

The defect density numbers are in the range of 18 to 30 cm^{-2} for the capacitor areas ranging from 0.05 to 0.001 cm^2. The plot of $-\ln P$ versus area is a straight line. The slope of the line yields the defect density ϱ. We can see that the density of defects is high for large area capacitors.

2. High pressure diode: In high pressure diode (Tegal 1513) system, three wafers were exposed to plasma for 10, 30, and 60 s. The etching gases are C_2F_6 + CHF_3 + He. The pressure was 2.3 Torr. This system etches silicon at 250 nm/min. As the time of exposure to plasma increases, the % good decreases for all areas as shown in Fig. 4. The defect densities are low for lower times. As the time of exposure increases the defect densities also increases.

3. MRC 720 oxygen plasma: The MRC 720 is a magnetically-enhanced RIE system. The variable in the experiments is the RF power – 100, 200, 500, 1000, and 1500 W. The % good generally decreases with the increase in power for 100, 200, and 500 W as shown in

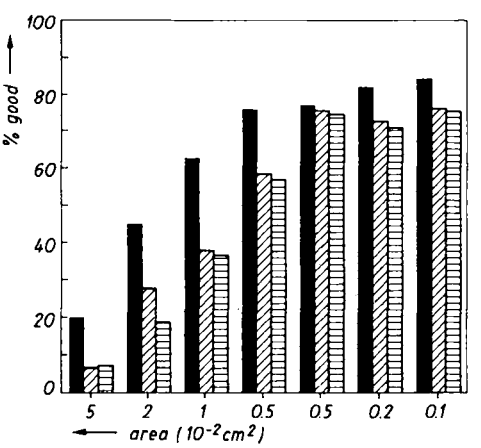

Fig. 4. High pressure diode for 10 (black columns), 30 (first hatched columns), and 60 s (second hatched columns), experiment 1

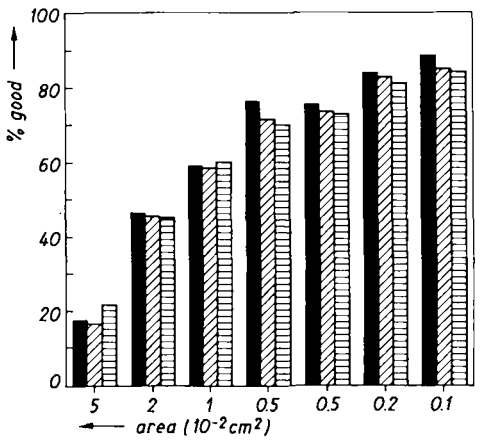

Fig. 5

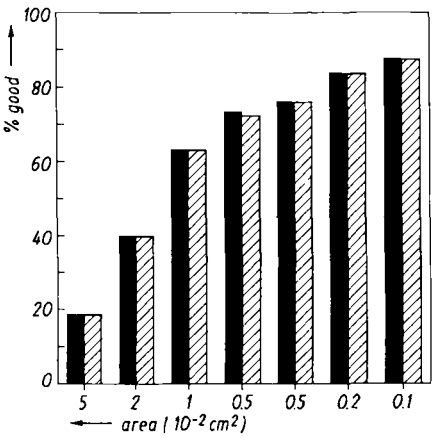

Fig. 6

Fig. 5. MRC Oxygen Plasma for 100 (black columns), 200 (first hatched columns), 500 W (second hatched columns), experiment 1

Fig. 6. Control: wafer No. 23 (black columns), No. 25 (hatched columns), experiment 1

Fig. 5. We found that at 1000 and 1500 W, 90% of the capacitors break down below 2 MV/cm.

4. Controls/no treatment: The characteristics of the controls are identical as shown in Fig. 6. In general, the yields were low for large area capacitors.

Defect density (ϱ) is expected to depend on the quality of the starting substrate, cleanliness of the processing environment, and the oxidation/annealing conditions. In particular, Czochralski silicon usually contains significant amounts of oxygen which can form

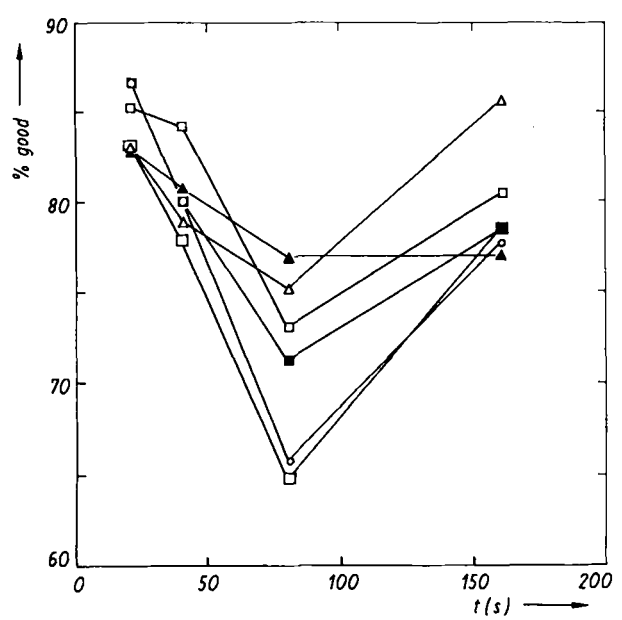

Fig. 7. High pressure diode for 20, 40, 80, and 160 s, Area: □ A1 = 0.05, ○ A2 = 0.02, ▲ A3 = 0.01, △ A4 = 0.005, ■ A5 = 0.002, □ A6 = 0.001 cm^2, experiment 2

precipitates depending on the oxygen concentration and the temperature of the various processing steps [9]. These precipitates, which can be incorporated into the oxide during oxidation, are believed to be the main source of the oxide defects in thermal oxides [6]. Therefore, defect density can be reduced by proper substrate preparation, including an intrinsic gettering process in which the surface region of the silicon is made free of oxygen followed by nucleation and precipitation of the oxygen in the bulk of the wafer.

Based on the results in experiment 1, we investigated further the effects of plasma etching in silicon. In experiment 2, we added a sacrificial oxidation. The process variables in this experiment were reactor type, time, and power.

The results of the *I–U* measurements of experiment 2 are discussed below:

1. High pressure diode: For the high pressure diode system, the time of exposure of the Si wafer to plasma is 20, 40, 80, and 160 s. From Fig. 7, we see that, as the time of exposure to plasma increases, the % good decreases and subsequently increases. This behavior is independent of the area of the capacitor.

2. MRC oxygen plasma: For MRC the variable chosen is the power in the range of 200, 400, 800, and 1600 W. From the breakdown measurements, it is seen that as the power increases, the % good increases, goes to a maximum and subsequently decreases. This is true for all areas as shown in Fig. 8.

3. Controls/no treatment: In the controls, we can evaluate the role of the sacrificial oxide. In general, sacrificial oxide helps in decreasing the defect densities, increasing E_{max} and improving the oxide integrity.

From the breakdown results, the maximum breakdown field obtained for a test current of 1 μA is 8.5 MV/cm for a control which has seen the sacrificial oxide versus 8.0 MV/cm for the control sample without sacrificial oxidation, as shown in Fig. 9. The low field breakdowns are 8% for the former and 12% for the latter one. For the high pressure diode system, the breakdown fields are low in the range of 4.0 to 7.5 MV/cm. For MRC system,

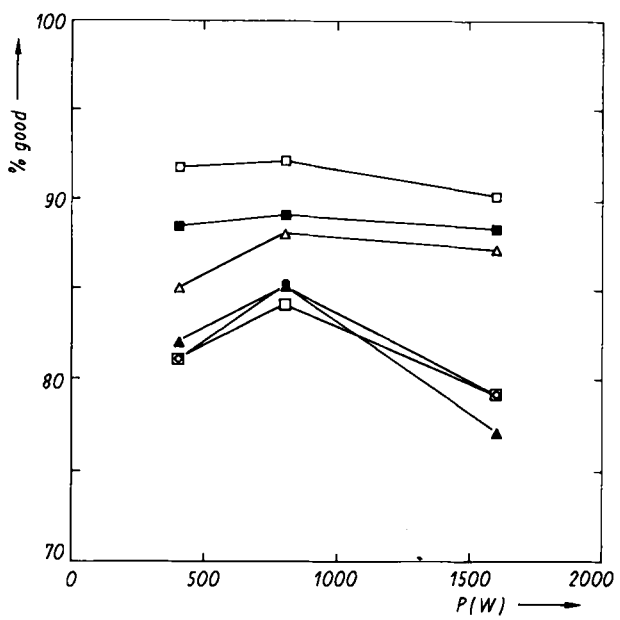

Fig. 8. MRC oxygen plasma for 400, 800, and 1600 W. For symbols see Fig. 7; experiment 2

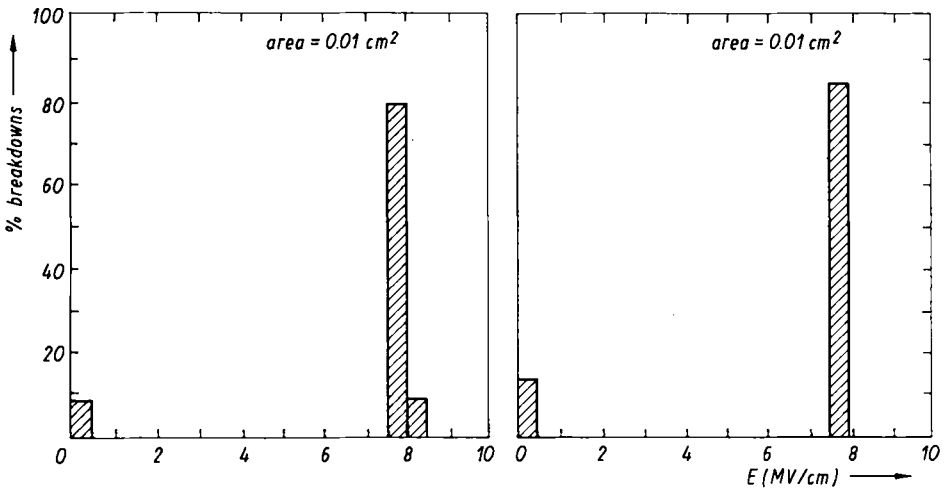

Fig. 9. Controls. a) Wafer No. 19 has seen a sacrificial oxide, b) wafer No. 20 is a routine process

at 400 W, the low field and high field breakdowns are 10% and 83%, respectively, for the sample which has seen the sacrificial oxidation, 23% and 72%, respectively, for the sample which has not seen the sacrificial oxidation. The maximum breakdown field for this case is 8 MV/cm.

From these experimental results, we conclude that the breakdown fields of the controls are better than the breakdown fields of the plasma-etched wafers. In this analysis, the large area capacitors were found to have very low breakdown fields. This may be due to pinholes and contaminants. For breakdown measurements, it is ideal to have small capacitors wherein the defects in the oxide will be low.

From the above results, we can say that the role of sacrificial oxide is very important in VLSI processes. The results have led to the following conclusions. The high pressure diode system uses C_2F_6, CHF_3, and He. Considering the possible chemical reactions, fluorine can also be incorporated into the surface of the silicon wafer. Many processes inadvertently introduce fluorine into the gate oxide. The effect of fluorine on electrical breakdown of SiO_2 films was investigated by many workers [10 to 13]. Of particular interest was the work done by Shioya et al. [10] and Wright and Saraswat [11]. Shioya et al. concluded that hydrogen is not a cause of the degradation of the breakdown field because hydrogen does not appear to diffuse into the oxide after annealing. Fluorine does not degrade the breakdown field of the oxide when it is only adsorbed on the surface of the oxide. However, fluorine partially destroys the structure of the oxide after annealing. It is considered that the current easily flows through the bonding of fluorine and Si atoms. It was hypothesized that the fluorine was responsible for degrading the oxide by breaking Si–O bonds and forming Si–F bonds.

According to Wright and Saraswat, fluorine was found not to be a mobile ion in the oxide. High doses of fluorine were found to increase flat-band voltages. Possible explanations for this include a negative fixed charge at the silicon–silicon dioxide interface and a strained interfacial bond. No gross degradation in oxide quality has been found for quantities of fluorine larger than that reported in [10]. The work reported by Shioya et al. showed a gross degradation in the breakdown field for silicided gates. When a layer of nitride was

deposited between the gate oxide and the gate, the breakdown distribution improved. High levels of fluorine have been found to increase the film thickness and lead to additional traps. Fluorine was found to have caused an improvement in interfacial properties. The breakdown field showed a small degradation with the highest fluorine concentration. These results indicate that devices with fluorine-enriched oxide will not show degradation as long as the concentration is sufficiently low.

4. Conclusions

The current–voltage measurements of the samples in the present study show some interesting results. The results of experiment 1 and experiment 2 are discussed. In experiment 1 which consists of p-Si as the substrate, two processes, particularly MRC and high pressure diode (HPD) showed the effects of the plasma. In HPD, time is the variable parameter, while in the MRC it is the power in the RIE reactor. In both cases, we see the decrease in % good as the power and time of exposure of Si wafer to plasma increases. From these observations, we conclude that at high powers, the crystalline silicon substrate may be damaged due to bombarding of high energy ions. The breakdown fields decrease for both the cases.

The breakdown results of experiment 2, which consists of n-Si as the substrate are shown in Table 1. The role of sacrificial oxidation is clearly seen in the I–U characteristics of the samples. In Tegal system where time is the variable parameter as the time of exposure to plasma increases, the % good decreases and reaches a minimum at 80 s and increases. This trend is true for all areas of the capacitors irrespective of the sacrificial oxidation step. For MRC oxygen plasma, the variable parameter is power. As the power increases, the % good increases and reaches maximum at 800 W and subsequently decreases. This is the case for small areas of capacitors including those that have seen the sacrificial oxidation step. This leads us to believe that there exists an optimum power and time in order to yield reliable devices. The effect of fluorine on oxide breakdowns is ambiguous.

Table 1
Results of I–U measurements of experiment 2 for an area of 0.001 cm^2

process		maximum breakdown field E (MV/cm)	
		without sacrificial oxide	with sacrificial oxide
controls/no. treatment		8.5	8.7
		8.7	9.0
high pressure diode	time (s)		
	20	4.9	7.3
	40	6.4	7.3
	80	6.8	7.8
	160	7.8	8.1
MRC oxygen plasma	power (W)		
	400	8.6	8.7
	800	8.3	8.9
	1600	8.6	8.8

Acknowledgements

This work was supported by a contract from SEMATECH through the Semiconductor Research Corporation and David Sarnoff Research Center (Contract No. 88-MC-504).

References

[1] T. SUGANO, Applications of Plasma Processes to VLSI Technology, Wiley 1985.
[2] E. D. NICOLLIAN and J. W. BREWS, MOS (Metal Oxide Semiconductor) Physics and Technology, Wiley, 1982.
[3] E. HARARI, J. appl. Phys. **49**, 2478 (1978).
[4] D. R. WOLTERS and J. J. VAN DER SCHOOT, Phil. J. Res. **40**, 115 (1985).
[5] D. R. WOLTERS and J. J. VAN DER SCHOOT, Phil. J. Res. **40**, 137 (1985).
[6] C. M. OSBURN and D. W. ORMOND, J. Electrochem. Soc. **119**, 591 (1972).
[7] J. ZHAO and N. M. RAVINDRA, Mater. Res. Soc. Symp. Proc. **159**, 217 (1990).
[8] C. M. OSBURN and D. W. ORMOND, J. Electrochem. Soc. **119**, 597 (1972).
[9] S. M. SZE, VLSI Technology, McGraw-Hill, Ser. Electrical Engineering (1988).
[10] Y. SHIOYA, S. KAWAMURA, I. KOBAYASHI, M. MAEDA, and K. YANAGIDA, J. appl. Phys. **61**, 5102 (1987).
[11] P. J. WRIGHT and K. C. SARASWAT, IEEE Trans. Electron Devices **36**, 879 (1989).
[12] I. C. CHEN, S. E. HOLLAND, and C. HU, IEEE Trans. Electron Devices **32**, 413 (1985).
[13] K. OHYU, T. ITOGA, Y. NISHIOKA, and N. NATSUAKI, Japan, J. appl. Phys. **28**, 1041 (1989).

(Received May 7, 1991; in revised form October 9, 1991)