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Formation of $TiSi_2/n^+/p$-Silicon Junctions by Implantation through Metal Technique

By

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Experimental studies of the formation and electrical characterization of $TiSi_2/n^+/p$-Si shallow junctions are presented. The formation of shallow n^+-p junction, by ion implantation of As^+ through Ti films evaporated on p-Si substrates followed by rapid thermal annealing (RTA) and conventional furnace annealing, is performed in these experiments. Structural techniques such as secondary ion mass spectroscopy (SIMS) and Rutherford backscattering (RBS) experiments are employed to characterize these devices. RUMP simulations are deployed to analyze and interpret the RBS data. Temperature dependent current–voltage measurements of these junctions are performed in the temperature range of 250 to 400 K. Interpretations for these results are sought from conventional p–n junction theory.

1. Introduction

In integrated circuit manufacturing, the scaling down of device features (large packing density and hence increased complexity on the chip) has been motivated by the promise of faster operating speed and less power consumption. With the reduction in device size, the sheet resistance contributing to RC time delay increases [1]. Refractory metal silicides have gained importance for very large integrated circuit application as low sheet resistance source/drain and gate interconnects, and ohmic contacts. $TiSi_2$ has become a promising material in sub-micron silicon technology, because of its low resistivities and high electromigration resistance, high temperature stability [2], and minimum metal spiking effect. The possibility of forming silicides directly on polysilicon has also made $TiSi_2$ a promising material, and therefore it can be self-aligned (SALICIDE).

Along with the reduction in lateral feature size for future ultra large scale integration (ULSI) devices, it is necessary to achieve very shallow junctions [3]. In the present study, devices were fabricated by ion implantation through titanium metal, and silicidation and dopant activation were performed by subsequent furnace and rapid thermal annealing.

2. Experimental Details

Single crystal silicon wafers (p-type Czochralski) of (100) orientation and 1 to 15 Ω cm resistivity were used in these experiments. The cleaning procedure consisted of the conventional RCA technique followed by a HF dip and a thorough rinsing with deionized (DI) water. Titanium films, ≈20 nm thick, were evaporated on silicon wafers in a vacuum

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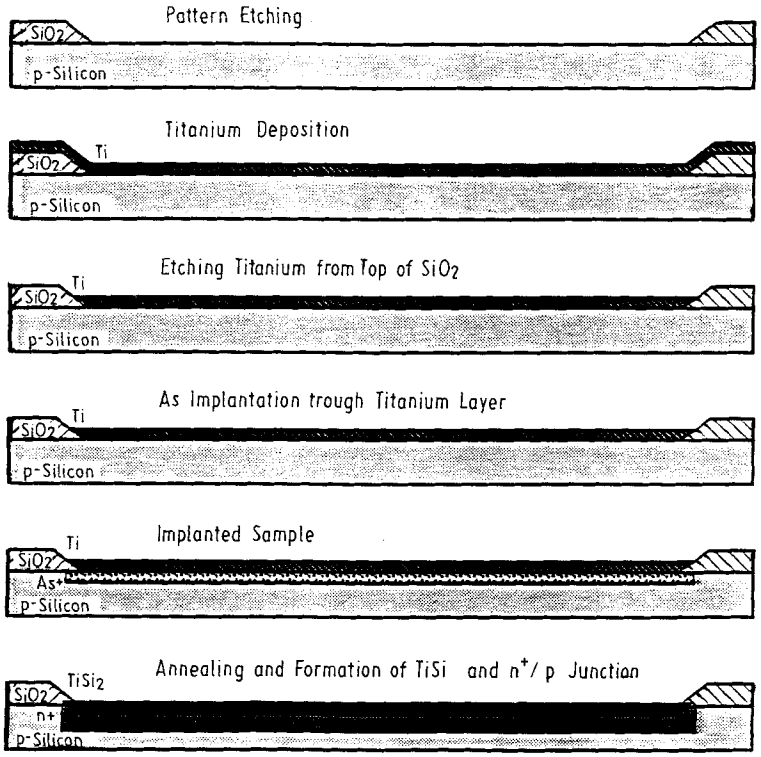

Fig. 1. Processing sequence for ITM technique

of 1.3×10^{-5} Pa. The deposition rate was kept low (< 1 nm s^{-1}) in order to minimize the interaction between the metal and the underlying substrate. For electrical measurements, similar depositions were performed using metal masks. The deposited films (through the mask) were circular in geometry and 0.8 mm in diameter. Ion beam mixing was performed with a 200 keV Varian 350D implanter using 100 keV As^+ ions. It is estimated that, at this

Table 1
Process details of samples

1. p-silicon, (100) orientation, 1 to 15 Ω cm resistivity
2. RCA cleaning, HF dip, and rinsing with DI water
3. deposition of 20 nm Ti through mask of 0.8 mm diameter
4. ion implantation through metal, arsenic 100 keV, 10^{16} cm^{-2}
5. annealing in the following sequences in Ar

wafer No.	annealing process
1	RTA 800 °C, 10 s
2	RTA 800 °C, 10 s; anneal 600 °C, 30 min
3	RTA 800 °C, 10 s; anneal 600 °C, 30 min; RTA 900 °C, 15 s
4	anneal 600 °C, 30 min; RTA 1100 °C, 15 s
5	RTA 800 °C, 10 s; anneal 600 °C, 30 min; RTA 1000 °C, 15 s

energy, the As^+ ions have a range, R_p, of 58 nm in Si. The current density was maintained below 1 $\mu A\ cm^{-2}$ in order to minimize substrate heating during ion implantation. A constant dose of 10^{16} ions cm^{-2} was used throughout the experiment.

An AG Associates 210T rapid thermal annealer (RTA) was used to sinter the films. Several sets of samples were prepared – the first one consisted of a single-step anneal, after ion implantation through metal. This set of samples was annealed in RTA at temperature of 900 °C for 20 s in an argon ambient. The second set of samples were subjected to two-step anneal – 500 °C in argon ambient for half an hour in a furnace followed by RTA at 1000 °C for 10 s in argon [4, 5]. The third set comprised of samples subjected to multiple anneals – RTA–furnace anneal–RTA. Additional sets of samples were considered for structural and compositional analyses. The electrical measurements were confined to two sets of samples involving single- and two-step anneals. The schematic detailing of the process steps is shown in Fig. 1. The details of all the sets of samples, considered in this study, are presented in Table 1. Electrical measurements of the current–voltage characteristics (I–U), at room temperature, were performed on these samples using a Keithley-236 source measure unit. These experiments, as function of temperature, were performed with a HP 4145A semiconductor parameter analyzer, low temperature microprobe, and programmable temperature controller.

3. Results and Discussion

RBS spectra for the samples are presented in Fig. 2. The RBS spectra for one of the samples with annealing conditions: RTA 800 °C, 10 s; furnace anneal 600 °C, 30 min; RTA 1000 °C,

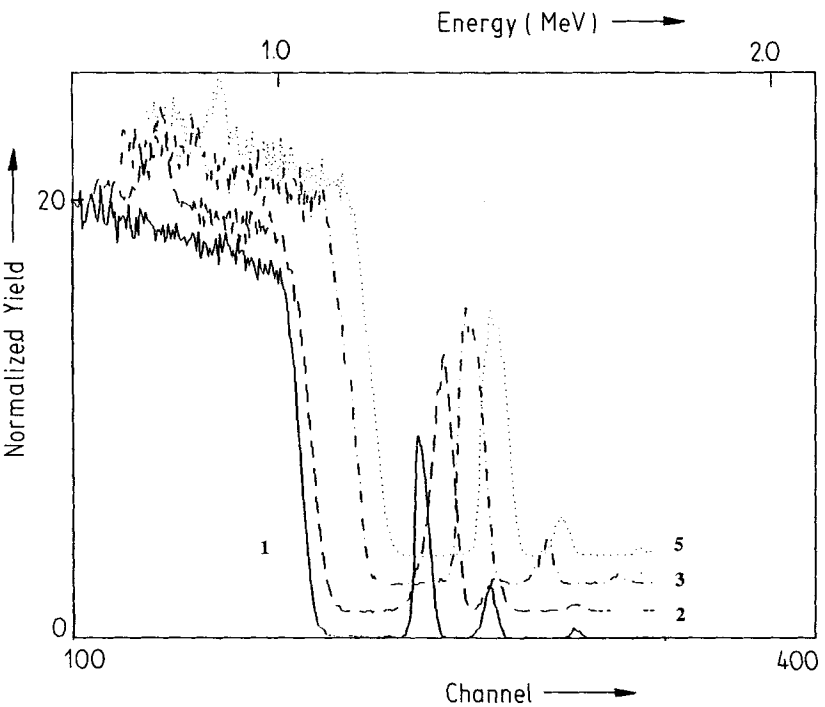

Fig. 2. RBS spectra for $TiSi_2/n^+/p$-Si at 165° scattering angle; wafer number is indicated at curves

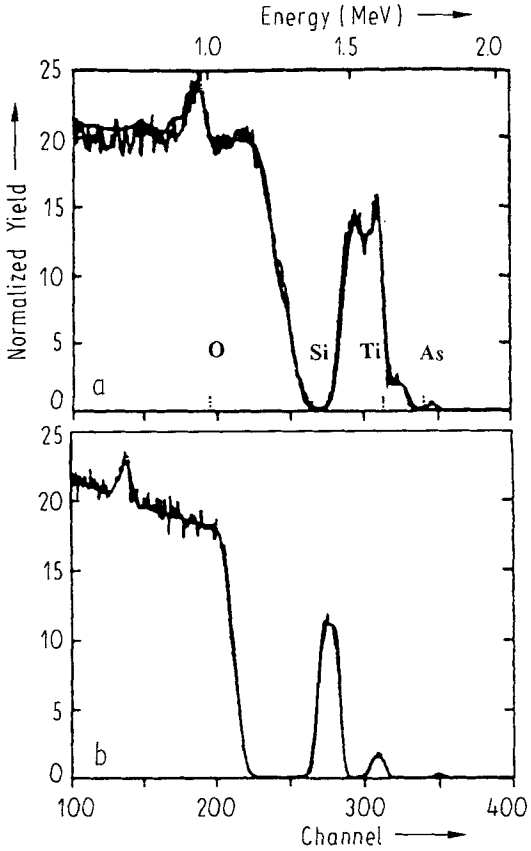

Fig. 3. RBS spectra and RUMP simulation plots for $TiSi_2/n^+/p$-Si at a) 70° and b) 165° scattering angles; sample 5, As^+ implant

15 s, for two different scattering angles of 70° and 165°, respectively, are shown in Fig. 3. The results of the RUMP simulation are compared with the experimentally obtained RBS spectra in Fig. 3. RBS measurements were carried out using a 1.8 MeV He^+ beam for two scattering angles, 70° and 165°, respectively. The RBS spectra were analyzed using computer program RUMP (Rutherford Universal Manipulation Program – developed at Cornell University [6]). The SIMS analyses were obtained, using a quadrupole-based ion microanalyzer PHI 6300. The cesium primary ion beam, utilized, was rastered over a $400 \times 400\ \mu m^2$ area, with secondary ions collected from the center 9% of the sputtered crater. The ion impact energy of the primary ions was 9 keV, with an angle of incidence of 60° to the surface normal. Electron neutralization was used to compensate for electrical charging while profiling through the insulating layer. The system vacuum was approximately $\approx 10^{-7}$ Pa when performing the sputter depth profiling [7]. SIMS spectra of the same samples are shown in Fig. 4. In Fig. 5, comparisons of SIMS and RBS data, including RBS simulation plots from RUMP, are shown.

When a metal film, formed on a silicon substrate, reacts to form a silicide upon annealing, the silicide–silicon interface moves into the silicon during the silicidation process and most of the silicide is buried in silicon [8]. Therefore, the junction depth for the silicided doped layers was defined as the distance from the silicide surface to the p–n junction (see Fig. 6). Assuming that all the Ti metal has been converted into $TiSi_2$, then growing a silicide of thickness x consumes a layer of silicon $0.936x$ thick (see Appendix). A 20 nm thick titanium metal layer can be converted into a 48.8 nm $TiSi_2$ silicide layer, as calculated in the Appendix. But, most of the time, RTA or furnace anneals do not convert all the Ti to silicide. The annealing processes do not lead to the formation of only silicide species of $TiSi_2$, but some other composition of titanium silicides also, such as TiSi, $TiSi_3$, etc.

During silicidation of titanium, an interface is formed separating the silicon from the silicide. As silicidation proceeds, this interface advances into the silicon. Doping impurities will redistribute at the interface until the chemical potential is the same on each side of the interface. This redistribution may result in an abrupt change in impurity concentration

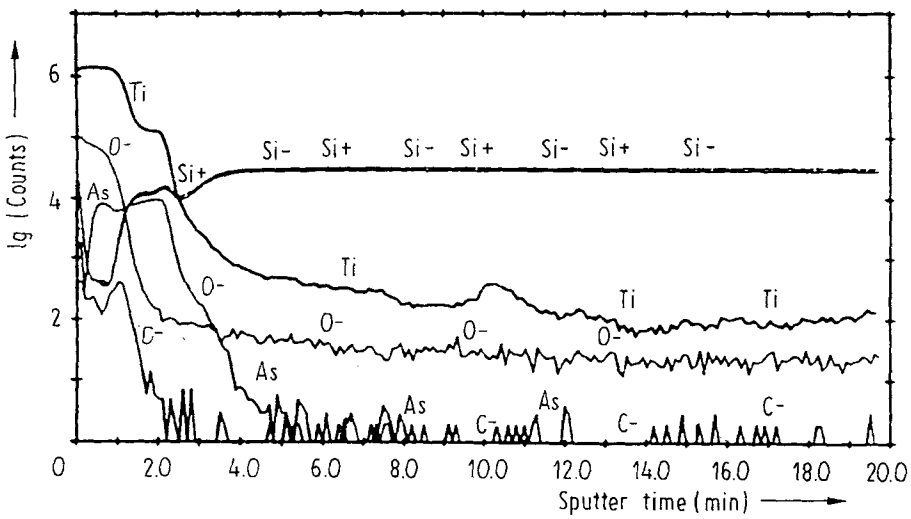

Fig. 4. SIMS spectra for $TiSi_2/n^+/p$-Si; sample 5

across the interface. The equilibrium segregation coefficient is determined primarily by the chemical potential difference and the kinetics of redistribution at the interface [8]. However, from Fig. 3 and 4, it is observed that arsenic distributes uniformly in the silicide layer and not just at the $TiSi_2/Si$ interface.

Very little is known of the diffusion of impurities in silicides. Arsenic has been reported to have a diffusivity in $TiSi_2$ that is several orders of magnitude higher than in silicon [2]. From the literature [9, 10], it is known that arsenic atoms have a very high diffusion coefficient, of the order of 10^{-13} cm^2/s at 600 °C, in the silicide. This is at least five orders

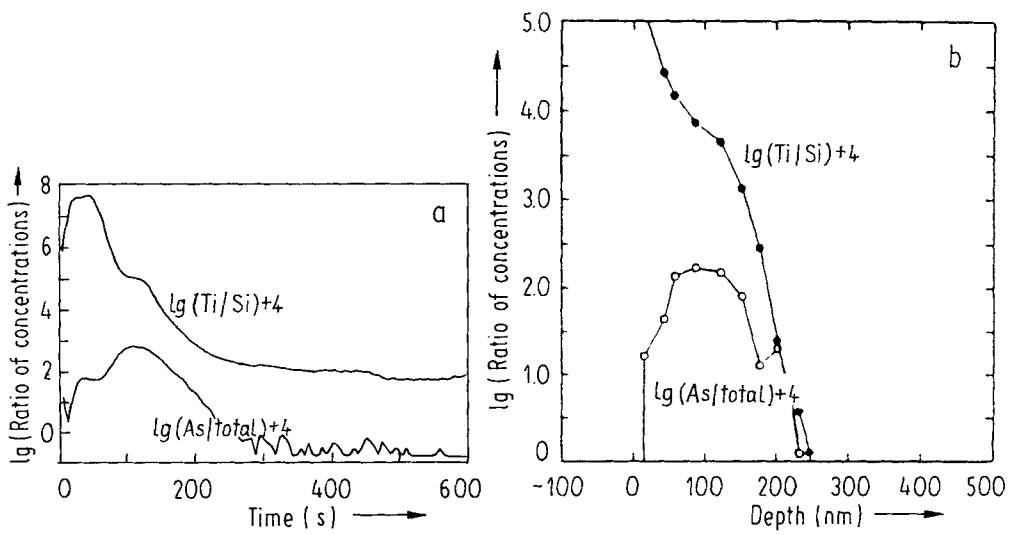

Fig. 5. a) Concentration ratios of primary species vs. ion milling time; SIMS data. b) Concentration ratios of primary species vs. depth; RBS simulation program RUMP data; sample 5

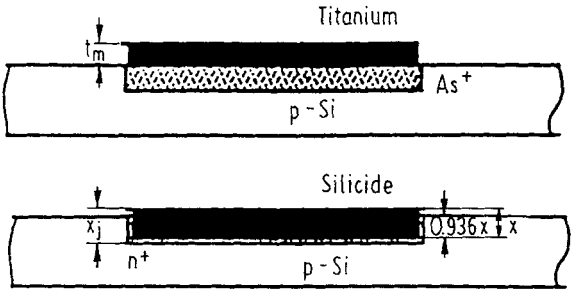

Fig. 6. Growth of silicide by thermal silicidation (x thickness of silicide layer, t_m thickness of titanium layer, x_j junction depth)

of magnitude larger than the diffusivity of arsenic in Si. Therefore, post annealing at temperatures higher than 600 °C leads to segregation of arsenic atoms into $TiSi_2$. The Ti and Si signals shown in RBS and SIMS spectra of Fig. 4 and 5 indicate the formation of an approximately 50 nm thick $TiSi_2$ layer, and arsenic concentration peaks are distributed at the interfaces.

Current–voltage characteristics for single-step annealed samples are shown in Fig. 7a and b, for temperatures of 250 and 300 K respectively. Representative I–U plots for two-step annealed samples for temperatures of 250, 300, 350, and 400 K are shown in Fig. 8a to d, respectively. From Fig. 7a and b, it is seen that the single-step annealed samples follow the p–n junction I–U characteristics but with a very high series resistance. A forward bias voltage from 0 to −3 V was applied to analyze the device behavior. From the I–U curves in Fig. 8a to d, it is seen that the two-step annealed samples follow the simple equation of p–n junctions under forward bias,

$$I = I_s\left(\exp\left\{\frac{qU}{nkT}\right\} - 1\right), \tag{1}$$

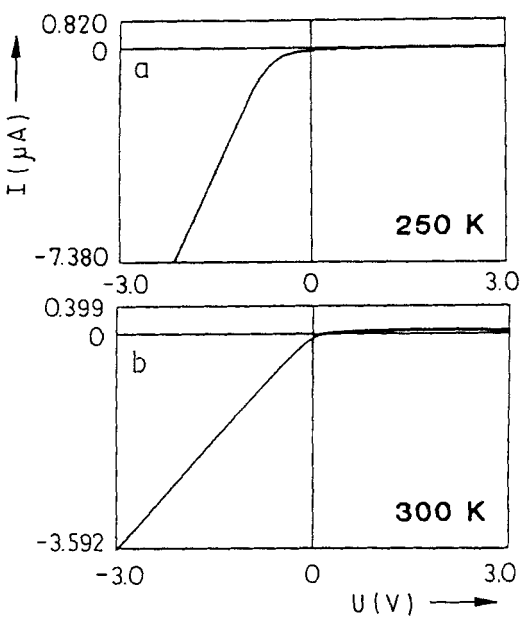

Fig. 7. I–U plots for $TiSi_2/n^+/p$-Si device for single-step anneal

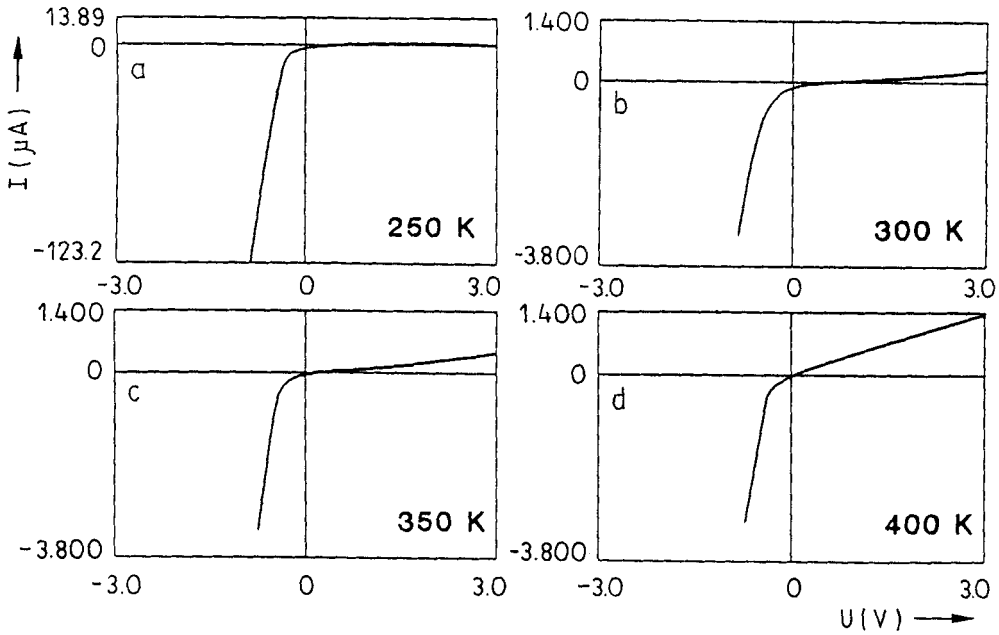

Fig. 8. $I-U$ plots for $TiSi_2/n^+/p$-Si device for two-step anneals

where I_s is the saturation current in A, U the applied voltage, n the ideality factor, k the Boltzmann constant, and T the temperature in K. From Fig. 8a to d, it is clear that $TiSi_2$ makes nearly ohmic contact with the n^+/p-Si devices, after appropriate annealing time and temperature. These figures show that, as the measurement temperature increases, the current flowing through the device increases. The saturation current is temperature dependent and is given by

$$I_s = \frac{qAD_n n_i^2}{L_n N_A}, \tag{2}$$

where A is the area of the device, D_n is the diffusivity of electrons in the p-region, L_n the diffusion length, n_i the intrinsic carrier concentration, and N_A the substrate doping. n_i is temperature dependent and is given by [11]

$$n_i(T) = a_i T^3 \exp\left(\frac{-E_{g0}}{kT}\right), \tag{3}$$

where

$$a_i = 4\left(\frac{2\pi k}{h^2}\right)^3 (m_n m_p)^{3/2} \exp(-\alpha_g), \tag{4}$$

where α_g is an empirical constant characteristic of the semiconductor. It is given by the equation

$$\alpha_g = \frac{dE_g}{dT}\frac{T-300}{kT}. \tag{5}$$

Table 2
Temperature dependent parameters

T (K)	n_i (cm^{-3})	E_g (eV)	D_n (cm^2/s)	μ_n (cm^2/V s)
250	9.6×10^7	1.13	0.0646	3.0
300	1.45×10^{10}	1.12	0.117	4.5
350	4.8×10^{11}	1.108	0.012	4.0
400	7.23×10^{12}	1.097	0.12	3.5

By simplifying the above equations, the intrinsic carrier concentration at various temperatures can be calculated by

$$n_i = 3.73 \times 10^{16} T^{3/2} \exp\left(\frac{-7014}{T}\right). \tag{6}$$

Also, the diffusivity of the electron is directly related to the mobility by the well-known Einstein relation,

$$D_n = \frac{kT}{q} \mu_n, \tag{7}$$

where the mobility is proportional to the temperature as $T^{-3/2}$. With increase in temperature, the mobility decreases [12].

In Table 2, the calculated values of n_i, E_g, D_n, and μ_n at different temperatures are presented. These are the factors that influence changes in the device current at different measurement temperatures. The ideality factors have been calculated from the experimental results and from the previously published data. These are summarized in Table 3. From this table, it is seen that the ideality factor varies from 0.5 to 3.6. This means that, at lower voltage range, 0.01 to 0.10 V, recombination currents will dominate. At the higher voltage range, 0.20 to 0.60 V, high injection and series resistance effects will dominate the current flow. The ideality factor is seen to depend on the annealing conditions. The data from [13, 14] show the ideality factor to be below 2.0. These samples [13, 14] were prepared at annealing temperatures, time, and implantation energy different from samples considered in the present study. The data from [10] show low saturation current and ideality factor compared to all other data. This work relates to the $TiSi_2/p^+/n$-Si structure [10] and all the other data are based on the $TiSi_2/n^+/p$-Si structure. As has been pointed out earlier, in the case of the $TiSi_2/n^+/p$-Si structure, arsenic atoms have very high diffusion coefficients of the order of 10^{-13} cm^2/s at 600 °C in the silicide. Thus, post annealing at temperatures higher than 600 °C leads to loss of arsenic atoms from n^+/p-Si into $TiSi_2$. This loss is expected to result in the Schottky-barrier formation. For the structure of $TiSi_2/p^+/n$-Si, the boron distribution in $TiSi_2$ is unaffected by post-silicidation anneals. There is no outdiffusion of boron from p^+/n-Si into $TiSi_2$ even at temperatures of 900 °C. This results in an increased electrical activation of carrier concentration of boron without any loss [10, 13 to 15].

At measurement temperatures of 400 K, it is found that the ideality factor is greater than 2 for all ranges of voltages. This means that recombination and high injection effects will dominate over the diffusion current through the device at high measurement temperatures. The saturation current, I_s, increases by three orders of magnitude as the measurement

Table 3
Analysis of current–voltage characteristics

T (K)	voltage range (V)	n	I_s (A)	area (cm^2)	J_s (A cm^{-2})
250	0 to 0.07	2.42	6.8×10^{-11}	5.18×10^{-3}	1.31×10^{-8}
	0.07 to 0.20	1.60			
	0.20 to 0.025	3.60			
	0.25 to 0.35	3.06			
	0.35 to 0.60	3.60			
300	0 to 0.10	1.09	1.8×10^{-10}	5.18×10^{-3}	3.47×10^{-8}
	0.10 to 0.20	1.92			
	0.20 to 0.275	2.90			
	0.275 to 0.60	3.30			
350	0 to 0.05	0.50	20×10^{-9}	5.18×10^{-3}	3.86×10^{-6}
	0.05 to 0.20	1.37			
	0.20 to 0.60	1.96			
400	0 to 0.20	2.26	53×10^{-9}	5.18×10^{-3}	1.023×10^{-5}
	0.20 to 0.275	2.78			
	0.275 to 0.35	2.26			
	0.35 to 0.60	3.00			
300 [13]	0 to 0.20	1.19	2×10^{-9}	4.22×10^{-3}	4.73×10^{-7}
	0.20 to 0.40	1.85			
300 [10]	0 to 0.10	0.64	1×10^{-12}	3.2×10^{-2}	3.125×10^{-11}
	0.10 to 0.40	1.06			
300 [14]	0 to 0.20	1.63	8×10^{-11}	1×10^{-4}	8.0×10^{-7}
	0.20 to 0.40	1.35			
300 [4, 5]	0.40 to 0.60	1.67	5.6×10^{-9}	1×10^{-2}	5.6×10^{-7}
	0 to 0.15	2.40			
	0.15 to 0.40	2.50			
	0.40 to 0.60	2.80			

temperature increases from 250 to 400 K. This current is proportional to n_i. As the temperature increases, the value of n_i increases.

In this work, it is observed that, for two-step annealed samples, complete conversion of Ti into $TiSi_2$ has occurred and most of the dopants are electrically activated. Earlier studies [5] of the structural properties of these samples, using transmission electron microscopy (TEM), have shown the formation of a uniform 40 nm thick silicide for the As^+ implanted samples. No evidence of ion-implantation induced damage is observed in the underlying silicon substrate. The TEM micrograph of the same sample (single-step) sintered at 900 °C for 20 s shows that the interface between the silicide and the substrate is rough. The sheet resistance, R_{sh}, for the As^+ implanted samples was typically in the range of 58 to 30 Ω/□. This decrease in R_{sh} was monitored as function of sintering temperature from 350 to 900 °C for 10 min in argon [5].

4. Conclusions

Experimental studies of the $TiSi_2/n^+/p$-Si shallow junction formation and electrical characterization are reported in the above study. By using ion implantation through metal

technique, with implantation followed by RTA and furnace annealing, ultra shallow junctions (junction depth <0.1 μm) with ohmic contacts by silicide layers can be formed at the same time. Structural analyses have led to an understanding of the composition of these structures for single-, two-, and three-step anneals. The temperature dependent current–voltage characteristics of these devices, for single- and two-step anneals, have led us to analyze the device structures qualitatively. Using the conventional p–n junction theory, the device parameters of these structures have been obtained.

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Appendix

Example 1. The volume of 1 mol silicon is

$$\frac{\text{molecular weight of Si}}{\text{density of Si}} = \frac{28.09\ \text{g/mol}}{2.33\ \text{g/cm}^3} = 12.06\ \text{cm}^3/\text{mol}\,. \tag{A1}$$

The volume of 1 mol titanium silicide is

$$\frac{\text{molecular weight of } TiSi_2}{\text{density of } TiSi_2} = \frac{104.08\ \text{g/mol}}{4.043\ \text{g/cm}^3} = 25.74\ \text{cm}^3/\text{mol}\,. \tag{A2}$$

Since 2 mol silicon is converted to 1 mol $TiSi_2$,

$$\frac{\text{thickness of Si} \times \text{area}}{\text{thickness of } TiSi_2 \times \text{area}} = \frac{\text{volume of 2 mol of Si}}{\text{volume of 1 mol of } TiSi_2}\,, \tag{A3}$$

$$\frac{\text{thickness of Si}}{\text{thickness of } TiSi_2} = \frac{12.06 \times 2}{25.74} = 0.936\,, \tag{A4}$$

$$\text{thickness of silicon} = 0.936 \times \text{thickness of } TiSi_2\,. \tag{A5}$$

Assuming all the deposited 20 nm thick Ti metal has been converted into $TiSi_2$ silicide, then:

Exampe 2. The volume of 1 mol Ti is

$$\frac{\text{molecular weight of Ti}}{\text{density of Ti}} = \frac{47.90\ \text{g/mol}}{4.5\ \text{g/cm}^3} = 10.64\ \text{cm}^3/\text{mol}\,. \tag{A6}$$

Because 1 mol Ti is converted to 1 mol $TiSi_2$,

$$\frac{\text{thickness of Ti} \times \text{area}}{\text{thickness of } TiSi_2 \times \text{area}} = \frac{\text{volume of 1 mol of Ti}}{\text{volume of 1 mol of } TiSi_2}\,. \tag{A7}$$

Thus,

$$\frac{\text{thickness of Ti}}{\text{thickness of } TiSi_2} = \frac{10.64}{25.74} = 0.41 . \tag{A8}$$

Thickness of 20 nm Ti can be converted to that of $TiSi_2$ as

$$\text{thickness of } TiSi_2 = \frac{20\text{ nm}}{0.41} = 48.8\text{ nm} . \tag{A9}$$

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