Rapid Thermal Processing of Silicon Wafers with Emissivity Patterns

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Fabrication of devices and circuits on silicon wafers creates patterns in optical properties, particularly the thermal emissivity and absorptivity, that lead to temperature nonuniformity during rapid thermal processing (RTP) by infrared heating methods. The work reported in this paper compares the effect of emissivity test patterns on wafers heated by two RTP methods: (1) a steady-state furnace or (2) arrays of incandescent lamps. Method I was found to yield reduced temperature variability, attributable to smaller temperature differences between the wafer and heat source. The temperature was determined by monitoring test processes involving either the device side or the reverse side of the wafer. These include electrical activation of implanted dopants after rapid thermal annealing (RTA) or growth of oxide films by rapid thermal oxidation (RTO). Temperature variation data are compared with a model of radiant heating of patterned wafers in RTP systems.

Key words: Rapid thermal annealing (RTA), infrared radiation, Si

INTRODUCTION

Rapid thermal processing (RTP) of silicon wafers is employed as a processing step whenever a short time at high temperature serves a critical need for a low thermal budget (loosely defined as a small temperature-time product).[1,2] Presently accounting for about 0.1% of capital and operating costs in integrated circuit (IC) manufacture, RTP is projected to extend to applications such as integrated nanoscale devices and nano-electro-mechanical systems (NEMS).[3] Temperature control and within-wafer uniformity determine whether a given rapid thermal annealing (RTA) process is able to meet stringent device fabrication requirements. Some critical needs in IC fabrication are processing the source, drain, and high-κ gate dielectric material for transistors. As process tolerances have narrowed, because of shrinking device dimensions driven by the pursuit of ever higher circuit densities coupled with low power requirements and low RC time delays, temperature control windows have become progressively tighter while cycling times to high temperature have become shorter.

The RTP methods that are considered in this paper use infrared radiation to heat wafers. A temperature cycle is determined by the maximum temperature; the time duration at maximum temperature, which ranges in this study from about 1 sec (for a "spike" process) to 60 sec (for a "soak" process); and the rates of heating and cooling. Fluctuations in temperature control depend on the type of RTP method and the sensitivity of the process to variable optical properties of wafers, such as the emissivities of film patterns.

Previous work, which has studied problems of nonuniform radiative transfer in RTA methods, has focused on rapid heating achieved by cycling the power to infrared lamps.[4–11] Less attention has been devoted to furnace heating where the wafer is transiently inserted into a steady heat source.[12] We denote temperature cycling methods that use a steady heater as type I and those that modulate the heater output as type II.[3] A bare silicon wafer can usually be heated with a temperature uniformity of 1 K variation (one standard deviation) in an RTA system. In the lamp method, for example, heater power can be profiled to compensate for geometrical effects such as the wafer edge, discreteness of the lamps, and chamber reflections. However, heating efficiency becomes less uniform across wafers that have been patterned with devices.

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Deposition and patterning of the film stacks, such as oxides and nitrides of silicon, amorphous silicon, and polycrystalline silicon, create variations in the thermal radiative properties of device-processed silicon. These include the thermal absorptivity, which determines the absorbed power, and thermal emissivity, which determines the reradiated power.[13] Radiative transfer effects are determined to a significant extent by a wafer's total absorptivity and emissivity, which are averages over the emission spectra of the heater and wafer, respectively, and averages over the hemispherical field of view from the perspective of the wafer surface.

In closed-loop control of temperature uniformity, information from one or more temperature sensors is used in a feedback loop to control one or more sources of heating radiation. Methods using arrays of heaters generally have limited ability to articulate the lateral distribution of the output power on a scale as fine as that of integrated circuit features. In lamp methods, the lateral resolution is fixed by the spacing between lamps. Recognizing this limitation on temperature control, the heaters in the RTP systems modeled in this paper are treated as infrared sources of radiant power that is uniform on the scale of the lateral emissivity variations on the wafer. It is worth mentioning that the resolution in closed-loop control could be improved, in principle, by measuring the emissivity, absorptivity, and temperature profiles of a wafer in real time and projecting compensating radiation patterns on the wafer. However, this level of complexity has yet to be realized in practice.

The influence of wafer emissivity on temperature in RTP was previously studied using wafers patterned with films of varying emissivity.[4–12] In these earlier works and the present work, temperature distributions within wafers are determined indirectly by monitoring process results that are sensitive to RTP temperature. Methods include measurement of the post-RTA sheet resistance of silicon previously implanted with a dopant impurity (e.g., a high-dose, shallow implant of As^+ or B^+) or the thickness of a SiO_2 film grown by rapid thermal oxidation (RTO) of silicon.

In this work, an analytical model is developed for temperature distributions of patterned wafers in various types of RTP systems. The model is then applied to an experimental study using implant-anneal or thermal oxidation processes to monitor the effect of emissivity patterns on wafer temperatures in furnace and lamp RTP systems. Three types of 200-mm wafers were used in the experiments: uniformly lightly doped wafers (bulk type), heavily doped wafers with a lightly doped epitaxial layer (epi type), and silicon-on-insulator wafers (SOI type). Emissivity patterns were produced by deposition of multiple layers of SiO_2, Si_3N_4, or polycrystalline Si (poly-Si) films on the wafers, followed by patterning with photolithography and dry-plasma or wet-chemical etching. Temperature variations across the wafers were determined by mapping the sheet resistance measured by a scanning four-point electrical probe or by mapping the oxide film thickness measured by a scanning ellipsometer. Processes for temperature monitoring used measurements performed on unpatterned reverse (lower) sides or on patterned device (upper) sides of the wafers.

RADIANT HEATING MODEL

The temperature distribution across a wafer is a fundamental metric for the capability of an RTP system. The present work is a study of furnace and incandescent-lamp RTP methods in which the source of heating radiation is relatively remote from the wafer, i.e., the heater need not be in intimate contact with the wafer (e.g., heater to wafer distance exceeds wafer thickness). In this case, while thermal conductive and convective modes of heat transport do make contributions, radiation is the dominant mechanism of heating and cooling at high temperatures (>1,000°C). The RTP methods also have a characteristic time duration on the order of 1 second or more, allowing the temperature distribution across the thickness, d (~0.75 mm), of the wafer to approach steady state. In particular, the temperature variation across the thickness of the wafer is small compared to lateral variations in the wafer plane. This allows one to use a two-dimensional model for the temperature distribution in the wafer plane, denoted as T(x,y).

The steady-state heat balance equation is therefore modeled with three terms: thermal energy per unit area transported laterally by diffusion; radiative power per unit area absorbed from the heater, denoted as $P_{ABSORBED}$; and radiative power per unit area emitted by the wafer, denoted as $P_{EMITTED}$; it is written as

$$\lambda_{\parallel} d\, \nabla^2 T(x,y) + P_{ABSORBED}(x,y) - P_{EMITTED}(x,y) = 0 \quad (1)$$

Here, $\lambda_{\parallel}$ is the effective in-plane thermal conductivity, i.e., it is the conventional solid phase thermal conductivity of silicon, λ(T), augmented by the effect of heat transported by spatial variation in the radiation field at the wafer, much of which is outside the body of the wafer. The power terms in Eq. 1 are taken to be functions of position in the plane of the wafer, owing to the lateral variations of the wafer's absorptivity and emissivity, denoted below by symbols α and ε, respectively.

Considering the (x,y) plane of the wafer as a horizontal plane, and denoting the upper and lower sides of the wafer by U and L, respectively, the absorbed power term in Eq. 1 is written as

$$P_{ABSORBED}(x,y) = \alpha_U(x,y,T,T_U)P_U + \alpha_L(x,y,T,T_L)P_L \quad (2)$$

where P_U and P_L are heater powers per unit area that are incident on the upper and lower surfaces of the wafer, respectively. This model assumes that the

freely radiating incident power is uniform. The functions α are effective total absorptivities that depend on the optical properties of the wafer material at location (x,y), wafer temperature, heater temperature (due to the spectral distribution of the radiation produced by the heater), and multiple reflections between the wafer and internal surfaces of the RTP chamber. The heater temperature, which is denoted in the general case as T_H, is given as either T_U for the heater facing the upper side of the wafer or T_L for the heater facing the lower side. Simplified two-parameter expressions are taken for P_U and P_L. In the case of furnace heating, the heater powers are $P_U = \varepsilon_U \sigma T_U{}^4$ and $P_L = \varepsilon_L \sigma T_L{}^4$, where ε_U and ε_L are the emissivities of the furnace chamber as viewed from the upper and lower surfaces of the wafer, respectively, and where σ is the Stefan–Boltzman constant ($\sigma = 2\pi^5 k_B{}^4/15c^2h^3$). For incandescent lamp heating, the heater powers are expressed as $P_U = f_U \varepsilon_U \sigma T_U{}^4$ and $P_L = f_L \varepsilon_L \sigma T_L{}^4$, where f_U and f_L are geometrical form factors (fractional areas of view of lamp filaments from the perspective of the wafer) and T_U and T_L are filament temperatures corresponding to the upper and lower lamps, respectively. The case of single-sided lamp heating is modeled by taking $P_L = 0$.

The emitted power term in Eq. 1 is the thermal radiation emitted by the wafer:

$$P_{EMITTED}(x,y) = \varepsilon_U(x,y,T)\,\sigma T^4(x,y) + \varepsilon_L(x,y,T)\,\sigma T^4(x,y) \quad (3)$$

The ε functions are effective total emissivities that depend on the optical properties of the wafer material at location (x,y), wafer temperature, and multiple internal reflections between the wafer and the RTP chamber.

The effective total absorptivities and effective total emissivities appearing in Eqs. 2 and 3 are determined from the freely radiating total absorptivities and total emissivities of the wafer, denoted as α_F and ε_F, respectively, and reflections within the RTP chamber. The freely radiating total α_F and ε_F, in turn, are determined by the spectral optical properties of the wafer, α_S and ε_S, respectively, in a hypothetical black body environment. At high wafer temperature ($T \sim 1{,}300$ K), at which intrinsic silicon is rendered opaque by thermally excited free carrier absorption, the spectral absorptivity equals the spectral emissivity. Spectral emissivities are calculated from the known optical properties of silicon (including doped Si) and the composition of the films on the wafer, taking into account the wafer temperature and the thickness, dielectric constant, and extinction coefficient of each layer on the surface.[13,14] Of interest here is the total emissivity, which is defined as the average of the spectral emissivity over angle of incidence, θ, and the average over wavelength, λ, weighted by the Planck distribution function, $F(\lambda,T) = [\exp(hc/\lambda k_B T) - 1]^{-1}$. From the spectral emissivity for the film structure at a given (x,y) location on the wafer and denoted as $\varepsilon_S(x,y,T,\lambda,\theta)$, the corresponding freely radiating total emissivity is determined by

$$\varepsilon_F(x,y,T) = \int_0^\infty d\lambda\, F(\lambda,T)\,\varepsilon_h(x,y,T,\lambda) \Big/ \int_0^\infty d\lambda\, F(\lambda,T) \quad (4)$$

The freely radiating total absorptivity, α_F, is a function of both wafer and heater temperature, and is determined by

$$\alpha_F(x,y,T,T_H) = \int_0^\infty d\lambda\, F(\lambda,T_H)\,\varepsilon_H(x,y,T,\lambda) \Big/ \int_0^\infty d\lambda\, F(\lambda,T_H) \quad (5)$$

where the Planck distribution for the heater temperature T_H (T_U or T_L) is used. The function,

$$\varepsilon_h(x,y,T,\lambda) = 2\int_0^{\pi/2} d\theta\, \sin\theta\cos\theta\,\varepsilon_S(x,y,T,\lambda,\theta) \quad (6)$$

which appears in both Eqs. 4 and 5, is the freely radiating hemispherical spectral emissivity of the wafer. As a simplifying approximation, the temperature, T, appearing in Eqs. 4 and 5 is taken to be the mean wafer temperature, T_0 (the average of T(x,y) over the wafer). The function $\varepsilon_h(x,y,T,\lambda)$ is determined for wafer film structure and temperature corresponding to (x,y,T) by "Multi-Rad," which is a computer program that uses empirical models to calculate emissivity.[14] The integral over angle θ in Eq. 6 and the integrals over wavelength λ in Eqs. 4 and 5 are computed numerically as discrete sums.

As an example application, the freely radiating hemispherical spectral emissivity of an SOI wafer at various temperatures is shown in Fig. 1a. The oscillatory variation of ε_h with wavelength λ is caused by interfering optical reflections at the Si/SiO_2 interfaces, which makes an SOI wafer less absorptive than a bulk Si wafer at wavelengths near 0.8 μm and more absorptive near 0.5 and 2.5 μm. Emissivity also has pronounced temperature dependence for wavelengths above 1.2 μm, due to the temperature dependence of the band gap and the density of intrinsic free carriers in Si. Figure 1b illustrates the Planck distribution function $F(\lambda,T)$ as it is applied in Eq. 4 for wafer temperature $T = 1{,}050°C$, and in Eq. 5 for furnace temperature $T_H = 1{,}350°C$, or lamp temperature, $T_H = 2{,}650$ K (2,377°C). The peak in $F(\lambda,T)$ shifts toward shorter wavelength with increasing temperature (Wien displacement law, $(\lambda T)_{MAX} = 2{,}898$ μm K). The spectral weight of $F(\lambda,T)$ in Eq. 5 allows α_F to be more sensitive to the wavelength region where ε_h has a local minimum, when compared to ε_F calculated from Eq. 4. The result is that, for the SOI wafer at 1,050°C, the total absorptivity is less than the total emissivity, whereas for bulk type Si, they are comparable to one another.

The effective quantities $\varepsilon_U(x,y,T)$, $\varepsilon_L(x,y,T)$, $\alpha_U(x,y,T,T_U)$, and $\alpha_L(x,y,T,T_L)$ that appear in Eqs.

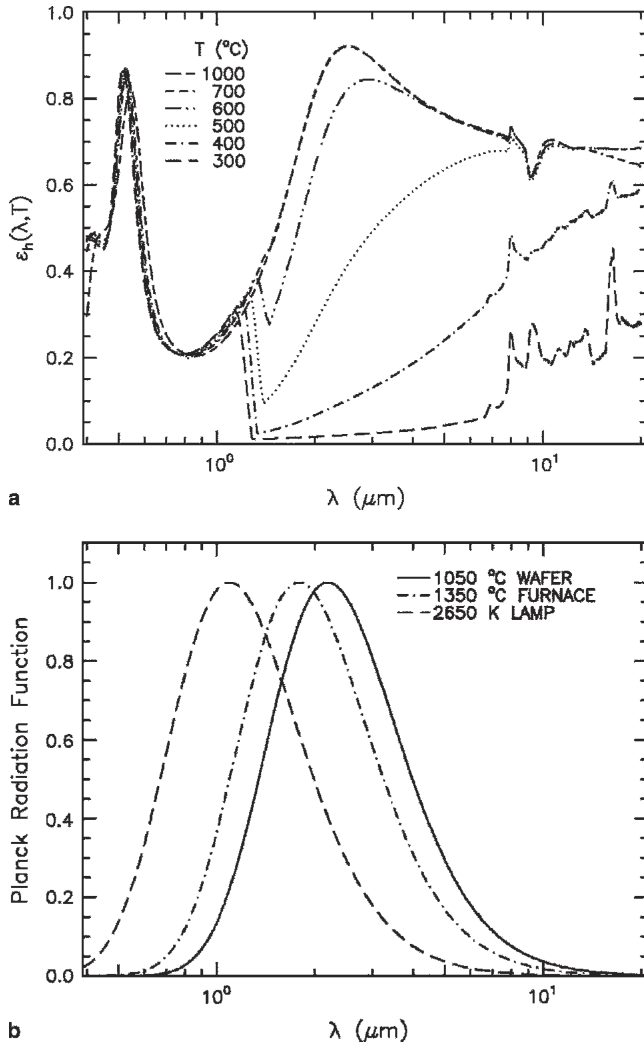

Fig. 1. (a) Model calculations of hemispherical freely radiating spectral emissivities of an SOI wafer (40-nm Si/140-nm SiO_2/725-μm Si) at temperatures from 300°C to 1,000°C. (b) Normalized Planck distribution functions at temperatures representative of a wafer and the heater in a furnace or lamp RTP system. λ is radiation wavelength.

2 and 3 take into account reflections within an RTP chamber that is modeled by chamber reflectivity, denoted generally as ρ_H, and specifically as either ρ_U or ρ_L, for the regions above or below the wafer, respectively. To illustrate the effect of multiple reflections between the wafer and the heating chamber surface, consider the case of a wafer with a uniform freely radiating total emissivity, ε_F. The total effective emissivity, ε, is given by the equation

$$\varepsilon = \varepsilon_F/[1 - \rho_H(1 - \varepsilon_F)] \quad (7)$$

A similar form gives the effective total absorptivity in terms of the freely radiating total absorptivity, α_F:

$$\alpha = \alpha_F/[1 - \rho_H(1 - \alpha_F)] \quad (8)$$

Extension of this treatment to include mixing of reflected images of a patterned wafer in the chamber is presented below in the "RTP Chamber Models" section.

EMISSIVITY TEST PATTERN

The current study uses an emissivity test pattern that is a periodic function of x and y for which one may apply periodic boundary conditions and solve Eq. 1 analytically (exclusive of wafer edge). The pattern structure is defined by a two-dimensional square lattice of spacing L with squares of edge dimension L/2 centered at each lattice site. This is illustrated in Fig. 2, showing that one-quarter of the pattern is occupied by squares; the remaining three-quarters are denoted as field area. The fraction of field area is $f_1 = 0.75$ and the fraction of square area is $f_2 = 0.25$. The effective emissivity and effective absorptivity of the field area surrounding the squares are denoted as ε_1 and α_1, respectively. The effective emissivity and effective absorptivity of the squares areas are denoted as ε_2 and α_2, respectively. The effective emissivity as a function of x and y can be expanded as Fourier series, written for convenience in the form

$$\varepsilon(x,y) = \varepsilon_0 + \varepsilon_\delta\left[\tfrac{1}{4}\left(1 + \sum_{n=1,3\ldots}^{\infty} a_n \cos k_n x\right)\left(1 + \sum_{n=1,3,\ldots}^{\infty} a_n \cos k_n y\right) - \tfrac{1}{2}\right] \quad (9)$$

where $k_n = 2\pi n/L$, $a_n = (-1)^{(n-1)/2}(4/\pi n)$, and n is an odd integer. The form of Eq. 9 is such that $\varepsilon_0 = (\varepsilon_1 + \varepsilon_2)/2$ and $\varepsilon_\delta = (\varepsilon_2 - \varepsilon_1)$. A form similar to Eq. 9 is used for the effective absorptivity function, $\alpha(x,y)$.

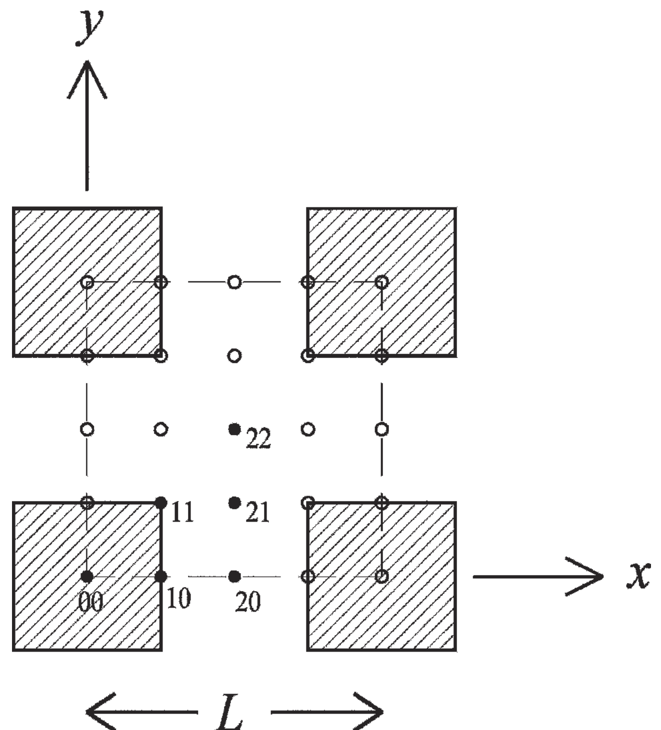

Fig. 2. Square lattice test pattern: squares areas (shaded), surrounded by field areas (white space), are repeated with periodicity of length L along both x and y directions. Dashed square encloses lattice unit cell. Circles indicate measurement test points (pL/4, qL/4), with indices p and q given for six filled circles.

The general solution to Eq. 1, which is commensurate with the pattern of Eq. 9, can be written in the form

$$T(x,y) = T_0 + \left[\tfrac{1}{4}\left(1 + \sum_{n=1,3,\ldots}^{\infty} t_n \cos k_n x\right)\left(1 + \sum_{n=1,3,\ldots}^{\infty} t_n \cos k_n y\right) - \tfrac{1}{2}\right] T_\delta \qquad (10)$$

where $t_n \approx (-1)^{(n-1)/2}(4/\pi n)(1 + L_d^2 k_n^2)^{-1}$ and $L_d \approx (\lambda_{\|} d/8\varepsilon_0 \sigma T_0^3)^{1/2}$ is a thermal diffusion length. The Fourier coefficients, t_n, are determined from an analytic solution of Eq. 1 under the approximation $T_\delta << T_0$.[15]

Recognizing that L_d may not be known à priori with sufficient accuracy, a practical approach is to use the symmetry properties of the periodic function T(x,y). Consider evaluating the solution $T(x_p, y_q)$ at specific sites given by $x_p = pL/4$ and $y_q = qL/4$, where p and q are integers. These sites are located on a square sublattice of periodicity L/4 and are shown as dots in Fig. 2. Among the 16 sublattice sites within the Wigner–Seitz unit cell of the pattern's two-dimensional lattice (i.e., bounded by $-L/2 \leq x \leq L/2$ and $-L/2 \leq y \leq L/2$), there are 6 inequivalent sites corresponding to (p,q) = (0,0), (1,0), (1,1), (2,0), (2,1), and (2,2). Evaluating Eq. 10 at these sites, and denoting $T_{pq} = T(x_p,y_q)$, one obtains

$$T_{pq} = T_0 + [\tfrac{1}{4}(1 + s\nu_p)(1 + s\nu_q) + \tfrac{1}{2}] T_\delta \qquad (11)$$

where $s = \sum_{n=1,3,\ldots}^{\infty} t_n$, $\nu_p = \cos(np\pi/2) = 1 - |p|$, and $\nu_q = \cos(nq\pi/2) = 1 - |q|$. The extrema in T_{pq} are T_{00} at the site at the center of a square, (x_0,y_0), and T_{22} at the site in the field, (x_2,y_2), diagonally midway between lattice sites (midway between next-nearest neighbor squares). The difference in the temperature T_{00} at the center of a square relative to the temperature T_{pq} at site (pq) can be written in the form

$$T_{00} - T_{pq} = S_{pq} T_\delta \qquad (12)$$

where

$$S_{pq} = \tfrac{1}{4}[(|p| + |q|)s + (|p| + |q| - |pq|s^2] \qquad (13)$$

The maximum temperature difference in the pattern is given by $T_{00} - T_{22} = sT_\delta$. The maximum temperature difference along the x-axis (Fig. 2) is given by $T_{00} - T_{20} = 1/2(s^2 + s)T_\delta$, where T_{20} is the temperature at a site in the field midway between nearest neighbor squares.

When the temperature distribution is expressed in the discrete form of Eq. 11, instead of the continuous function of Eq. 10, the infinite number of unknown coefficients, t_n, in the general solution is conveniently reduced to a single parameter, s. In the analysis of the experimental data, Eq. 11 is fitted to independent measurements of the six temperatures T_{pq}, using T_0, T_δ, and s as adjustable parameters.

The determination of T_δ is of special interest, since it is the theoretical solution to Eq. 1 in the limit of large L/L_d, where the first term for thermal diffusion transport may be neglected. This leads to s = 1 and the solution for T(x,y) then reduces to the two extrema, $T_1 \equiv T_{22}|_{s=1} \rightarrow T_0 - T_\delta/2$ for the temperature in the field areas between squares and $T_2 \equiv T_{00}|_{s=1} \rightarrow T_0 + T_\delta/2$ for the temperature in the squares areas. The mean temperature is T_0 and the temperature difference between the two areas in this limit is $T_\delta = T_2 - T_1$. In the following section, calculations of T_1 and T_2 are presented using models of multiple reflections in furnace and lamp RTP chambers.

RTP CHAMBER MODELS

In the experiments reported in this paper, the emissivity pattern of Fig. 2 is produced on only the upper (device) side of the wafer, while the lower side remains uniform (bare Si or with uniform protective coatings). The following treatment is applied to the steady-state radiant heating model. For the upper side field and squares areas, respectively, the freely radiating total emissivities are denoted as ε_{F1} and ε_{F2}, and the freely radiating total absorptivities are denoted as α_{F1} and α_{F2}. For the entire area of the lower side of the wafer, the freely radiating total emissivity is denoted as ε_{F3}, and the freely radiating total absorptivity is denoted as α_{F3}. Effective emissivities and absorptivities depend on internal reflections between a patterned wafer and the chamber.

The internal surfaces of an RTP chamber may reflect radiation emitted or reflected by a region of the wafer back onto an area that can be comparable to, or larger than, the scale of the emissivity pattern (e.g., lateral dimension greater than L). This has been considered for specific RTP chambers by ray tracing methods.[6] An analytic model of an RTP system, which is based on limiting cases for treating internal chamber reflections, is presented below.

In the limiting case, where there is no mixing of multiple reflections between areas of differing emissivity, the chamber reflects radiation emitted or reflected by a region of the wafer back onto that same region (such as in close-spaced mirror imaging). In this case, the secondary reflections of absorbed and emitted powers at the two areas of the wafer are not intermixed by chamber reflections and remain completely decoupled. Following Eqs. 7 and 8, the effective total emissivities and absorptivities of the three regions of patterned wafer in such a nonmixing chamber are given as

$$\varepsilon_i = \varepsilon_{Fi}/[1 - \rho_H(1 - \varepsilon_{Fi})] \qquad (14)$$

$$\alpha_i = \alpha_{Fi}/[1 - \rho_H(1 - \alpha_{Fi})] \qquad (15)$$

where index i is 1, 2, or 3, and denotes field, squares, or lower side areas, respectively, and $\rho_H = \rho_U$ for i = 1 or 2, and $\rho_H = \rho_L$ for i = 3.

Balancing the absorbed and emitted powers for both sides of the wafer, one has for the field area in the pattern, which is at temperature T_1,

$$\alpha_U \varepsilon_1 \sigma T_1^4 + \alpha_L \varepsilon_3 \sigma T_1^4 = \alpha_1 P_U + \alpha_3 P_L \tag{16}$$

and, for the squares areas in the pattern, which is at temperature T_2,

$$\alpha_U \varepsilon_2 \sigma T_2^4 + \alpha_L \varepsilon_3 \sigma T_2^4 = \alpha_2 P_U + \alpha_3 P_L \tag{17}$$

where $\alpha_U = 1 - \rho_U$ and $\alpha_L = 1 - \rho_L$ are the absorptivities of the chamber facing the upper and lower sides of the wafer, respectively. The solution to Eqs. 16 and 17 is expressed as a function of the temperature ratio:

$$(T_1/T_2)^4 = \frac{(\alpha_U\varepsilon_2 + \alpha_L\varepsilon_3)/(\alpha_U\varepsilon_1 + \alpha_L\varepsilon_3)}{(\alpha_1 P_U + \alpha_3 P_L)/(\alpha_2 P_U + \alpha_3 P_L)} \tag{18}$$

One observes from Eq. 18 that $T_1 = T_2$ in the limit of uniform total emissivity and absorptivity.

An analytical model can also represent the limiting case of complete mixing where chamber reflections are thoroughly homogenized. Denoting the fraction of wafer area corresponding to the field region by f_1 and the square area by f_2, the mean freely radiating total emissivity of the upper side of the wafer, denoted as ε_{MF}, is expressed in terms of the weighted average of the freely radiating total emissivities of the two pattern regions:

$$\varepsilon_{MF} = \varepsilon_{F1} f_1 + \varepsilon_{F2} f_2 \tag{19}$$

Similarly, we have, for the mean freely radiating total absorptivity, α_{MF},

$$\alpha_{MF} = \alpha_{F1} f_1 + \alpha_{F2} f_2 \tag{20}$$

The power emitted by the field areas in the pattern is the sum of the freely radiating emitted power and multiple reflections of power emitted from both field and squares areas. Summing up the multiple reflections between the wafer and the chamber, the result for the effective power emitted by field areas, which are at temperature T_1, is given by the expression

$$P_{EMITTED,1} = \alpha_U \sigma \left\{ \varepsilon_{1F} T_1^4 + \rho_U (1 - \varepsilon_{1F}) [1 - \rho_U (1 - \varepsilon_{MF})]^{-1} [f_1 \varepsilon_{1F} T_1^4 + f_2 \varepsilon_{2F} T_2^4] \right\} \tag{21}$$

It should be noted that the last term in Eq. 21 includes the contribution from multiple reflections of the power emitted by the squares areas, which are at temperature T_2. A similar expression is obtained for the power emitted by the squares areas:

$$P_{EMITTED,2} = \alpha_U \sigma \left\{ \varepsilon_{2F} T_2^4 + \rho_U (1 - \varepsilon_{2F}) [1 - \rho_U (1 - \varepsilon_{MF})]^{-1} [f_1 \varepsilon_{1F} T_1^4 + f_2 \varepsilon_{2F} T_2^4] \right\} \tag{22}$$

The effective power emitted from regions of the lower surface of the wafer that are opposite the field (i = 1) or the squares (i = 2) is given by an analogous expression:

$$P_{EMITTED,3,i} = \alpha_L \sigma \left\{ \varepsilon_{3F} T_i^4 + \rho_U \varepsilon_{3F} (1 - \varepsilon_{3F}) [1 - \rho_U (1 - \varepsilon_{3F})]^{-1} [f_1 T_1^4 + f_2 T_2^4] \right\}, i = 1,2 \tag{23}$$

In Eq. 23, the index 3 denotes the lower surface of the wafer and the index i determines whether a field (1) or square (2) area is on the opposing upper side of the wafer.

Summing multiple chamber reflections under the proviso that the chamber totally mixes radiation received from the wafer, one obtains an effective power absorbed from the heater by the field (i = 1) or square (i = 2) areas in the form $\varepsilon_{iF}\rho_U[1 - \rho_U(1 - \varepsilon_{MF})]^{-1}P_U$, where i = 1,2. The coefficient of P_U acts as an effective absorptivity, analogous to Eq. 8. A similar calculation determines the power absorbed on the lower side of the wafer, which is the same for both areas, that is, in the form $\varepsilon_{3F}\rho_U[1 - \rho_L(1 - \varepsilon_{3F})]^{-1}P_L$. Adding the two contributions, the power absorbed on both sides of the wafer corresponding to area (i) is given by

$$P_{ABSORBED,i} = \varepsilon_{iF} \rho_U [1 - \rho_U (1 - \varepsilon_{MF})]^{-1} P_U + \varepsilon_{3F} \rho_U [1 - \rho_L (1 - \varepsilon_{3F})]^{-1} P_L, i = 1,2 \tag{24}$$

In steady state, the emitted and absorbed powers are in balance at each of the areas (no heat is transferred between the field and square in the limit of large L):

$$P_{EMITTED,i} + P_{EMITTED,3,i} = P_{ABSORBED,i},\ i = 1,2 \tag{25}$$

The simultaneous solution of the two equations given by Eq. 25 for i = 1 and i = 2 yields the following algebraic expression for the temperature ratio:

with the definitions

$$(T_1/T_2)^4 = \frac{p[\varepsilon_{2F}(f_2^{-1} + \rho_2\rho_U) + a\,\varepsilon_{3F}(f_2^{-1} + \rho_3\rho_L)]}{\varepsilon_{1F}(f_2^{-1} + \rho_1\rho_U) + a\,\varepsilon_{3F}(f_1^{-1} + \rho_3\rho_L)}$$

$$\frac{-\rho_1\rho_U\varepsilon_{2F} - a\,\rho_3\rho_L\varepsilon_{3F}}{-p\,[\rho_2\rho_U\varepsilon_{1F} + a\,\rho_3\rho_L\varepsilon_{3F}]} \tag{26}$$

$$p = \frac{\alpha_1 P_U + \alpha_3 P_L}{\alpha_2 P_U + \alpha_3 P_L} \tag{27}$$

$$a = \alpha_L/\alpha_U \tag{28}$$

and

$$\alpha_i = \alpha_{iF}/[1 - \rho_U(1 - \alpha_M)], \quad i = 1,2 \tag{29}$$

$$\alpha_3 = \alpha_{3F}/[1 - \rho_L(1 - \alpha_{3F})] \tag{30}$$

$$\rho_i = (1 - \varepsilon_{Fi})/[(1 - \rho_U(1 - \varepsilon_M)], \quad i = 1,2 \qquad (31)$$

$$\rho_3 = (1 - \varepsilon_{F3})/[(1 - \rho_L(1 - \varepsilon_{F3})] \qquad (32)$$

Application to a furnace RTP system, where the chamber walls and other reflective surfaces are not close to the wafer, is modeled by the solution for T_1/T_2 obtained from Eq. 26 for fully mixed chamber reflections. Chamber reflectivities are generally assumed to have small values (<0.1) for furnace RTP systems. The heater power ratio, P_L/P_U, for a furnace RTP can be treated as an adjustable parameter in fitting this model to experiment.

Application to a lamp-based RTP system, where lamps and reflectors are located near the wafer for promoting heating and cooling efficiency, is modeled by combining the solution for T_1/T_2 obtained from Eq. 26 for fully mixed chamber reflections with that from Eq. 18 for no mixing. In applying this model to experiments with lamp RTP systems, one takes ρ_U and ρ_L as adjustable parameters.

The model parameters that are used to characterize RTP systems implicitly depend on chamber architecture, specularity of chamber surfaces, and structures contained within the chamber for optical access, wafer support, and purge gas.

PATTERNED WAFER FABRICATION

The influence of emissivity patterns of the type illustrated in Fig. 2 in rapid thermal processing was tested by two experimental procedures, which are categorized as A and B. The objectives of procedure A are to compare RTP methods and processes. The RTP methods are single-side lamp, dual-side lamp, and furnace RTP systems. The process variables are the time duration of the RTP process (ranging from spike to soak) and the type of process monitor employed (implant anneal or thermal oxidation). The objective of procedure B is to compare pattern-induced temperature variations for three types of substrate wafers that are commonly used in device fabrication (bulk, epi, and SOI) involving furnace and single-side lamp RTP systems. The wafers prepared for the two procedures, all of which are 200-mm diameter, are described in Table I. Freely radiating total emissivities calculated for the field and squares areas are also shown in Table I.[13,15]

Procedure A employed double-side polished bulk-type wafers with the pattern illustrated in Fig. 2 (repeated for a total of 69 squares) on the upper side. The lower side of the wafer was left bare. Films for the emissivity pattern, shown in Table I, were deposited on the upper side of the wafer and then etched back to bare silicon in the squares areas. Two film combinations were used to study cases in which the emissivity of the field area is either lesser (for wafer type A1) or greater (for wafer type A2) than the emissivity of the bare silicon in the squares areas.

Process temperatures were inferred from the temperature sensitivity of measurements on the unpatterned lower side of the wafer, which were either (1) the sheet resistance of implanted silicon after RTA or (2) the thickness of an oxide film after RTO.

Table IIA describes the RTP processes for procedure A. The wafers prepared for the implant-anneal RTA process were n-type bulk substrates that were implanted on the unpatterned bare-Si lower side with B^+ at 2 keV energy and 10^{15} cm^{-2} dose. The sheet resistance (R_s) of the implanted layer, which is electrically isolated from the substrate by the p-n junction that is formed upon RTA and is sensitive to the RTA temperature, is used to infer variations in effective process temperature. Wafers prepared for the thermal oxidation RTO process received an RCA type clean, with the final step before RTO being an etch in 100:1 dilution HF, which leaves a hydrophobic bare Si surface, or is alternatively given a rinse in ozonated deionized water, which leaves a hydrophilic chemically oxidized Si surface (~0.5-nm SiO_2). The thickness of the SiO_2 film that is grown by RTO is sensitive to temperature and is used to infer variations in effective process temperature. Although the sensitivity of the RTO process to temperature is equivalent for both surface treatments, the hydrophilic preparation is less prone to particulate contamination and allows the experimenter some time delay between the wafer clean and the RTO steps. The hydrophilic clean was used for single-side lamp RTO, which was coordinated to immediately follow the HF clean.

Procedure B employed device quality p-type bulk, epitaxial, and SOI type wafers with film patterns (Fig. 2) given in Table I. The films deposited for the pattern structure in procedure B on the B1 (bulk type) and B2 (epi type) wafers produce an emissivity of the field area that is greater than the emissivity of the square area. For the SOI wafer, the emissivity of the field area is smaller than the emissivity of the square area. The wafers in procedure B received a 25 keV, 10^{16} cm^{-2} As^+ implant prior to deposition of the films and their patterning. The anneals in procedure B used a spike RTA method, i.e., nominally zero time at peak temperature, during which variations in effective process temperature are inferred from measurements of R_s after the anneal. Two wafers of each type were processed.

EXPERIMENTAL PROCEDURE

Table II presents listings of the RTO and RTA processes used in procedure A and the RTA processes used in procedure B. Process results, expressed as wafer-mean measurements of oxide thickness, t_{ox}, or sheet resistance, R_s, are also shown. For the RTO process, the time duration at the peak temperature was varied from nominally zero (<1 sec) to 150 sec. For the RTA process, the time duration was either nominally zero or 1 sec.

Dual-side lamp heating for RTO processes in procedure A used an A.G. Heatpulse model 8108 (Metron Technology, San Jose, CA). The system

Table I. Patterned Wafers, for Procedure A, p-Type Bulk for RTO and n-Type Bulk for RTA*, and, for procedure B, p-type bulk, epi, or SOI

A. Procedure A

Wafer Type A1—Bulk Type

Area, i	Wafer Area Description	Films	ε_{Fi}	α_{Fi} (Furnace)	α_{Fi} (Lamp)
1	Upper side, field	20 nm Si_3N_4 110 nm poly-Si 199 nm SiO_2	0.6312	0.5836	0.4719
2	Upper side, squares	(None)	0.6713	0.6690	0.6545
3	Lower side	(None)	0.6713	0.6735	0.6545

Wafer Type A2—Bulk Type

Area, i	Wafer Area Description	Films	ε_{Fi}	α_{Fi} (Furnace)	α_{Fi} (Lamp)
1	Upper side, field	100 nm Si_3N_4 19 nm SiO_2	0.7248	0.7372	0.7961
2	Upper side, squares	(None)	0.6713	0.6690	0.6545
3	Lower side	(None)	0.6713	0.6735	0.5645

B. Procedure B

Wafer Type B1—Bulk p Type

Area, i	Wafer Area Description	Films	ε_{Fi}	α_{Fi} (Furnace)	α_{Fi} (Lamp)
1	Upper side, field	110 nm poly-Si 100 nm SiO_2	0.7033	0.67208	0.5485
2	Upper side, squares	70 nm SiO_2	0.6768	0.67642	0.6787
3	Lower side	(None)	0.6713	0.67351	0.6545

Wafer Type B2—Epi p/p+ Type

Area, i	Wafer Area Description	Films	ε_{Fi}	α_{Fi} (Furnace)	α_{Fi} (Lamp)
1	Upper side, field	110 nm poly-Si 100 nm SiO_2	0.7033	0.67210	0.5485
2	Upper side, squares	80 nm SiO_2	0.6785	0.67878	0.6862
3	Lower side	420 nm SiO_2 500 nm poly-Si	0.7796	0.76735	0.7624

Wafer Type B3—SOI p Type

Area, i	Wafer Area Description	Films	ε_{Fi}	α_{Fi} (Furnace)	α_{Fi} (Lamp)
1	Upper side, field	110 nm poly-Si 100 nm SiO_2 40 nm Si 140 nm SiO_2	0.6545	0.62190	0.5137
2	Upper side, squares	80 nm SiO_2 40 nm Si 140 nm SiO_2	0.7773	0.75678	0.5850
3	Lower side	(None)	0.6713	0.67351	0.6545

*Films are listed in order of deposition. Calculated freely radiating total emissivities, ε_{Fi} (1,050°C wafer temperature), and freely radiating total absorptivities, α_{Fi}, for single-side lamp (2,377°C upper side heater) and furnace (1,250°C upper side heater, 850°C lower side heater) RTP systems. Field and squares areas of patterned upper side (Fig. 2) and entirety of unpatterned lower side are denoted by i = 1, 2, or 3, respectively.

has arrays of linear quartz-halogen lamps within a reflective enclosure, and the wafer receives a fixed power distribution to minimize the variation in oxide film thickness. The ambient was O_2 at atmospheric pressure. Temperature was measured and controlled by a pyrometer viewing a point near the center of the wafer.

Single-side lamp heating was tested using an Applied Materials RTP Centura (Santa Clara, CA) system. The heater is a hexagonal matrix of quartz-halogen lamps that receive a controllable power distribution to minimize temperature variability, as determined by multipoint pyrometry. The wafer is rotated to achieve azimuthal uniformity. The

Table IIA. RTP Processes (Lower Side Measurement) for Experimental Procedure A*

RTO

Sequence No.	RTP System	Clean	Temperature (°C)	Time (sec)	O_2 Pressure (torr)	t_{ox} (nm)
1	Furnace	Chemox	1,050	150	760	10.6
2	Dual side lamp	Chemox	1,100	60	760	10.2
3	Dual side lamp	Chemox	1,100	<1	760	2.2
4	Single side lamp	HF	1,050	150	700	9.9
5	Single side lamp	HF	1,100	60	700	8.5
6	Single side lamp	HF	1,100	1	700	3.1
7	Single side lamp	HF	1,100	1	80	1.6

RTA

Sequence No.	RTP System	Temperature (°C)	Time (sec)	R_s (Ω)
1	Furnace	1,050	<1	259
2	Furnace	1,050	1	199
3	Single Side Lamp	1,050	1	186

*RTO used bulk p-type wafers with HF etch or chemical oxidation (chemox) cleans; t_{ox} is mean SiO_2 thickness on the lower side. RTA used bulk n-type wafers implanted on the lower side with B^+ at 2 KeV, 10^{15} cm^{-2}; R_s is the mean post-RTA sheet resistance on the lower side.

Table IIB. Spike RTA Processes (Upper Side Measurement) for Experimental Procedure B*

Sequence No.	Wafer Type	RTP System	R_s (Ω)
1	Bulk	Furnace	128
2	Bulk	Single side lamp	113
3	Epi	Furnace	128
4	Epi	Single side lamp	113
5	SOI	Furnace	137
6	SOI	Single side lamp	129

*Wafers implanted on upper side with As^+ at 10 keV, 10^{16} cm^{-2} prior to deposition of pattern films. R_s, mean sheet resistance on upper side after stripping pattern films, is shown for anneals at 1,050°C.

single-side lamp system was used for implant RTA tests and to study the dependence of the RTO process on time duration and ambient O_2 pressure.

Furnace heating was tested using an Axcelis Technologies Summit XT (Beverly, MA). This system has a SiC bell jar heated with a vertical temperature gradient. Wafer temperature is varied by elevated motion and is controlled using a central point pyrometer.

Temperatures, which were ramped up and down at 75°C/s, were controlled by closed-loop feedback methods. The various radiation pyrometers used to sense the wafer temperature in these systems either measure (furnace RTP) the emissivity of the wafer (which is generally unknown à priori and varies with temperature and process) or compensate for it (lamp RTP).

Given that oxidation and anneal processes are thermally activated (E_A ~2 eV and ~4 eV, respectively), it is useful to define a process temperature as the maximum in the RTP cycle (the peak temperature in a spike process or the steady temperature in a soak process). These are the temperatures listed in Table II. However, temperature distributions within the wafers are not measurable in real time with the required resolution (such as at the dotted points in Fig. 2) for the RTP systems in this study. Therefore, an effective process temperature is defined, where temperature is inferred from post-RTP mapping measurements of oxide film thickness t_{ox} in the case of RTO or the electrical sheet resistance R_s in the case of implant RTA. Each of these measured quantities is sensitive to the effective process temperature, owing to the thermal activation of film growth or dopant diffusion. Temperature sensitivities are determined in separate experiments (RTO or RTA) whereby a set of wafers is processed at several temperatures, $\{T_j\}$, and a model function, e.g., a polynomial or an activation formula, is fitted to the measurements of $\{t_{oxj}\}$ or $\{R_{sj}\}$ (a method referred to as "temperature calibration"). Studies of the temperature sensitivity of RTO processes, for example, were reported in a previous TMS symposium.[16] The model RTO and RTA functions for procedure A were determined with a set of bare (unpatterned) bulk-type monitor wafers; the model RTA function for procedure B was determined with a set of identically patterned wafers.

In procedure A, measurements of t_{ox} were obtained with a Thermawave (Fremont, CA) multipoint scanning ellipsometer. For each RTO process, experimentally determined calibration curves were used to convert individual measurements of t_{ox} to local wafer temperatures. An example of a contour map of t_{ox} obtained for a wafer of type A2 (Table I) that received a single-side 1s-RTO process (Table IIA, RTO, refer to sequence number 6) is illustrated in Fig. 3. The maximum diameter of the mapped region (50 mm) was dictated by ellipsometer capability at high resolution. The square lattice pattern of several unit cells is clearly discerned, with the oxide film thickness (and effective process temperature) being minimum at the centers of the squares.

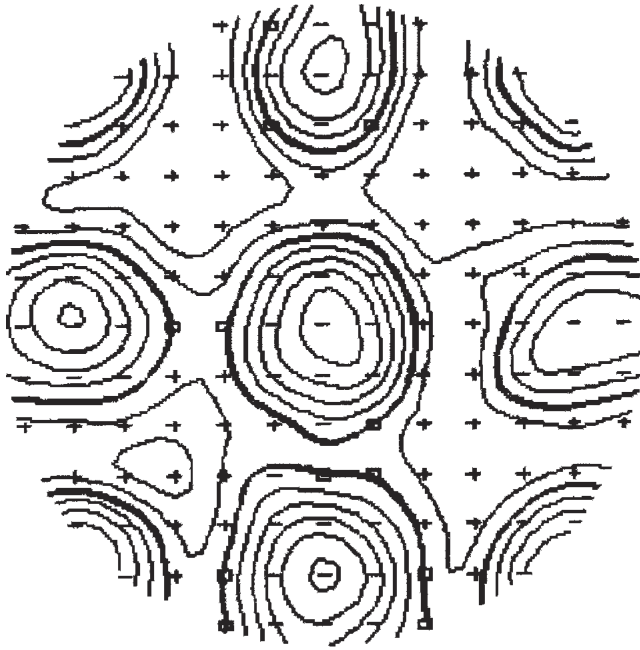

Fig. 3. Oxide film thickness contour map for procedure A single side lamp 1,100°C–1 sec RTO process for patterned wafer-type A2 (p-type substrate, HF clean). Mapped region is 50-mm diameter at wafer center. Contours spaced 1% (0.28 nm, 1.8°C). Mean thickness is 2.85 nm (2.70–2.95 nm range).

The contour spacing is equivalent to 1.8°C, and the temperature range is 8°C. The scanning ellipsometer was also used to make across-wafer diameter scans of $t_{ox}(x,0)$ along the x-axis and $t_{ox}(0,y)$ along the y-axis directions (Fig. 2). These data were converted to temperature distributions, T(x,0) or T(0,y), and average values of T_{00} and T_{20} (defined in Eq. 11 and illustrated in Fig. 2) were calculated. The difference $T_{00} - T_{20}$ gives the peak-to-peak variation in effective process temperature along an axis. Results for $T_{00} - T_{20}$ obtained by RTO for wafer types A1 and A2 in the three RTP systems are presented in Table IIIA.

Implant-anneal RTA processes were monitored by mapping sheet resistance with a four-point scanning probe (CDE ResMap). An example of the variation in sheet resistance along a wafer diameter is shown in Fig. 4 (x-axis scan, 381 probe points, 0.5-mm spacing). These results were obtained for three epi-type B2 wafers (Table I) that received the furnace spike RTA process of procedure B (Table IIB) at temperatures of 1,025°C, 1,050°C, and 1,075°C. The separation between adjacent R_s curves conveys the scale of the temperature sensitivity (~0.68°C/Ω). The oscillatory variation of R_s with x (period L = 2 cm) indicates a 1.6°C peak-to-peak variation of effective process temperature, which is substantially smaller than the 25°C interval between traces. These data also show that the squares areas (e.g., at x = 0) received a slightly higher process temperature (lower R_s) than the intervening field regions. The four-point probe was also used to probe sites on the sublattice points illustrated in Fig. 2 (a total of 1,129 points on a 5 mm × 5 mm square grid). The R_s map was then calibrated with an experimentally determined T versus R_s curve to find average values of T_{pq}, defined by Eq. 11, at the six (pq) points illustrated in Fig. 2.

Temperature differences, $T_{00} - T_{20}$, for wafer types A1 and A2 in procedure A are presented in Table IIIB. For wafer types B1, B2, and B3 of procedure B, $T_{00} - T_{20}$ and $T_{00} - T_{22}$ are shown in Table IV (results for two wafers in each test were averaged).

In order to validate that the patterned films cause these temperature differences, two control experiments were performed with the single-side lamp

Table IIIA. RTO Process Results for Procedure A; $T_{00} - T_{20}$ is Maximum Temperature Variation along the x-axis (Fig. 2)

Wafer Type A1 (Field: Si_3N_4/poly-Si/SiO_2)					
Sequence No.	**RTP System**	**Temperature (°C)**	**Time (sec)**	**O_2 Pressure (torr)**	**$T_{00} - T_{20}$ (°C)**
1	Furnace	1,050	150	760	10.7
2	Dual side lamp	1,100	60	760	19.4
3	Dual side lamp	1,100	<1	760	25.2
4	Single side lamp	1,050	150	700	33.9
5	Single side lamp	1,100	60	700	35.6
6	Single side lamp	1,100	1	700	36.3
7	Single side lamp	1,100	1	80	37.5
Wafer Type A2 (Field: Si_3N_4/SiO_2)					
Sequence No.	**RTP System**	**Temperature (°C)**	**Time (sec)**	**O_2 Pressure (torr)**	**$T_{00} - T_{20}$ (°C)**
1	Furnace	1,050	150	760	–3.1
2	Dual side lamp	1,100	60	760	–3.4
3	Dual side lamp	1,100	<1	760	–5.5
4	Single side lamp	1,050	150	700	–6.8
5	Single side lamp	1,100	60	700	–6.6
6	Single side lamp	1,100	1	700	–7.9
7	Single side lamp	1,100	1	80	–8.8

Table IIIB. RTA Process Results for Procedure A; $T_{00} - T_{20}$ is Maximum Temperature Variation along x-axis (Fig. 2)

Wafer Type A1 (Field: Si_3N_4/poly-Si/SiO_2)				
Sequence No.	RTP System	Temperature (°C)	Time (sec)	$T_{00} - T_{20}$ (°C)
1	Furnace	1,050	<1	8.5
2	Furnace	1,050	1	7.4
3	Single side lamp	1,050	1	29.5
Wafer Type A2 (Field: Si_3N_4/SiO_2)				
Sequence No.	RTP System	Temperature (°C)	Time (sec)	$T_{00} - T_{20}$ (°C)
1	Furnace	1,050	<1	−6.9
2	Furnace	1,050	1	−5.9
3	Single side lamp	1,050	1	−7.5

system. Three unpatterned, bulk n-type B-implanted wafers, which were annealed in the same way as the patterned wafers of procedure A, yielded the result $T_{00} - T_{20} = 0.2 \pm 1.0$°C. In addition, two patterned wafers of type A2 processed with the patterned surface facing the lower reflector (the unpatterned surface facing the lamps), i.e., upside down, yielded the result $T_{00} - T_{20} = -0.4 \pm 1.4$°C. These two findings of a null temperature difference, to within experimental uncertainty, were obtained because unpatterned surfaces of the wafers were exposed to the heating lamps in each control test. The next section presents the model analysis of the temperature differences on the patterned wafers.

ANALYSIS OF THE RESULTS

The experiments presented in this paper have tested three types of patterned films, three types of wafer substrates, two types of RTP processes, and three types of RTP systems. A general observation drawn from the results of procedure A, which compared the three RTP systems, is that within-wafer temperature variations are the least for the furnace RTP system, the greatest for the single-side lamp RTP system, and in between for the dual-side lamp system. The furnace RTP system produces less overall dependence of within-wafer temperature differences on either the type of film pattern or the type of wafer substrate, when compared to the wide range of temperature differences produced by the single-side lamp RTP system.

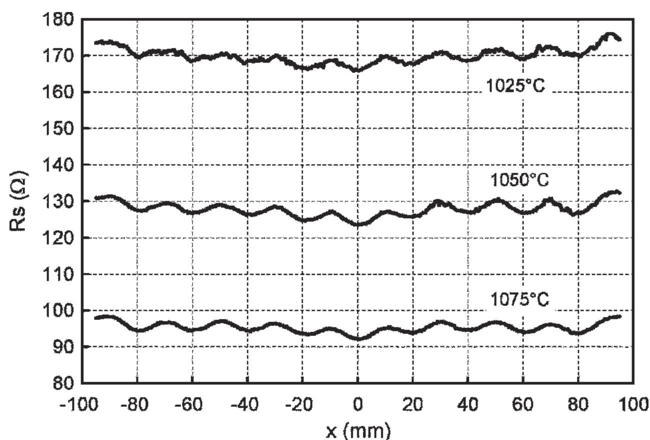

Fig. 4. Sheet resistance versus x for furnace spike 1,050°C RTA process on patterned wafer-type B2 (epi substrate, As^+ implant) at temperatures indicated; procedure B.

When the effective process temperatures in the field and squares areas are compared, areas with bare Si reach higher temperatures than areas coated with Si_3N_4/poly-Si/SiO_2 (wafer type A1) and lower temperatures than areas coated with Si_3N_4/SiO_2 (wafer type A2). For all wafers of procedure B, the squares areas coated with SiO_2 reach higher temperatures than the field areas coated with poly-Si/SiO_2. When the three types of substrates used in procedure B are compared, the within-wafer temperature differences for SOI substrates are systematically smaller than for bulk or epi substrates.

The RTO processes, which examined the influence of dwell time at maximum temperature, show that within-wafer temperature differences for 1-sec oxidations are larger by 25% for dual-side lamps and 10% for single-side lamps, when compared to oxidations of 60 sec or longer duration (Table IIIA). Temperature variations are larger in spike processes, when compared to soak processes, because of the comparatively larger influence of ramp up, where heating power exceeds that in steady state. Short duration (1-sec) RTO and implant RTA processes with similar temperature-versus-time functional forms were compared in procedure A in the single-side lamp system. Within-wafer temperature differences for the A1 and A2 wafers, as determined by either RTO (Table IIIA) or RTA (Table IIIB), are nearly the same. This reproducibility indicates that pattern-induced differences in effective process temperature depend primarily on the type of film pattern, rather than on the type of process that is used for determining the effective process temperature (e.g., details such as diffusion and activation energy). Thus, the steady-state models presented in this paper should have general validity in interpreting experimental results, with the caveat that, in theory, effective process temperature and effective heating power include portions of the RTP cycle where temperature is ramped.[17]

Table IV. Spike RTA at 1050°C Process Results for Procedure B*

Sequence No.	Wafer Description	RTP System	$T_{00} - T_{20}$ (°C)	$T_{00} - T_{22}$ (°C)	T_δ (°C)
1	Bulk	Furnace	1.6	2.2	4.1
2	Bulk	Single side lamp	21.2	27.9	51.7
3	Epi	Furnace	1.6	2.2	4.1
4	Epi	Single side lamp	22.1	29.0	55.7
5	SOI	Furnace	6.9	9.0	17.3
6	SOI	Single side lamp	7.3	9.5	18.2

*Wafers implanted beneath pattern on upper side (prior to film deposition) with As^+ at 10 keV, 10^{16} cm^{-2}. R_s is mean sheet resistance measured after stripping pattern films. $T_{00} - T_{20}$ is maximum temperature variation along the x-axis (Fig. 2); $T_{00} - T_{22}$ is maximum temperature variation along direction x = y (Fig. 2); and T_δ is determined by fitting Eq. (12) to all points in temperature map.

The RTP chamber models were tested using the experimental results for pattern-induced temperature differences from 12 wafer temperature maps obtained in procedure B (two RTP systems × three wafers types × two wafers in each test = 12 data sets). The spike-RTA data of procedure B were selected for analysis because the wafers have nominally identical film patterns. Six temperature differences, $T_{00} - T_{pq}$, corresponding to the six test points, (pq), in Fig. 2, were determined from the temperature map of each wafer. The function in Eq. 12, with S_{pq} defined by Eq. 13, was then fitted to the data for $T_{00} - T_{pq}$ using 13 adjustable parameters: a single value of s for all wafers and 12 individual values of T_δ for each wafer. The fit yields s = 0.522. The fitted parameters T_δ for the two wafers in each test were averaged and are presented in Tables IV and V. The temperature difference data of procedure A were fitted with fixed s = 0.522 and the results for T_δ are presented in Table IV. The uncertainty in s is estimated to be approximately ±0.05. The statistical uncertainty in each T_δ is approximately 2°C; the global systematic uncertainty in T_δ (primarily due to the uncertainty in s) is approximately 10%. One may interpret T_δ as the temperature difference between the field and squares areas in a pattern of length scale, L, that is large compared to the transverse thermal diffusion length, L_d, and where s = 1.

A comparison between model and experiment for within-wafer temperature differences is presented graphically as plots of S_{pq} versus R_{pq} in Fig. 5a for the furnace RTP method and Fig. 5b for the single-side lamp RTP method, where R_{pq} is the distance between the center of a square and the test point (pq), given as $R_{pq} = 1/4(p^2 + q^2)^{1/2}L$. The data points for S_{pq} are the normalized temperature differences, $(T_{00} - T_{pq})/ T_\delta$, which are determined experimentally with the fitted T_δ parameters. The model function for S_{pq} is determined from Eq. 13 with the fitted s parameter and is plotted as cross-hair symbols. The error bars are standard deviations in the data corresponding to the six wafers processed in each of the RTP systems. One notes that the agreement between the model and experiment is 10% or better, even though the within-wafer temperature differences (T_δ) among the wafers vary by a factor of 8 (Table IV). Moreover, the deviation between model and experiment, which appears to have a systematic dependence on the site (pq), is about the same for each type of RTP system.

The above results show that temperature differences induced by emissivity patterns can be generally represented by the results for T_δ that are presented in Table V. Predictive models for the RTP chambers take into consideration the temperature of the field area, represented by $T_1 = T_0 - T_\delta$, and the temperature of the squares areas, represented by $T_2 = T_0 + T_\delta$, where T_0 = 1,050°C.

The furnace RTP system is modeled by Eq. 26, which assumes that the chamber walls diffuse and randomize internal reflections. Although chamber reflectivities have not been determined à priori, the furnace provides a nearly blackbody environment, so it is modeled by using a small reflectivity parameter $\rho_U = 0.01$ for the upper-chamber

Table V. Experimental and Model Results for Temperature Difference Parameter T_δ, Defined in Eqs. (10) and (11), for RTA at 1050°C

Procedure	Wafer Type	Wafer Description	RTP System	Experiment T_δ (°C)	Model T_δ (°C)
A	A1	Bulk	Furnace	18.7	17.9
A	A1	Bulk	Single side lamp	74.4	67.2
A	A2	Bulk	Furnace	−14.9	−10.7
A	A2	Bulk	Single side lamp	−18.9	−21.2
B	B1	Bulk	Furnace	4.1	6.3
B	B1	Bulk	Single side lamp	51.7	49.9
B	B2	Epi	Furnace	4.1	6.6
B	B2	Epi	Single side lamp	55.7	51.1
B	B3	SOI	Furnace	17.3	13.2
B	B3	SOI	Single side lamp	18.2	14.0

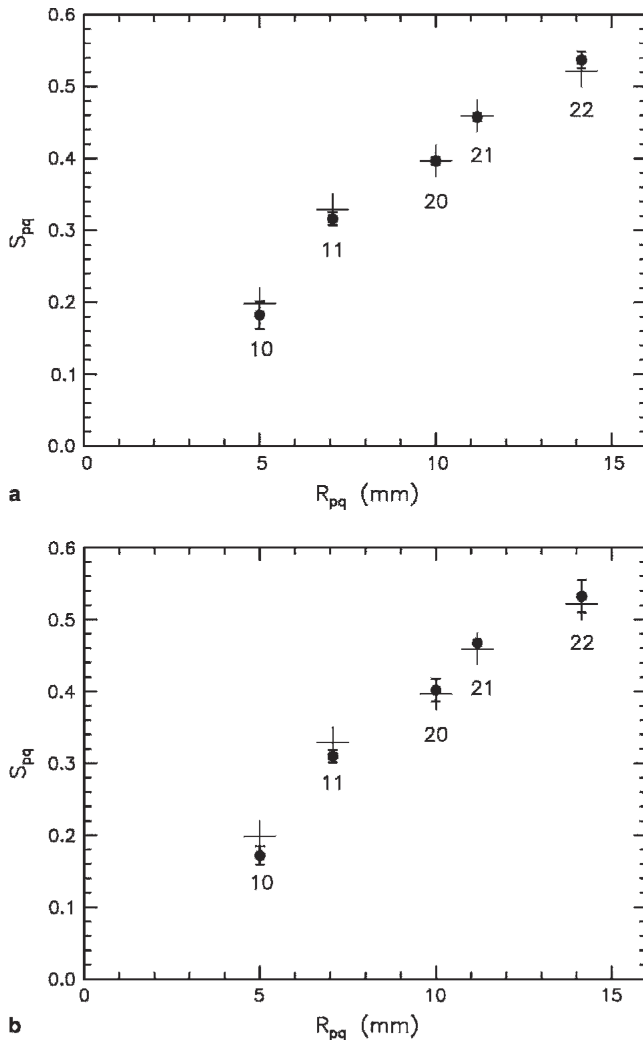

Fig. 5. Normalized temperature difference parameter, S_{pq}, for patterned wafers of procedure B as function of distance from the center of square, $R_{pq} = 1/4\ (p^2 + q^2)^{1/2}L$, for (a) furnace RTA and (b) single-side lamp RTA. Filled circles: data via Eq. 12 with s = 0.522; and cross-hair symbols: theory from Eq. 13.

reflectivity in Eq. 26. The quartz support structure below the wafer is expected to contribute to additional reflections, so the lower-chamber reflectivity is estimated as $\rho_L = 0.05$. The power ratio parameter p, which is defined in Eq. 27, depends on the furnace radiation impinging on the wafer from the upper and lower surfaces, P_U and P_L, respectively, and is treated as a fitting parameter. The freely radiating hemispherical emissivities and absorptivities in Eq. 26 are taken from the calculated values presented in Table I. Fitting Eq. 26 to experimentally determined T_1/T_2 yields a power ratio $P_L/P_U = 0.494 \pm 0.1$. This analysis also yields theoretical or model values for T_δ, which are presented in Table V adjacent to the corresponding experimental values for T_δ.

The power ratio can be interpreted by considering the approximate expression $P_L/P_U \approx (T_L/T_U)^4$, where T_L and T_U represent effective furnace temperatures above and below the wafer, respectively. Estimating the heat balance of Eq. 25 by the expression $2T_0{}^4 \approx T_L{}^4 + T_U{}^4$, one finds $T_L \approx 920°C$ and $T_U \approx 1{,}150°C$. The temperature distribution in the furnace (a vertical gradient) spans a significantly larger range, typically from ~150°C to ~1,350°C.

The single-side lamp RTP system has reflectors close to the wafer that partially randomize wafer reflections, so it is modeled by summing a fraction f_{MIX} of the formula for $(T_1/T_2)^4$ for fully mixed reflections given by Eq. 26 and a fraction $(1 - f_{MIX})$ of the formula for $(T_1/T_2)^4$ for unmixed reflections given by Eq. 18. Equation 18 is written in terms of effective emissivities and absorptivities, which are computed according to Eqs. 14 and 15 using the calculated freely radiating emissivities and absorptivities given in Table I. For single-side heating, one has $P_L = 0$, so that the expressions of Eqs. 18 and 26 do not depend on P_U. The best fits of this model to the data for T_1/T_2 are obtained with $\rho_U = 0.72$, $\rho_L \approx 0.05$, and $f_{MIX} = 0.31$. The uncertainty in reflectivities is 0.05 and the uncertainty in f_{MIX} is 0.04. The theoretical or modeled T_δ values obtained by this analysis are presented in Table V.

The reflectivity of the upper chamber surface of the single-side lamp RTP system found by this modeling analysis falls significantly below unity, presumably because of lamp optics embedded in the reflector. While the lower chamber surface is highly reflecting at the wavelength of the pyrometer (~0.85 μm), its total effective reflectivity is found to be negligibly small. Low chamber reflectivity promotes rapid wafer cooling during the ramp-down phase of an RTP cycle. Unlike the case of the furnace RTP, 31% of the reflections between the wafer and the upper reflector in the single-side lamp RTP have mirrorlike character, according to the model fit (f_{MIX}). While such reflections help to reduce pattern effects,[6] lamp heating nevertheless produces larger T_δ than furnace heating, and the variability of T_δ among wafer and pattern types is significantly greater, as shown in Table V.

The models for the furnace and single-side lamp RTP systems are capable of replicating the observed pattern-induced temperature differences expressed by T_δ to an accuracy of 3.6°C (one standard deviation in the data of Table V). The corresponding accuracy in determining T_1/T_2 is 0.53%. For the test pattern of this work (L = 2 cm), this corresponds to an accuracy of 1.9°C in predicting the temperature difference between the center of the field areas (T_{22}) and the center of the squares areas (T_{00}). These results are subject to experimental uncertainties in the thickness of the films that are used to compute emissivities and absorptivities, the approximations used to model the RTP systems, and the assumption that temperature distributions are in a steady state.

Experimental results for the maximum within-wafer temperature differences, $|T_{22} - T_{00}|$, for the furnace and single-side lamp RTP systems are presented graphically in Fig. 6. The boxes in the figures denote the mean and ±1 standard deviation of $|T_{22} - T_{00}|$ in each system; vertical lines above and below the boxes extend to the largest and smallest $|T_{22} - T_{00}|$ for each system. The largest

$|T_{22} - T_{00}|$ for the furnace system nearly overlaps the smallest $|T_{22} - T_{00}|$ for the single-side lamp system. The difference between heater and wafer temperature in lamp RTP is larger than in furnace RTP by an order of magnitude ($|T_H - T_o| \sim 1{,}000$ versus 100°C), and this causes pattern-induced temperature variations in lamp RTP that are larger than in furnace RTP by a factor of 4.

The expression of Eq. 10 can be used to extrapolate the temperature differences between field and squares areas, $T_{22} - T_{00}$, to arbitrary pattern spacing, L. Combining the theoretical expression for s in the limit $(T_{22} - T_{00}) << T_0$,

$$s = \sum_{n = 1,3,\ldots}^{\infty} (-1)^{(n-1)/2}(4/\pi n)(1 + L_d^2 k_n^2)^{-1} \quad (33)$$

With the experimental result, $s = 0.522 \pm 0.05$, one obtains an estimate for the diffusion length, $L_d = 0.365 \pm 0.032$ cm. This may be compared to $L_d = (\lambda_{\|} d/8\varepsilon_0 \sigma T_0^3)^{1/2} = 0.49$ cm that is calculated with $\lambda_{\|} = 24.6$ W/m-K,[18] $d = 0.725$ mm, $\varepsilon_0 = 0.7$, and $T_0 = 1{,}050$°C. Using the relationships $T_{22} - T_{00} = sT_\delta$ and $T_\delta = (T_2 - T_1)$, the temperature difference, normalized to the $L/L_d \rightarrow \infty$ limit, is given by the expression

$$\frac{T_{22} - T_{00}}{T_2 - T_1} = \sum_{n=1,3,\ldots}^{\infty} (-1)^{(n-1)/2} \frac{(4/\pi n)}{1 + (2\pi n L_d/L)^2} \quad (34)$$

Equation 34, which is plotted in Fig. 7 with the experimental value for L_d at $T_0 = 1{,}050$°C, gives a model prediction for the temperature differences, relative to the temperature differences in the limit of large L/L_d, as a function of the pattern dimension, L.

CONCLUSIONS

Pattern-induced within-wafer temperature distributions were determined for furnace and lamp-based RTP systems by monitoring oxidation or implant spike-anneal processes. Test wafers (bulk n and p, p/p+ epitaxial, and silicon-on-insulator) were prepared by film deposition (combinations of poly-Si, SiO_2, or Si_3N_4) and etching to produce a pattern of 1-cm squares spaced 2 cm apart on a square grid, where the squares and surrounding field areas have different thermal absorptivities and emissivities. The furnace RTP method is found to produce smaller pattern-induced temperature differences than lamp-based RTP methods by nearly a factor of 4. The lamp-based RTP system shows more than 3 times wider variability of within-wafer temperature differences with films and wafer substrates, when compared to the furnace RTP method. This dependence on the pattern length scale is derived by modeling (Fig. 7).

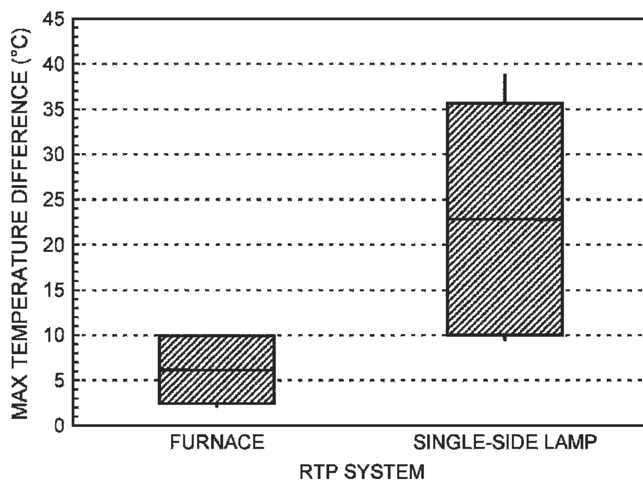

Fig. 6. Maximum within-wafer temperature differences ($|T_{22} - T_{00}|$ as defined in the text) observed on the patterned wafers processed with furnace and single-side lamp RTP systems. Bars within boxes are means; heights of boxes are 2 standard deviations; and extension bars denote the data range.

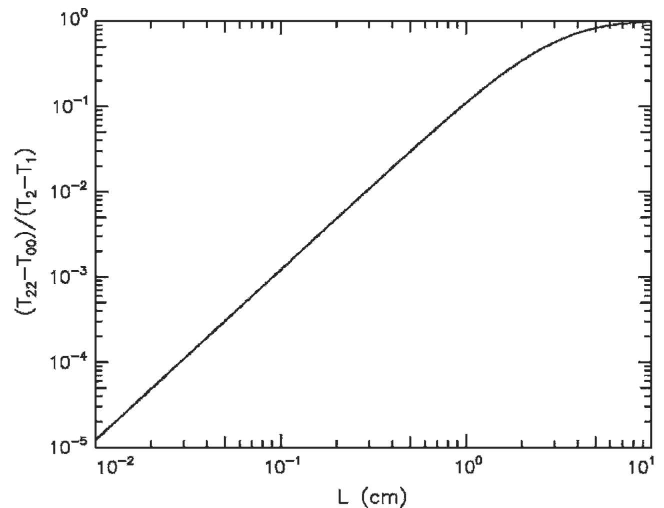

Fig. 7. Temperature difference T_{22}–T_{00} (between squares and field areas, respectively) normalized to large L limit as a function of pattern periodicity distance, L, from Eq. 34 for thermal diffusion length $L_d = 0.365$ cm at $T_0 = 1{,}050$°C.

Models for processing patterned wafers in furnace and lamp-based RTP systems were presented and applied to calculate temperature differences for various patterned wafers. Wafer temperatures were mapped at test points that are commensurate with the periodicity of the pattern. Steady-state temperature models can explain data for within-wafer temperature differences for spike anneals to an accuracy of 10% (±1.6°C on average). Parameters characterizing the furnace RTP system (relative heater power delivered to the upper and lower wafer surfaces) and single-side lamp system (chamber reflection characteristics) were determined by fitting analytical models to within-wafer temperature difference data. Experiments with RTO processes in the single-side lamp system indicate that temperature ramping associated with spike processes systematically increases within-wafer temperature variations by about 10%, when compared to soak processes.

On average, the furnace RTP system produces within-wafer temperature differences that are only 27% as large as those produced in the single-side

lamp RTP system. The variation of temperatures among the wafer and pattern types in the furnace RTP is 29% of such variation in the lamp RTP system. While it was not directly examined in this experiment, the emissivities of structures surrounding the wafer (support ring in single-side lamp RTP and passive ring in furnace RTP and dual-side RTP) are generally different from the emissivity of the wafer. This can produce temperature differences at the wafer edge that are comparable to those observed in this work. While the present results were obtained with a special pattern suitable for experimentation and modeling, the relative magnitudes of the pattern-induced temperature differences observed in the tested RTP systems could be applied to device and integrated circuit processing, where the emissivities and absorptivities are less well characterized.

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