Advances in Microelectronic Processing

N.M. Ravindra and A. Kumar

N.M. Ravindra

Silicon semiconductor technology has been a key contributor to the remarkable economic growth of the U.S. high-technology industry in the last decade. The Semiconductor Industry Association[1] and its member companies have worked collectively to advance the competitiveness of the $76 billion U.S. chip industry. This industry, which is the largest value-added sector in the U.S. economy, provides high-quality employment to hundreds of thousands of U.S. citizens and is projected to grow at a compound annual rate of 15 percent for the next several years. The growth will create opportunities for new applications that will spawn new industries and it will ensure the continued vitality of many of the information technology industries. Semiconductors have had an unprecedented impact on the economy because the industry has provided its customers with exponential increases in performance-per-unit-expenditure of resources for the last several decades.

However, several questions arise amid the ongoing upheaval in semiconductor-technology-related stocks, the semiconductor industry, the job market as a whole and its influence on the stock market. From a philosophical standpoint, have we just become too materialistic or too dollar driven? Or, does the economy drive technology and not the other way around? Consider, for example, the constant updates and upgrades in the personal computer software and hardware markets and the demand for these products. If necessity is the mother of invention, why are these continuous evolutions in the personal-computer industry needed? The semiconductor industry could be accused of lacking social responsibility for producing enormous quantities of electronic garbage if the older versions of microprocessors cannot be recycled.

Although silicon-wafer diameter has been increasing, physical-device dimensions have been shrinking. The goal in silicon-device technology has been to improve yield, reduce cost, and improve chip performance. In this process, a large number of unsettling trends have emerged that, if not addressed, will threaten continued progress and possibly undermine future technology-based economic growth. For example, the physical limits to silicon semiconductor performance are fast approaching. When those limits are reached, a new technological revolution will be forced for which the science base is rather weak.

Industry experts believe that, within six years, the semiconductor industry will face technical challenges for which there are no known solutions.[2] History teaches us that it will now be difficult to introduce new technologies into manufacturing in time to sustain the Moore's Law cadence, even if solutions were available from research today. Integrated-circuit performance is increasingly dependent on the physics of material interfaces between atomic-scale films rather than on bulk material properties, and increasingly dependent on the precise positioning of atoms rather than on the statistical properties of their distributions. As device features shrink, demands on ever-thinning gate dielectrics remain high, driving a need for a better understanding of the physics of atomic-scale materials and processes that would enable the synthesis of novel materials. Examples include the development of new gate dielectric materials, the generation of new inter-level dielectrics and improved conductors for interconnect systems, fabrication of precisely controlled, ultra-thin silicon films, and channel doping in excess of the material density-of-states limit to achieve very low contact resistance. In addition, copper seems to be in place in silicon-integrated circuit manufacturing. This will require and highly compatible diffusion barriers, though.

With these issues in mind, the thin films and interfaces committee of TMS is pleased to present three relevant articles in this issue of *JOM*. In the first article, by Sailesh M. Merchant, Seung H. Kang, Mahesh Sanganeria, Bart van Schravendijk, and Tom Mountsier, the authors focus their investigation on copper/low-k dielectric materials that have been rapidly replacing the conventional aluminum-alloy/SiO_2-based interconnects for the fabrication of state-of-the-art silicon semiconductor devices. The authors present an industry perspective on the advantages of transitioning to copper/low-k interconnects, including materials and process challenges. This paper concludes with reliability concerns associated with devices with copper/low-k interconnects.

A. Kumar

The second article, by S.V. Babu, Y. Li, and A. Jindal, focuses on chemical-mechanical planarization (CMP). As device dimensions continue to shrink, multilevel (>8) interconnects are required for an efficient implementation of complex logic device designs in a single silicon chip. When the number of metal interconnect levels increases, the available depth-of-focus budget of lithographic tools imposes stringent planarity requirements that can only be met currently by CMP. This paper reviews some of the recent advances in the fundamental understanding of the interplay between the mechanical and chemical components of the material removal process during CMP of copper and tantalum films.

The third and final article, by Rajnish K. Sharma, Ashok Kumar, and John M. Anthony, focuses on recent developments in high dielectric constant gate insulator materials for future ultra large scale integration devices below 100 nm technologies. Since conventional gate oxide poses problems as device features are scaled down to nanometers, it becomes necessary to develop new gate dielectric materials that show properties similar to SiO_2 and are compatible with current, complementary metal-oxide semiconductor technology. As the thickness of silicon dioxide approaches less than 1.5 nm, the leakage current becomes higher than 1 A/cm^2 and a significant increase in tunnel current is observed. Therefore, it is necessary to develop materials that provide excellent electrical characteristics.

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References

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2. *The 2000 International Technology Roadmap for Semiconductors* (San Jose, CA: Semiconductor Industry Association, 2001).

N.M. Ravindra is with the Department of Physics at the New Jersey Institute of Technology and the JOM advisor from the Thin Films and Interfaces Committee of the TMS Electronic, Magnetic & Photonic Materials Division. A. Kumar is with the Center for Microelectronics Research at the University of South Florida.