The Magnetic Field-Assisted Assembly of Nanoscale Semiconductor Devices: A New Technique

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Magnetic field-assisted assembly is an integration technique for the efficient placement of a large number of nanodevices into receptor sites etched in semiconductor wafers with or without circuitry. The diverging flux from a magnetic field source helps in attaching heterostructure nanodevices into wafers. Various approaches of magnetic field-assisted assembly using air pressure, vibration assistance, fluid, and feed tape are briefly explained in this article. Magnetic field-assisted assembly is anticipated to become a manufacturing approach that will be driven by its simplicity and promise of high yield at low cost.

INTRODUCTION

In a new approach, nanoscale semiconductor devices are assembled on a substrate or embedded with silicon integrated circuits using a magnetic field. Using this method, nanodevices are placed via a magnetic field in patterned recesses on the surface of an integrated circuit wafer. After the recesses are filled with nanostructures, the wafer is processed further to convert the nanostructures into devices that are integrated with the underlying circuitry.

The heterogeneous integration of high-performance electrical, microelectromechanical (MEMS), and optoelectronic devices onto the same substrate is important for the development of low-cost and/or high-performance/density microsystems. The integration of different materials and device functions has significant applications in the market. However, some problems are inherent when combining different materials, such as differences in thermal expansion coefficient between materials and process conditions for device fabrication. For example, the thermal expansion mismatch is very large between silicon, the primary material of interest for large-scale high-density integrated circuits, and III-V compounds, the materials of choice for optoelectronic and microwave devices and circuits.[1]

A great range of sensor and actuator devices currently are able to be produced through microengineering.[2] This fabrication method consists mainly of bulk and surface silicon micromachining, laser micromachining, and LIGA (a German acronym for lithographie galvanoformung abformung). In the next generation of MEMS and nanoelectromechanical systems (NEMS), micro- and nanomechanical sensors and actuators will be integrated with electronic and optical components to produce powerful and complex microsystems.[3,4] The integration of MEMS and NEMS sensors and actuators with other classes of nanocomponents—electronic, optical, and electromechanical devices—onto a single substrate has the potential to create powerful and complex micro- and nano-systems.[3,4]

As the market for low-cost and high-performance electronic, optoelectronic, and electromechanical integrated circuits grows, many new assembly and integration techniques must be developed. It has become increasingly important to integrate high-performance, low-cost electronic, optoelectronic, and/or radio frequency components onto dissimilar substrates. To improve system performance and reduce assembly cost, often compound semiconductor devices must be integrated monolithically into active circuitry contained in the substrate. Of primary interest is integrating compound semiconductor devices with silicon complementary metal oxide semiconductor technology in order to increase the number of on-wafer functions available and ultimately reduce the cost, size, and weight of micro- and nano-device based systems.

As the dimensions of microelectronic, optoelectronic, and MEMS devices and systems decrease to the nanoscale, and as their complexity increases, there is a need to use assembly and integration techniques to simplify the processing of these devices. Several approaches have been proposed for fabricating and assembling different microdevices (or generally microstructures) onto a substrate. Such proposed approaches include selective area growth,[5–8] flip-chip bonding,[9–11] epitaxial lift-off,[12–15] electrostatic alignment,[16] fluidic self-assembly,[17–23] magnetically assisted statistical assembly,[24] and magnetic self-alignment.[25,26] Each of these methods has its advantages, drawbacks, and technological issues that are application specific.

Magnetically assisted statistical assembly[24] is a new technique for the monolithic heterogeneous integration of compound semiconductor devices with silicon integrated circuits. This method uses statistical self-assembly with magnetic retention to locate compound semiconductor device heterostructures in recesses patterned into a wafer that also contains integrated circuits.[24] In this method, selectively etched heterostructure nanopills with magnetic layers on them are slurried over a substrate with patterned recesses of matching shapes and sizes. The high-coercivity magnetic layers at the bottom of the patterned recesses in the wafer locate and attach the nano-pills to the recesses because of strong short-range magnetic attractive forces.[24] The authors' approach[27] differs from this promising technique in many important ways.

THE ASSEMBLY PROCESS

The magnetic field-assisted assembly[27] begins with the preparation of the substrate and the heterostructure nanounits. The entire assembly process is shown schematically in Figure 1. The starting material can be a separate substrate (insulator) or semi-processed wafer or final wafer with integrated circuitry on it. In all cases, recesses are patterned into either the dielectric layer covering the wafer surface or the surface of the insulator, as shown in Figure 1. The shape and thickness of the nanounits match the shape and depth of the recesses formed on the surface. A ferromagnetic material with a high coercive field, such as cobalt or nickel or a cobalt-platinum alloy, is deposited on the insulator substrate or on the wafer. The magnetic layer is patterned to form simple and complex features in the bottom of the recesses. The patterned magnetic layer is subsequently magnetized to act as a host for heterostructure nanounits, and the wafer is ready for assembly.

A soft magnetic material layer is deposited on a separate substrate wafer. Patterned holes of precise dimensions are formed on the magnetic material (guide layer), the shape of which should match the patterned recesses formed in the insulating layer on the substrate wafer and the shape of the heterostructure nanounits. This guide layer is then etched free from its original substrate using a selective etch. A soft magnetic guide layer is employed on top of the patterned recesses in the insulating layer of the substrate wafer and precisely aligned.

The next step is the formation of heterostructure nanounits, which act as guests to a host substrate. It begins with a separate III-V compound semiconductor such as a GaAs or an InP wafer. Under optimum conditions, the heterostructure nanounits from which the devices are being integrated are fabricated on the appropriate wafer. A thin layer of cobalt or nickel is deposited on the backside of the wafer. An etch-free layer is deposited on the heterostructure substrate. The heterostructure nanounits are patterned in a shape and size similar to that formed on the substrate wafer. These heterostructure nanounits are then freed from their substrate into individual heterostructure nanounits using etchants.

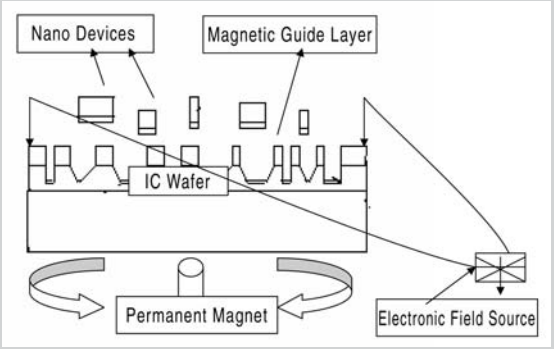

Figure 1. A schematic of the magnetic field-assisted assembly method of integrating nanodevices and integrated circuits.[27]

The heterostructure nanounits, having a soft magnetic layer, now play a guest role for the host substrate wafer and are ready for the assembly process.

During assembly,[27] the magnetic field is applied on the backside of the patterned substrate wafer using a moving magnetic field source, which is continuous and/or oscillatory so as to cover the entire portion of the backside of the wafer. The heterostructure nanounits with a soft magnetic layer are sprinkled or placed on a magnetic guide layer with patterned holes on the top of the patterned recesses in the insulating layer on the wafer with an integrated circuit in it or on the magnetic guide layer with patterned holes on the top of the patterned recesses in the substrate (insulator). When the magnetic field is applied across the patterned holes formed in the magnetic guide layer, each recess acts as a crack, and a north pole and south pole form at the edge of the crack. The magnetic field exits the north pole and re-enters at the south pole. The magnetic field spreads out when it encounters the small air gap created by the crack because air cannot support as much magnetic field per unit volume as the magnet. When the field spreads out, it appears to leak out of the material and, thus, it can be called a flux leakage field.[27] This, combined with the magnetic field created at the backside of the wafer, results in heterostructure nanounits that are attracted to the patterned holes in the magnetic guide layer. These nanounits pass through the holes and become attached to the magnetic layer at the bottom of the patterned recesses in the wafer or substrate. They are retained there by a strong short-range magnetic attractive force. The size and shape registry between the heterostructure nanounits and the patterned recesses in the substrate wafer along with the flux leakage field created on the patterned holes in the magnetic guide layer permits only those nanounits to move to their respective position, as does the supporting magnetic field created on the backside of the wafer. When these heterostructure nanounits settle into a recess, the strong short-range magnetic attractive force will keep the nanounits from being removed from the recess by another nanounit.

Heterostructure nanounits will be fixed permanently once they settle in the recesses using a polymer layer. The polymer layer will also fill in any voids and will facilitate in planarizing the surface. State-of-the-art monolithic photolithographic techniques are used to convert the heterostructure nanounits into devices and integrate them with the pre-existing electronics in the wafer.[24]

Optimized air pressure and vibration are used respectively as facilitators of the magnetic assembly process. Magnetic-field assisted assembly can also be achieved using a liquid medium. The plurality of heterostructure nanounits is preferably slurried using low-viscosity, non-corrosive fluid such as kerosene over the surface of the recessed wafer or on the magnetic guide layer.[27]

Another approach to magnetic field-assisted assembly using feed tape[27] is illustrated in Figure 2. A substrate is patterned with multiple recesses that are shaped to receive correspondingly matched heterostructure nanounits. The heterostructure nanounits are temporarily attached to feed tape. Upon completion of the magnetic self-assembly of heterostructure nanounits, individual units are attached to the matching recesses on the substrate. Feed tape portions are guided by wheels. A magnet

moves adjacent to and relative to the substrate in a direction parallel to the substrate. Equivalently, the substrate moves continuously relative to guide wheels. The feed tape portion that is parallel to the substrate executes little or no relative motion in the direction parallel to the substrate. The magnet executes continuous and/or oscillatory movement in any direction with respect to the substrate.

Exposed faces of the heterostructure nanounits on the feed tape have coatings of the material with high magnetic permeability, such as unmagnetized ferromagnetic material with a low coercive field. The coating becomes magnetized when placed near an external magnet. The coating may also include a physical or chemical agent for subsequent permanent bonding of heterostructure nanounits to the substrate. The magnetic field produced by the moving magnet magnetizes the coating. The ensuing magnetic force of attraction pulls the heterostructure nanounits off the tape and into recesses in the substrate. Heterostructure nanounits are pulled preferentially into recesses by several physical characteristics of the magnetic and contact forces.

The direct magnetic field-assisted assembly method[27] does not rely on statistical randomness. Its desirable attributes, when compared to statistical assembly, are, therefore, scalability to rapid assembly of a plurality of heterostructure nanounits on a substrate and avoidance of frustration effects that can lead to assembly errors.

Frustration occurs if the path from one or more heterostructure nanounits to a matching site on the substrate is blocked, or one or more sites on the substrate remain unoccupied owing to the path being blocked. In addition, the magnetic field-assisted assembly requires no liquid such as in the fluidic self-assembly process, leading to the full advantage of a clean and dry environment. It provides a new technique for assembling and integrating heterostructure nanodevices onto a silicon wafer or on a separate substrate. The magnetic field-assisted assembly process is carried out in such a manner as to avoid damaging the pre-existing electronics on the substrate. This process takes full advantage of very large diameter silicon wafers.

CONCLUSIONS

This technique preserves all the advantages of the state-of-the-art semiconductor-based processing and avoids compromising or damaging the pre-existing electronics on the wafer. Low-cost, efficient, and reliable, this method permits wafer-level batch processing and monolithic integration. The yield is significantly enhanced by intermediate testing of the device and circuit so that assembly of defective devices can be avoided.

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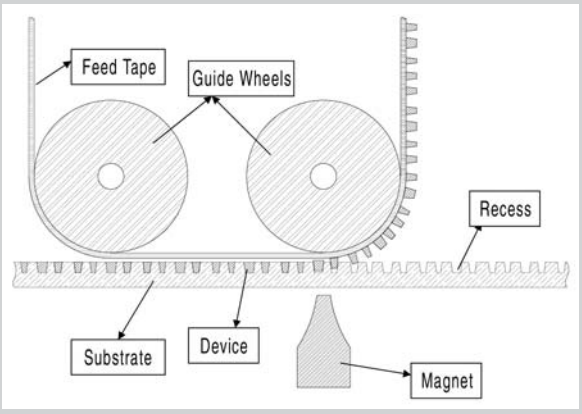

Figure 2. A schematic view of the magnetic field-assisted assembly process using feed tape.[27] Figure not drawn to scale.

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