Strain-induced lateral self-organization in Si/SiO_2 nanostructures

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We show that strain, arising from the mismatch between Si and SiO_2 thermal expansion coefficients, directs the thermal crystallization of amorphous Si along Si/SiO_2 interfaces, and produces continuous, fully crystallized nanometer thick Si layers with a lateral-to-vertical aspect ratio close to 100:1. These Si nanolayers exhibit a low density of structural defects and are found to be elastically strained with respect to the crystal Si substrate. *© 2010 American Institute of Physics*. [doi:10.1063/1.3290250]

The unprecedented growth of the Si-based electronic industry is largely due to the unique properties of the Si/SiO_2 interface and the ability to fabricate electronic devices using a simple and cost-effective process of crystalline Si thermal oxidation. However, it is well known that Si and SiO_2 have a significant mismatch in their coefficients of thermal expansion,[1,2] and several studies have shown a distortion of the Si crystal lattice near the Si/SiO_2 interface.[3] Is it possible to produce a few nanometer thick strained $SiO_2/Si/SiO_2$ nanostructures controllably, similar to that in traditional fabrication of strained Si using lattice mismatched heteroepitaxy,[4–7] "smart-cut" technology,[8] Si_3N_4 capping of thin silicon-on-insulator (SOI) layers,[9] and porous Si stressors?[10] An interesting approach is to use nanometer thick amorphous Si (a-Si) layers sandwiched between thin SiO_2 layers that can easily be fabricated by Si physical or chemical deposition and converted into nanocrystalline Si by using the process of thermal crystallization.[11] Thermal crystallization of nanometer thick a-Si layers, however, seems to be a largely uncontrolled step, and it is certainly a complicated one;[12,13] depending on the initial a-Si layer thickness, the shape of Si nanocrystals (NCs) can be spherical, oval, pyramidal, and even laterally elongated with bricklike Si NCs separated by grain boundaries.[11,14,15] Different experiments show that these grain boundaries are sources of structural defects (mainly dangling bonds and residues of amorphous Si), and that they are responsible for charge trapping leading to limitations in the device applications of such Si nanostructures.[13] In this letter, we demonstrate that elastically strained Si nanolayers (NLs) with a low-density of grain boundaries and a lateral-to-vertical aspect ratio close to 100 to 1 can be fabricated using controlled thermal annealing of ultrathin a-Si layers sandwiched between ultrathin SiO_2 films.

Samples for this work were fabricated in the form of $SiO_2/a\text{-}Si/SiO_2$ periodic structures on (001) crystalline Si substrates with numbers of periods ranging from one (a single a-Si layer between two SiO_2 layers) to 20 using magnetron sputtering and plasma oxidation (for details see Refs. 11 and 12). Typical thicknesses of the initially a-Si layers were controllably varied between 5 to 20 nm and the thicknesses of the $a\text{-}SiO_2$ separating layers ranged from 2 to 7 nm. As a post-treatment procedure, samples were subjected to rapid thermal and conventional furnace annealing. For samples discussed in this letter, the furnace annealing was performed starting with slow (~5 °C/min) ramping temperature from 350 to 1100 °C. At 1100 °C, samples were kept in the furnace for an hour in a nitrogen atmosphere. To minimize the thermal stress and uncontrollable oxidation, the temperature was then slowly reduced to ~300 °C before the samples were removed from the furnace.

Figure 1(a) shows a transmission electron microscopy (TEM) micrograph of ~20 nm thick initially a-Si layer sandwiched between 5 nm thick SiO_2 layers that had been subjected to a rapid (~30 s) annealing at 350 °C. A nearly spherical Si nucleus 5–7 nm in size can clearly be seen in the middle of the original a-Si layer. After a second ~30 s annealing at 450 °C, the nanocrystalline Si nucleus grew approximately twice as long laterally, but the vertical dimension remained the same [Fig. 1(b)]. After using furnace annealing at temperature of 1100 °C for ~1 h, we observed a fully crystallized ~20 nm thick and several hundred nanometer long Si NL without visible grain boundaries and remnants of a-Si [Fig. 1(c)].

We found that crystallization of the nanometer thick Si layers strongly depends on the annealing conditions such as thermal budget and thermal stress. Figure 2 shows a larger

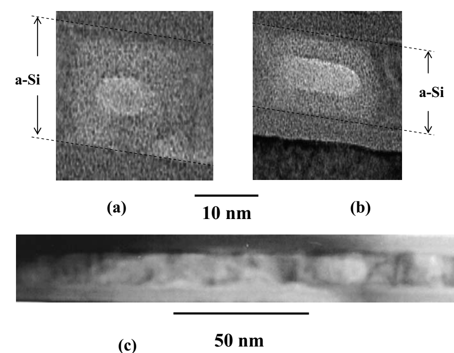

FIG. 1. TEM images of individual Si NCs within an a-Si layer sandwiched between SiO_2 layers at different nucleation stages: (a) after ~30 s rapid annealing at 350 °C and (b) after a second ~30 s annealing at 450 °C. (c) TEM of a fully crystallized, ~20 nm thick Si NL fabricated using ~1 h long furnace annealing at 1100 °C.

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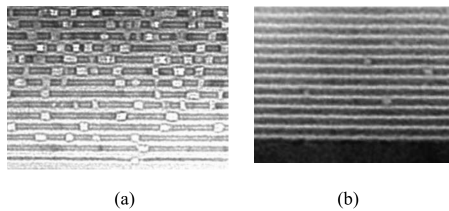

FIG. 2. Larger scale TEM micrographs comparing samples of Si NLs (darker area) sandwiched between SiO_2 layers (lighter area) fabricated by furnace annealing at 1100 °C: (a) without and (b) with slow ramping temperature and thermal stress reduction fabrication steps. In both cases, the nominal Si NL thicknesses are 10 nm.

scale TEM pictures and compares two samples: one fabricated by the standard annealing process[11] [Fig. 2(a)] and the other by using the described slow ramping temperature furnace annealing and slow temperature reduction from 1100 to 300 °C in a nitrogen atmosphere to avoid thermal stress and uncontrollable oxidation [Fig. 2(b)]. It is clear that the sample in Fig. 2(b) shows a significantly lower number of "broken" Si NLs and a lower density of the structural defects associated with the grain boundaries within the Si NLs.

We have examined samples similar to those shown in Fig. 2(b) with high-resolution x-ray diffraction (XRD) reciprocal space mapping. Figure 3 shows the reciprocal space map of a sample with 20 periods of 10 nm thick Si NLs separated by 2 nm thick SiO_2 layers measured around the asymmetric (2 2 4) reflection of the (001)-oriented Si substrate. The diffracted intensity from the Si NLs is elongated in the direction of the reciprocal lattice vector Q_z that corresponds to the layer growth direction. Thus, we have observed the clear signature of elastically strained Si NLs separated by SiO_2 layers. The measured composite strain value for the Si NLs is found to be $\Delta d/d = +6.2 \times 10^{-4}$ [where d is the distance between the (2 2 4) atomic layers], showing that the average Si NL lattice parameter in the growth direction is slightly larger than that in a single-crystal Si substrate. The reciprocal space map also shows that the Si NL average in-plane lattice parameter is the same as that of the Si substrate. The cross section of the reciprocal space map taken along the Q_z direction reveals the layer thickness fringes, and from these fringes we determined the total thickness of the Si/SiO_2 multilayer samples to be 219 nm, which agrees with the total thickness extracted from TEM measurements (220 nm). The observation of the thickness fringes provides additional evidence that the anisotropic Si NL lattice parameters are maintained throughout the entire structure.

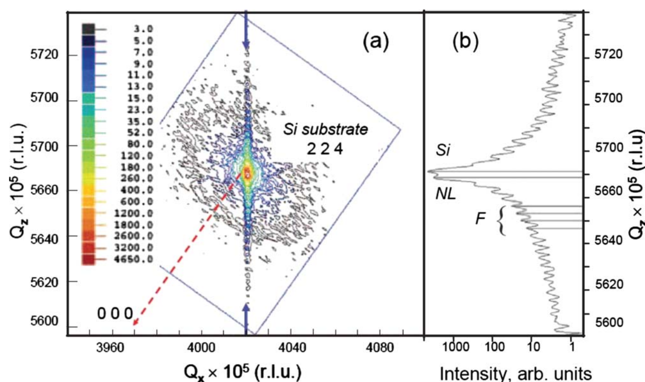

FIG. 3. (Color online) (a) Reciprocal space map of a 20 period Si/SiO_2 multilayer sample consisting of 10 nm thick Si NLs and 2 nm thick SiO_2 alternating layers measured around the (2 2 4) reflection of the (001)-oriented Si substrate. The intensity maximum in the center of the map corresponds to the Si substrate, while the vertically aligned signal originates from the superlattice. The strongest peak just below the substrate peak corresponds to the global strain of the multiple Si NLs. The dark gray (red) arrow shows the direction toward the origin [(0 0 0) point of reciprocal space]. The light gray (blue) arrows indicate the Q_z direction for the cross section of the x-ray diffracted intensity plot presented in (b). The total thickness of 219 nm of the Si/SiO_2 multilayers is determined from the separation between the thickness fringes F, while the strain is obtained from the Si substrate and NL peak separation.

The shape of the reciprocal space map in Fig. 3 is similar to that found in strained, epitaxially-grown semiconductor heterostructures.[16,17] In contrast, a system with a significant density of structural defects (e.g., grain boundaries, dislocations, etc.) and/or a residue of a-Si should exhibit a reciprocal space map with a diffracted signal center moved toward the origin [indicated with a dark gray (red) dotted line in Fig. 3]. Thus, the observation by XRD of elastically strained Si-NL/SiO_2 multilayers confirms that the samples have a low density of structural defects, as also evidenced from the TEM studies.

These results suggest that in nanometer thick Si layers, crystallization near the a-Si/SiO_2 interface is suppressed due to strain arising from the mismatch between the Si and SiO_2 thermal expansion coefficients. The strain field localized near the Si/SiO_2 interface induces Si homonucleation (i.e., nucleation within the Si layer, away from the Si/SiO_2 interface), "directs" the crystallization process parallel to the Si/SiO_2 interface and eventually produces the observed continuous Si NLs with sharp Si/SiO_2 interfaces. By carefully ramping up the annealing temperature and by slowly cooling the sample down, heat stress and a nonuniform heat distribution are avoided, which due to the extremely low thermal conductivity of Si/SiO_2 multilayers[18] might break the Si NLs and produce a smaller laterally dimensioned Si NC. It is significant that this Si nanofabrication process is not affected by multiple Si-NC nucleations within the initially a-Si layer; it is known that small-size (<10 nm) nanocrystals have a significantly reduced melting temperature compared to that in bulk materials.[19–22] In addition, small Si NCs are surrounded by grain boundaries, and that also decreases the local thermal conductivity. Thus, only relatively large, laterally extended Si NLs survive the ~1 h long heat treatment at 1100 °C, while smaller Si NCs surrounded by grain boundaries melt and merge together to form the experimentally observed, continuous Si NLs. During this process, structural defects are pushed toward the Si/SiO_2 interface, where they are either removed due to Si surface reconstruction or passivated by oxygen. In the careful cooling down from 1100 °C to room temperature without breaking up the Si NLs (see Fig. 2), the known mismatch in thermal expansion between Si and SiO_2 produces the observed homogeneously strained Si nanostructures.

In conclusion, carefully performed thermal crystallization and cooling of initially amorphous, nanometer thick Si layers sandwiched between thin SiO_2 layers allows the fabrication of strained continuous Si NLs with a ~100:1 lateral-to-vertical dimension ratio and sharp Si/SiO_2 interfaces. These strained Si NLs are processed using standard Si microfabrication high-temperature treatments and thermal oxidation, and they exhibit a strong potential for employment in three-dimensional device and system integration.

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[1]Y. Okada and Y. Tokumaru, J. Appl. Phys. **56**, 314 (1984).
[2]J.-P. Colinge, *Silicon-On-Insulator Technology: Materials to VLSI*, 3rd ed. (Springer, Boston, 2004), p. 384.
[3]H. Akatsu and I. Ohdomari, Appl. Surf. Sci. **41**, 357 (1989).
[4]R. People, J. C. Bean, D. V. Lang, A. M. Sergent, H. L. Störmer, K. W. Wecht, R. T. Lynch, and K. Baldwin, Appl. Phys. Lett. **45**, 1231 (1984).
[5]R. People and J. C. Bean, Appl. Phys. Lett. **48**, 538 (1986).
[6]T. Tezuka, N. Sugiyama, and S. Takagi, Appl. Phys. Lett. **79**, 1798 (2001).
[7]M. L. Lee, E. A. Fitzgerald, M. T. Bulsara, M. T. Currie, and A. Lochtefeld, J. Appl. Phys. **97**, 011101 (2005).
[8]B. Ghyselen, J.-M. Hartmann, T. Ernst, C. Aulnette, B. Osternaud, Y. Bogumilowicz, A. Abbadie, P. Bessonc, O. Rayssac, A. Tiberj, N. Daval, I. Cayrefourq, F. Fournel, H. Moriceau, C. Di Nardo, F. Andrieu, V. Paillard, M. Cabié, L. Vincent, E. Snoeck, F. Cristiano, A. Rocher, A. Ponchet, A. Claverie, P. Boucaud, M.-N. Semeria, D. Bensahel, N. Kernevez, and C. Mazure, Solid-State Electron. **48**, 1285 (2004).
[9]S. E. Thompson, M. Armstrong, C. Auth, M. Alavi, M. Buehler, R. Chau, S. Cea, T. Ghani, G. Glass, T. Hoffman, C.-H. Jan, C. Kenyon, J. Klaus, K. Kuhn, Z. Ma, B. Mcintyre, K. Mistry, A. Murthy, B. Obradovic, R. Nagisetty, P. Nguyen, S. Sivakumar, R. Shaheed, L. Shifren, B. Tufts, S. Tyagi, M. Bohr, and Y. El-Mansy, IEEE Trans. Electron Devices **51**, 1790 (2004).
[10]O. Marty, T. Nychyporuk, J. de la Torre, V. Lysenko, G. Bremond, and D. Barbier, Appl. Phys. Lett. **88**, 101909 (2006).
[11]L. Tsybeskov, K. D. Hirschman, S. P. Duttagupta, M. Zacharias, P. M. Fauchet, J. P. McCaffrey, and D. J. Lockwood, Appl. Phys. Lett. **72**, 43 (1998).
[12]L. Tsybeskov and D. J. Lockwood, in *Advances in Crystal Growth Research*, edited by K. Sato, Y. Furukawa, and K. Nakajima (Elsevier, Amsterdam, 2001), Vol. 252.
[13]S.-Y. Chung, Y.-M. Kim, J.-G. Kim, and Y.-J. Kim, Nat. Phys. **5**, 68 (2009).
[14]G. F. Grom, D. J. Lockwood, J. P. McCaffrey, H. J. Labbé, P. M. Fauchet, B. White, Jr., J. Diener, D. Kovalev, F. Koch, and L. Tsybeskov, Nature (London) **407**, 358 (2000).
[15]L. Tsybeskov, K. D. Hirschman, S. P. Duttagupta, M. Zacharias, P. M. Fauchet, J. P. McCaffrey, and D. J. Lockwood, Appl. Phys. Lett. **75**, 2265 (1999).
[16]P. F. Fewster, Crit. Rev. Solid State Mater. Sci. **22**, 69 (1997).
[17]D. J. Dunstan, H. G. Colson, and A. C. Kimber, J. Appl. Phys. **86**, 782 (1999).
[18]B. V. Kamenev, H. Grebel, and L. Tsybeskov, Appl. Phys. Lett. **88**, 143117 (2006).
[19]A. N. Goldstein, Appl. Phys. A **62**, 33 (1996).
[20]S. Veprek, Thin Solid Films **297**, 145 (1997).
[21]A. N. Goldstein, C. M. Echer, and A. P. Alivisatos, Science **256**, 1425 (1992).
[22]K.-C. Fang and C.-I. Weng, Nanotechnology **16**, 250 (2005).

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