

A Switcher ASIC Design for Use in a Charge-Pump Detector

Zhi Yong Li, Gianluigi De Geronimo, D. Peter Siddons, Durgamadhab Misra, Trevor A. Tyson, and Emerson Vernon

Abstract—The objective of this paper is to describe a Switcher ASIC with 64 high voltage output channels. Each channel provides two high voltage control pulses with maximum amplitudes of 32 V. The high voltage level shifter was designed with a current mirror switching circuit that has a readily adjustable switching speed, unlike conventional switching circuits. The logic control circuit uses a forward and reverse chain of Flip-Flops along with other combinational logic gates to generate bidirection sequential control pulses with adjustable pulsewidth and polarity. The layout was carefully designed to achieve a 14 μm width for the last stage transistors' drain path based on the 50 μm output channel pitch set up. At least a 200 mA current driving capability was obtained for each channel. The design was fabricated using TSMC's 180 nm CMOS HV technology. The paper further discusses the critical design steps including chip architecture, layout, simulation and bench test. The final experimental results demonstrate that the Switcher ASIC meets requirements and the rising time could reach 480 ns with a 1 nF capacitive load at 15 V pulse amplitude. With this load, the total power consumption of the chip was measured to be approximately 4 mW when the input clock period was 42.2 μs . In addition to use in a charge-pump detector, the ASIC can be used to control the charge accumulation and readout in other detectors, such as X-ray pump probe detectors (XPP).

Index Terms—Charge-pump detector, level shifter, switcher, X-ray correlation spectroscopy.

I. MOTIVATION

ACTIVE pixel detectors play a growing role in high energy and astrophysics experiments [1]. Conventional CCD systems have been successfully used but with some disadvantages. The depleted field effect transistor (DEPFET) pixel sensor [1] was developed later for astrophysics applications

Manuscript received January 06, 2012; revised April 24, 2012; accepted August 15, 2012. Date of publication October 23, 2012; date of current version December 11, 2012. This work was supported in part by the U.S. Department of Energy, Office of Science, Office of Basic Energy Sciences, under Contract No. DE-AC02-98CH1088, by the Linac Coherent Light Source (LCLS) at SLAC National Accelerator Laboratory, by National Science Foundation, Major Research Instrumentation Grant DMR 0722730 (NJIT) and by the New Jersey Institute of Technology.

Z. Y. Li and D. Misra are with the Department of Electrical and Computer Engineering, New Jersey Institute of Technology, Newark, NJ 07102 USA (e-mail: zyl2@njit.edu; dmisra@adm.njit.edu).

G. De Geronimo, D. P. Siddons, and E. Vernon are with Brookhaven National Laboratory, NY 11973 USA (e-mail: degeronimo@bnl.gov; Siddons@bnl.gov; vernon@bnl.gov).

T. A. Tyson is with the Physics Department, New Jersey Institute of Technology, NJ 07102 USA (e-mail: Tyson@adm.njit.edu).

Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/TNS.2012.2215883

to achieve longer X-ray exposure time, lower noise level [2] and higher spatial resolution [2]. The X-ray correlation spectroscopy (XCS) sensor [3], [4] (for which the current circuit was designed) was developed specifically for the XCS experiment to be performed at the Linac Coherent Light Source at SLAC. The strategy of using bias electrodes to move charges from pixels to readout amplifiers is similar for all of these devices.

The charge-pump detector, designed at Brookhaven National Laboratory for use in X-ray correlation spectroscopy [3], is based on the XCS sensor which has 1024 rows \times 1024 columns of 56 micrometer pixels [3]. The LCLS source produces a 50 fs X-ray laser pulse at a 120 Hz rate. The charges created by the detection of the scattered X-rays are collected in the XCS sensor, and must be read out before the next X-ray pulse is delivered, i.e., in less than 8 ms. The outputs of all 1024 columns are connected to 1024 preamplifiers at the bottom of the array. The charges from each row are transferred to the 1024 preamplifiers sequentially in a repetition period of less than 7.8 μs [3], similar to the row wise operation of the DEPFET detector [5], [6]. Each pixel requires two bias pulses to transfer the charges, thereby only two bias pulses are required for row controls. The bias pulsewidth needs to be less than 7.8 μs to be able to transfer 1024 rows within 8 ms. The Switcher ASIC here discussed was designed to meet these requirements.

The structure of a single XCS sensor pixel is displayed in Fig. 1. The sensor is built based on an N type semiconductor substrate (blue). On the bottom is a P+-doped area where a high negative bias (~ 100 volts) is applied. On the top, the center circle area D is doped N+ and is the node for extracting the stored charge. It is surrounded by 3 P+-doped electrodes which are marked C, B and A in the figure. The dimension of the sensor is 56 μm \times 56 μm . The electrodes A, B, C, D are biased with -15 V, -3 V, -15 V, 0 V, respectively, and the bottom is biased with a negative high voltage of around 100 V. The bottom side of the sensor is fully depleted initially. When X-rays are absorbed in the depleted silicon they create electron-hole pairs. The electrons will drift towards the B node because of the potential valley created by the electrode biases, and will not be able to move past the D node because of the potential barrier created by the C electrode bias. After the charges are accumulated for a certain time period, the B node bias will be changed to -11 V from -3 V and the C node bias to -1.5 V from -15 V, the electron charges on the B node will start to move towards the D node for readout (as in [3]). This type of sensor is able to store the charge produced by up to 180 X-ray photons of 8 KeV in each pixel while its equivalent noise charge (ENC) is maintained to be less than 100 electrons [3].

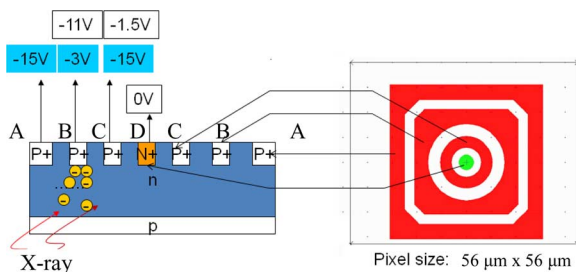


Fig. 1. Single element of CCD-like XCS array sensor, left side is cross section, right side is top view. On the left panel, the voltages marked with cyan and white are the bias voltages of the nodes. The nodes marked with white are P+; with orange is the N+.

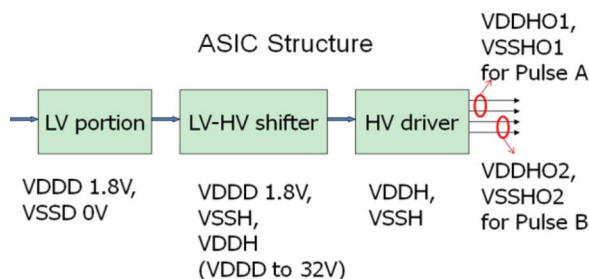


Fig. 2. Switcher ASIC architecture.

Implementation of this detector requires the Switcher ASIC to provide multiple control channels for row operation. Each control channel should be able to provide two bias pulses changing from -1.5 V to -15 V and from -11 V to -3 V to control one row. The pin pitch of these pads needs to be matched with XCS pixel size for wire bonding purpose. These pulses need to be able to propagate from one channel to another at the falling edge of the row clock for the sequential row-wise operation. The speed of the row clock needs to be faster than $7.8 \mu\text{s}$ period with the line load of 1 nF capacitor. Also, the pulsewidth and polarity need to be adjustable for control flexibility. Such a device is not found on the commercial market and hence we produced the design described in this paper.

II. ARCHITECTURE

To provide the row controls for 1024×1024 pixel sensors, we developed a control system which has 16 Switcher ASICs. Each ASIC possesses 64 high voltage output channels. Each channel provides two control pulses, A and B, with maximum amplitude of 32 V. The polarity of pulses A and B can be separately reversed. The Switcher architecture is shown in Fig. 2. It consists of 3 sections of LV (Low Voltage) portion, LV-HV (High Voltage) shifter and HV driver. TSMC018 HV technology is used for this design, for which the LV transistors require 1.8 V and HV transistor can support up to 32 V.

The LV portion provides the digital control for pulse propagation both in forward and reverse directions. It also provides pulsewidth and polarity control. The circuit contains the forward and reverse chain of Flip-Flops and combinational logic circuits. Detailed function description can be found in the simulation section.

The low voltage circuit (LV portion) uses a power supply, VDDD (voltage drain to drain (VDD) digital) (1.8 V, positive)

with VSSD (voltage for substrate and sources (VSS) digital). LV-HV shifter circuit uses a power supply, VDDH (VDD High voltage) (32 V maximum, positive) with VSSH (VSS high voltage). The LV-HV shifter converts the pulse amplitude from 1.8 V to high voltage in the range from 1.8 V to 32 V. Details are displayed on Fig. 4.

The HV driver unit is designed with a large current drive capability which can drive a 1 nF capacitor with 200 mA peak current at high voltage. It has four stages and the optimized stage effort [7] is used to switch quickly with the minimum number of stages. The HV driver for Pulse A uses the power supply which is connected to the “VDDHO1” (VDDH Output 1) (positive) pad and “VSSHO1” (VSSH Output 1) (negative) pad. Pulse B circuit power is connected to “VDDHO2” (VDDH Output 2) (positive) pad and “VSSHO2” (VSSH Output 2) (negative) pad. Each channel has two sets of circuits and each set contains the LV portion, LV-HV shifter and HV driver. These two sets of circuits share parts of the LV portion circuit and provide separately the outputs of HV pulse A and HV pulse B. Both HV Pulse A and B are triggered at the falling edge of clock. The VDDH needs to be connected with most positive voltage of VDDHO2, VDDHO1, and VDDD. VSSH needs to be connected with most negative voltage of VSSHO2, VSSHO1, and VSSD.

(Two versions of the ASIC were developed finally. The revision 1 was developed for $56 \mu\text{m}$ XCS sensor. It has the transistors test circuits to monitor the fabrication process. These test circuits were removed in revision 2, which is developed for $90 \mu\text{m}$ sensors. Both versions share the same ASIC structure described above. Other difference between revision 1 and 2 are the pad sizes and pin pitches and Pulse polarity control for A port (PA). The pad sizes and pin pitches of two revisions are provided in detail in Section IV. The PA function difference has been discussed in the second paragraph of Section V.)

III. LV-HV SHIFTER CIRCUIT DESIGN

The conventional voltage level converter circuit in Fig. 3 [8] cannot satisfy our needs because of its complex bias circuit and the difficulty of adjusting the response speed.

A new level shifter circuit, displayed in Fig. 4, is utilized for the Switcher ASIC, in which, the current mirror principle [9] is applied to copy current from a low voltage switching circuit (M1, M2, M3, M4) to high voltage (M7, M8, M9, M10) switching. In this way the output voltage level can shift from 1.8 V to 32 V. Also, an adjustment circuit (M5, M6) is added to adjust the transient response speed and prevent both M8 and M10 from turning on at the same time.

In Fig. 4, V^- and V^+ are the 1.8 V pulse signals to be level shifted, which come from the LV portion of the Switcher. In the case V^- is switched from high to low (1.8 V to 0 V) and V^+ from low to high (0 V to 1.8 V), V^- turns on the HV transistor of M1. V^+ signal turns off the HV transistor of M2.

Before V^- and V^+ are switched, M6 is in the linear state since its gate is biased with the same gate voltage as M4, which is in the saturation state when V^+ is low. Therefore, when V^- and V^+ are switched, while M3 is at the cut off state and M8 is still on, M6 is turned on immediately to prevent turning on M7, M9, M10. M4 continues to be on to discharge the node capacitor until the voltage of its drain/gate drops below threshold.

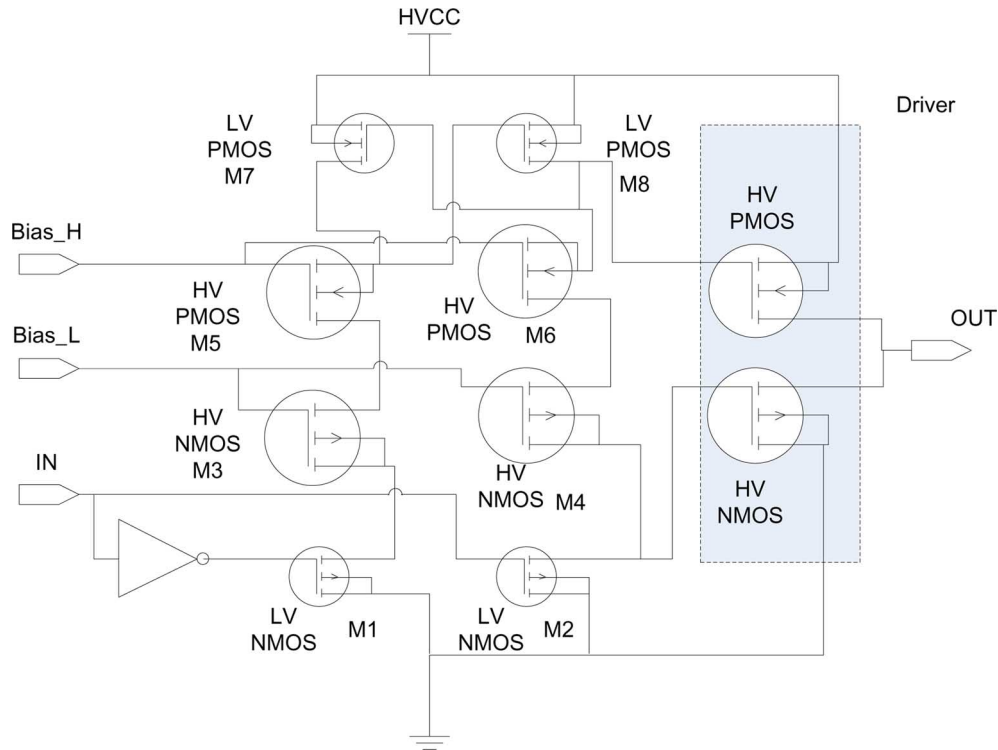


Fig. 3. Conventional voltage level shifter circuit demonstrated in [8].

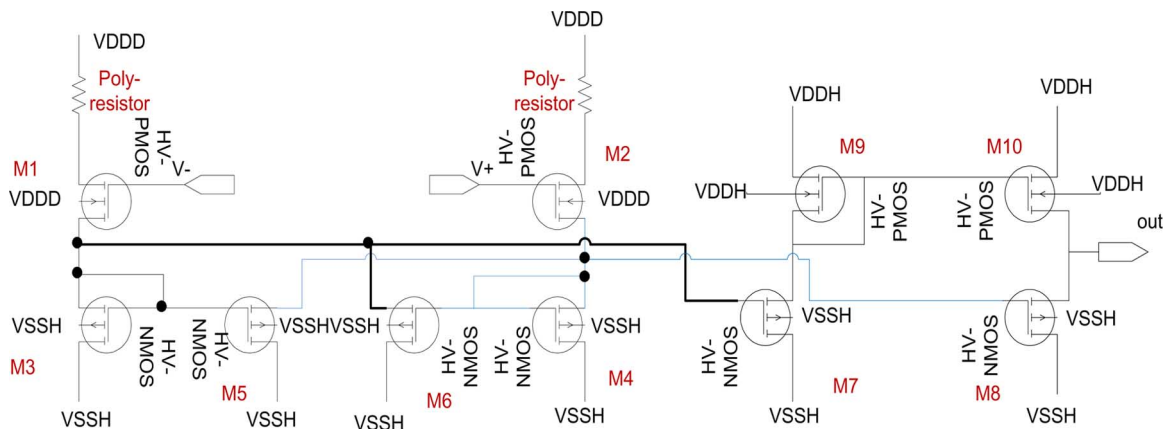


Fig. 4. New voltage shifter using current mirror circuit.

This will decrease the gate voltage of M6 as well and the drain voltage of M6 will be increased to maintain the current until it is big enough to turn on the M3, M5 and M7. If M5 is on, it facilitates the discharge process of the drain node of M4 and the voltage of the node falls below the transistor threshold voltage more quickly and thus M8 will be turned off faster. Similarly, when V^- is switched from low to high, M5 and M6 will also play a similar role in speeding up the turn-off of M7 and the turn-on of M8. Therefore, the adjustment circuit improves the performance of the circuit during the transition period and switching speed can be readily adjusted by changing the size of these two transistors.

M1 and M6 are turned on first when V^- is changed to high voltage and later when M3 starts to be turned on and saturated, M6 will be cut off. The current, limited by a poly resistor be-

tween M1 and VDD can thus be expressed as the drain current of M3. When it is copied to M7 and it could be amplified by a factor of $(W_2)/(W_1)$. Where W_2 is the width of M7 and W_1 is the width of M3, assuming the lengths of M3 and M7 are equal.

When M7 is on, it turns on HV PMOS M10 by another current mirror circuit. Since M8 is turned off by M4 and M5, the output of "out" will be "VDDH." Similarly if V^+ is switched from 1.8 V (VDDD) to 0 and V^- from 0 to 1.8 V (VDDD), M10 will be off and M8 will be on, the output will be "VSSH." Thus, the LV (VDDD, VSSD) to HV (VDDH, VSSH) transition is achieved by copying the current from the LV to HV switching circuit.

IV. LAYOUT DESIGN

The challenge for the layout design is to decide which semiconductor technology can be used for HV and how to put all the

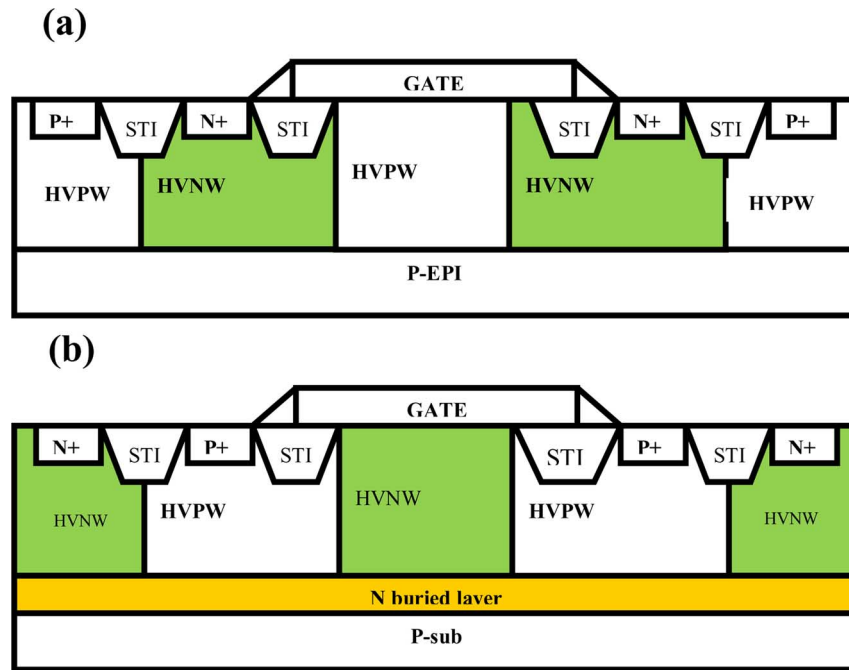


Fig. 5. (a) HV symmetric NMOS cross section. (b) HV symmetric PMOS cross section.

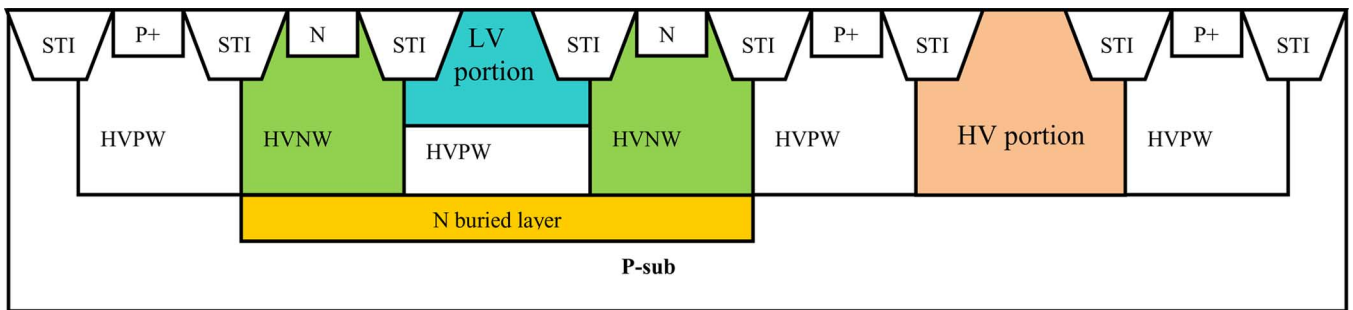


Fig. 6. LV and HV arrangement for the Switcher ASIC.

transistors of two channels (2 A and 2 B outputs) within a distance of $100 \mu\text{m}$, while providing the maximum output current drive capability on the output pads.

The breakdown voltage of a PN junction is presented in [8] as follows:

$$BV \cong \frac{\epsilon_{si}(N_A + N_D)}{2qN_A N_D} E_{\text{Max}}^2$$

where ϵ_{si} is the dielectric permittivity of silicon, N_A is the doping concentration of the acceptors of P-type material, N_D is the doping concentration of the donors in the N-type material, q is the charge of an electron and E_{Max} is the critical electric field for silicon. Since the TSMC018 HV transistors use the lightly doped N-well or P-well to form the P or N channel of HV symmetric P/NMOS, as indicated in Fig. 5, it will give a high breakdown voltage and can be used for the HV (32 V) purpose of the Switcher ASIC. (In this figure STI denoted Shallow Trench Isolation, P-EPI denoted P type EPitaxy).

To prevent latch up, the HV and LV devices are totally isolated by the N-well (NW) and P-well (PW). The LV devices were placed on the left side of the ASIC after the input pads,

The HV devices were placed on the right side before the HV output pads. The cross section of such an arrangement is displayed in Fig. 6.

To reach the maximum current drive capability for the output ports with $50 \mu\text{m}$ channel pitch given (Fig. 7), it requires the path width from the Drain of PMOS and NMOS to the output pads to be as wide as possible. Such a layout arrangement for two channels is displayed in Fig. 7. We achieved about $14 \mu\text{m}$ widths for the last stage transistor drain path which is the best case of the layout and obtained at least 200 mA peak current driving capability for each channel.

The view of entire layout of the Switcher ASIC (revision 2) and its corresponding function blocks are displayed in Fig. 8. The layout different between revision 1 and 2 is the test pins and pin pitch of the input and output pads. On revision 1, N/PMOS test transistors are added to monitor the fabrication process; therefore additional 13 input pins are added for the purpose. The input pins are displayed on the left side of Fig. 8. For revision 1, pin pitches are $\sim 100 \mu\text{m}$ and $\sim 140 \mu\text{m}$ and pad size is $60 \mu\text{m}$ (L) \times $60 \mu\text{m}$ (W). For revision 2, the test pins were removed, the pad size is $200 \times 100 \mu\text{m}$ and input pin pitch is $168 \mu\text{m}$.

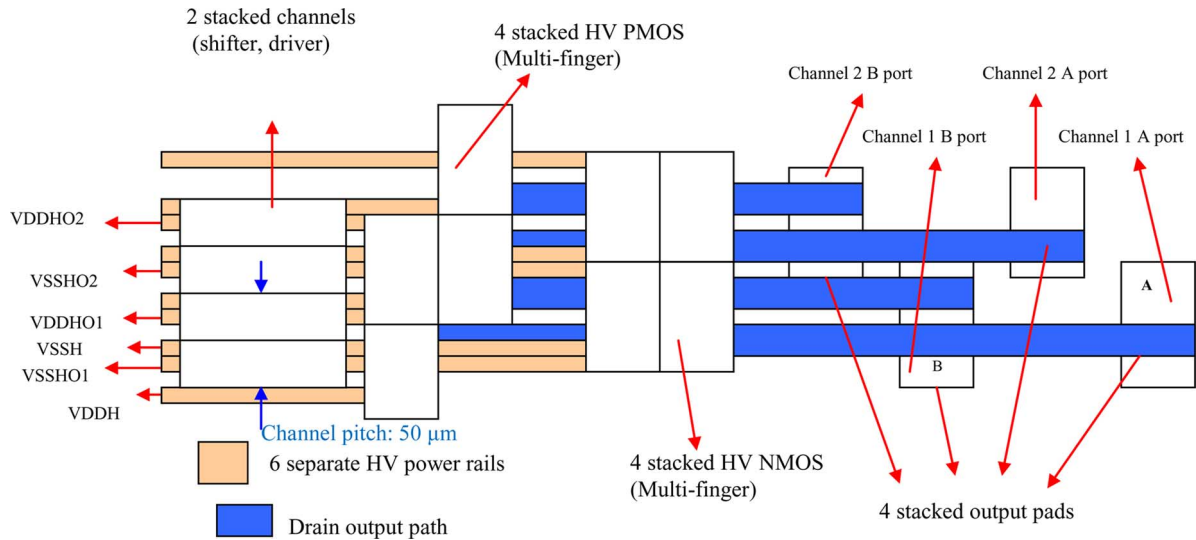


Fig. 7. Layout plan for two channels cell (HV portion) of the Switcher ASIC.

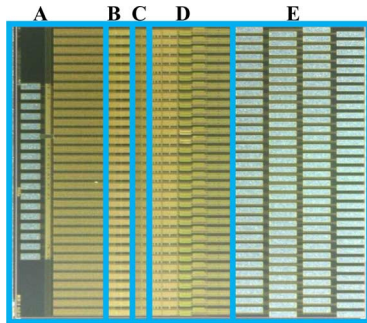


Fig. 8. 64 channels switcher ASIC die (revision 2). Size of layout is $3203 \mu\text{m} \times 3307 \mu\text{m}$. Block A: Pad in circuit which contains the input pads, Schmitt trigger circuits and test transistors. Block B: Low voltage circuit, includes logic control circuits to propagate the pulse and the pulse polarity and width control, etc. Block C: LV-HV level shifter circuit. Block D: HV driver which contains four stages buffer. Block E: Output pads.

The output pins are displayed on the right side on Fig. 8. For revision 1, output pin pitch is $134 \mu\text{m}$ for pins at the same column and $33 \mu\text{m}$ for pins at adjacent columns and pad size is $154 \mu\text{m}$ (L) \times $60 \mu\text{m}$ (W). For revision 2, pin pitch is $168 \mu\text{m}$ (same column) and $85 \mu\text{m}$ (adjacent column) and pad size is $300 \mu\text{m} \times 90 \mu\text{m}$.

V. SIMULATION

A simulation of the entire circuit (64 channels with 128 HV outputs) was performed to verify the design. In this paper we discuss only a four channel cell simulation.

The simulation is done with the 1 nF capacitor load for each pulse output of each channel based on the Switcher ASIC revision 1. The functional difference between revision 1 and 2 is the control function of PA. For revision 1, output pulses of A port and B port are positive when PA is logic high and Pulse polarity for pulse B (PB) is logic low. Both of them are negative when PA is logic low and PB is high. For revision 2, output pulses of A and B port are both positive when PA and PB are logic low and are both negative when PA and PB are high.

The connection to test these four channels is made according to Fig. 9. As displayed in Fig. 9, in the forward pulse propagation direction, the LV pulse output of channel (Ch)1 which is labeled with TDOA (Token Data Output of pulse A) is routed to the input of Ch2 which is labeled with TDIA (Token Data Input of pulse A). The LV pulse output of Ch2 is connected to Ch3, and so on. The LV pulse is propagated from Ch1 to Ch4. Then the LV output pulse of Ch4 (TDOA) is routed back by connecting to the reverse direction input of itself which is labeled TDIAr (TDIA reversed). Its reverse direction pulse output is connected to Ch3, and so on; the pulse is propagated back to Ch1 again. In this way, the outputs are sequenced continuously up and down the four channels.

The simulation result is shown in Fig. 10. In Fig. 10, 18 signals of simulation are displayed. The input stimulus pulse TDIA of channel 1 is displayed in signal 4. The HV outputs of channel 1 (A1, B1) are displayed in signals 11 and 12. It is activated at the falling edge of clock signal (CLK) which is displayed in signal 8. The width of the HV output pulse is adjusted by the AI (pulse A width adjust control Input) or the BI (pulse B width adjust control Input) displayed in signals 9 and 6. This can be verified by checking signals 1 and 2 displayed in Fig. 10(a). Signal 1 is the LV signal which is passed to the LV-HV shifter to produce HV pulse B. Its width is adjusted by BI signal. Signal 2 is the LV signal for pulse A. Similarly, its width is adjusted by the AI signal. The polarity of the HV pulse is adjusted by PA or PB which is displayed in signals 10 and 5. The control pulse is propagated from Ch1 to Ch2 (A2, B2), Ch3 (A3, B3) and Ch4 (A4, B4) at the falling edge of the clock signal CLK sequentially when the reset signal ($-\text{RST}$) displayed in signal 7 is high. The A* and B* are the HV (32 V) outputs of pulse A and B at channel * which are displayed from signals 13 to 18. The polarity of A* is negative because PA is logic low in the forward propagation process. On the contrary, it changes to the positive when PA is logic high in the reversal direction. The polarity of pulse B* is positive when PB is logic low at the forward direction and changes to negative when PB is logic high at the reverse direction. PA and PB control function can also be clearly

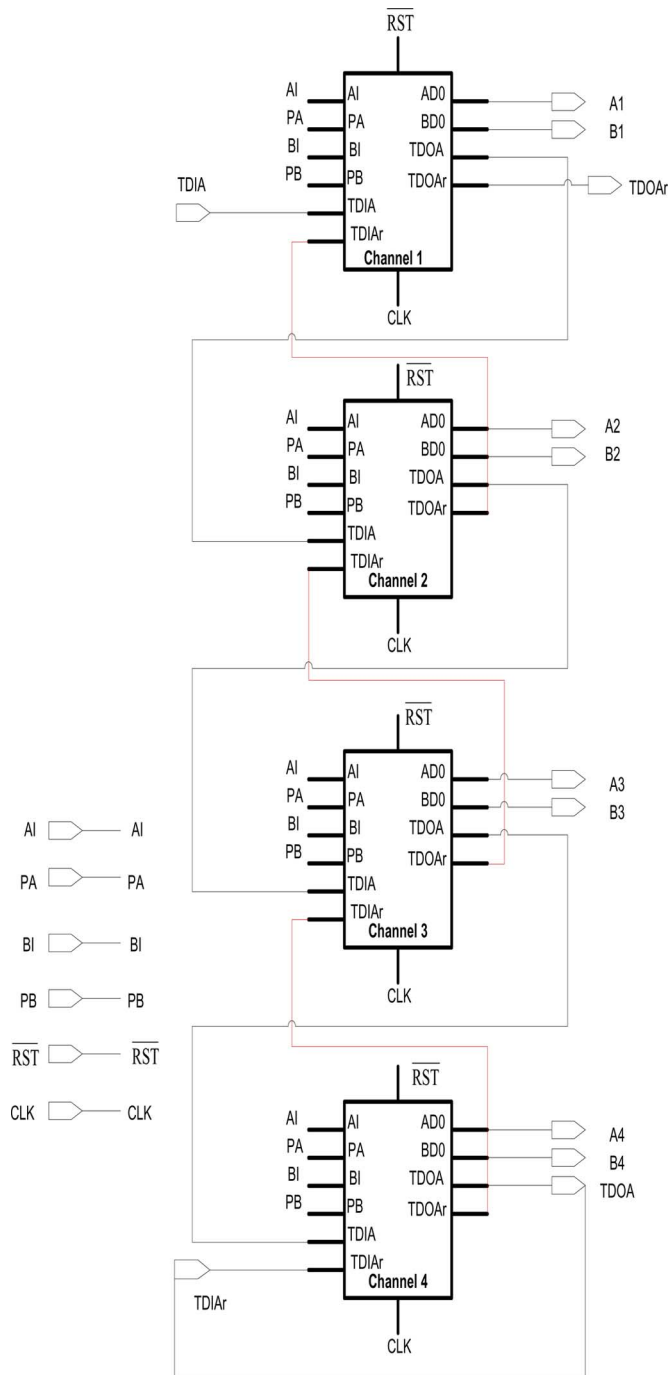


Fig. 9. Circuit connection for four-channel simulation.

verified by comparing signal 1 to signal 18 and signal 2 to signal 17 where signals 1 and 2 are the low voltage pulses adjusted by pulsewidth signals but not yet adjusted by the polarity control signals. The polarity will be changed according to PA and PB and is reflected in the HV outputs of channel 4 which is signals 17 and 18.

The LV pulse output (TDOA) of the last channel (channel 4) is deliberately designed to be triggered at the rising edge of CLK (same to the TDOAr of the first channel (Ch1)); therefore it is delayed half clock period of the input pulse (TDIA of Ch4). This is verified by the TDIAr waveform displayed on signal 3 which is obviously triggered at the rising edge of CLK. Since the

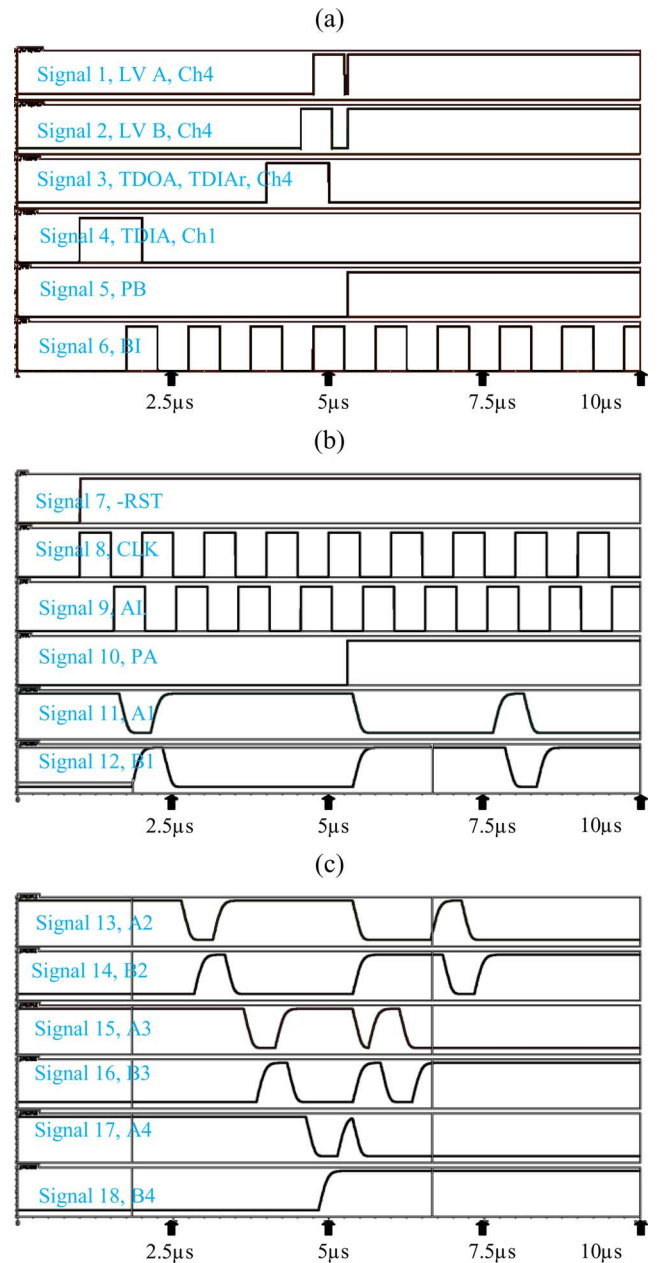


Fig. 10. Four-channel simulation signals in $10\ \mu\text{s}$ time scale total. The load for each channel is $1\ \text{nF}$ capacitor. (a) Signals from 1 to 6 are $1.8\ \text{V}$, where Signal 1 is LV pulse output of B for channel 4. Signal 2 is LV pulse output of A for channel 4. Signal 3 is LV forward direction pulse output of channel 4 (TDOA, TDIAr). Signal 4 is forward direction pulse input for channel 1 (TDIA). Signal 5 is PB, pulse polarity control for B port. Signal 6 is BI, pulsewidth control for B port. (b) Signals from 7 to 10 are $1.8\ \text{V}$; signals from 11 to 12 are $32\ \text{V}$. Signal 7 is the reset signal ($-\text{RST}$) which is active low. Signal 8 is the clock signal (CLK). Signal 9 is the AI signal, pulsewidth control for A port. Signal 10 is PA, pulse polarity control for A Port. Signal 11 is A1, HV output of port A of channel 1. Signal 12 is B1, HV output of port B of channel 1. (c) Signals from 13 to 18 are $32\ \text{V}$. Signal 13 is A2, HV output of port A of channel 2. Signal 14 is B2, HV output of port B of channel 2. Signal 15 is A3, HV output of port A of channel 3. Signal 16 is B3, HV output of port B of channel 3. Signal 17 is A4, HV output of port A of channel 4. Signal 18 is B4, HV output of port B of channel.

TDOA is connected to TDIAr in Ch4 in which the TDIAr pulse will be adjusted and finally passed to LV-HV shifter circuit at the coming falling edge of clock, the HV output of TDIAr pulse is therefore overlapped with the HV output of TDIA pulse of

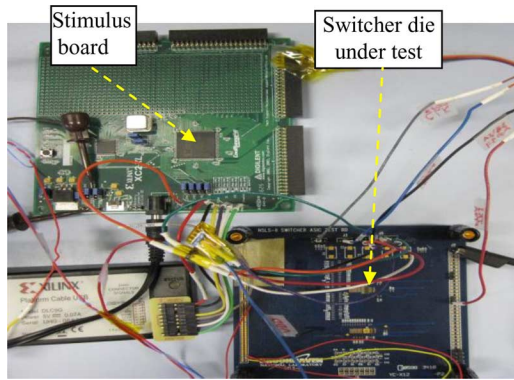


Fig. 11. Bench test set up. Switcher die is bonded to the pads of print wire board with wires.

channel 4. This is why only one pulse is seen on A4 and B4. It shows that the pulse of end channel will be with the same phase as the pulse of the start channel of the next chip if we connect the LV output directly from one chip to the input of another chip. This is a problem and an external additional flip-flop is required to give one clock delay on the propagation path between chips.

To summarize, from Fig. 10, the function of the 4-channel Switcher is verified to perform as expected. Since it is only the end two channels which require external I/O connections, the 64 channel Switcher is actually realized by placing the channel 1 of 4-channel Switcher first, 62 copies of channel 2 in the second and a copy of the channel 4 at the last. The TDOAr of first channel (Ch1) is 1/2 clock shift from the pulse output of second channel (Ch2) and triggered at rising edge of CLK. The TDOA of last channel (Ch64) is 1/2 clock shift from pulse output of 63th channel (Ch63) and triggered at rising edge of CLK. The TDOAr pulse propagated from Ch64 to Ch2 and TDOA pulse from Ch1 to Ch63 are triggered at the falling edge of CLK. The rest functions of these 64 channels are the same, just like four channels switcher simulated above, the HV outputs of A and B of one channel are synchronized at the falling edge of CLK and one clock shift from the previous channel. The pulsewidth and polarity are adjusted by AI, BI, PA, PB signals.

VI. BENCH TEST OF SWITCHER DIE

Fig. 11 shows the bench test set up for Switcher ASIC revision 2. The stimulus board on the left side provides the clock, reset, input LV pulse and AI/BI pulse, given in detail in Figs. 12, 13. These stimulus signals were connected to “CLK” “-RST” “TDIA” “AI” and “BI” of the die on the test board. The PA, PB are connected to logic low. All the HV power supplies (VDDH, VDDHO1, VDDHO2) are connected to 15 V, while VSSH, VSSHO1, VSSHO2, VSSD, die substrate are connected to ground. As expected, Fig. 12 shows that the TDOA pulse of the last channel (Ch64) appears at the rising edge of the 64th clock of “CLK” signal after TDIA pulse.

The HV output was also checked on the selected ports (A15, A16, B17 and B18 port); A15 output is displayed here in Figs. 13 and 14 as an example. AI, BI are connected to logic high first, it gives the result of Fig. 13. Then they are connected to the pulse displayed in Ch2 of Fig. 14. A15 gives the output in Ch4 of Fig. 14 and shows that the output pulse is positive

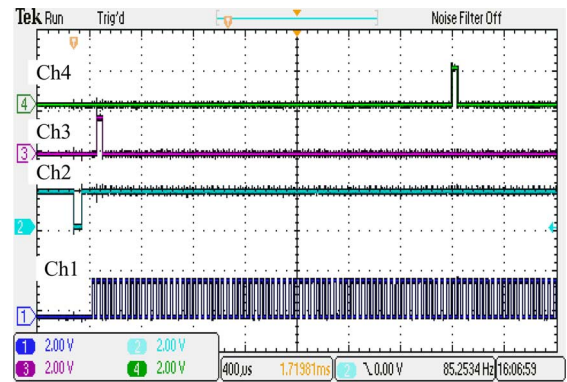


Fig. 12. Test results of TDOA. Ch3 is the TDIA to the first ASIC channel. Ch2 is the reset (-RST) signal. Ch4 is the TDOA of the last ASIC channel (Ch64); Ch1 is the clock signal (CLK). All four channels of scope are in 2 V, 400 μ s scale.

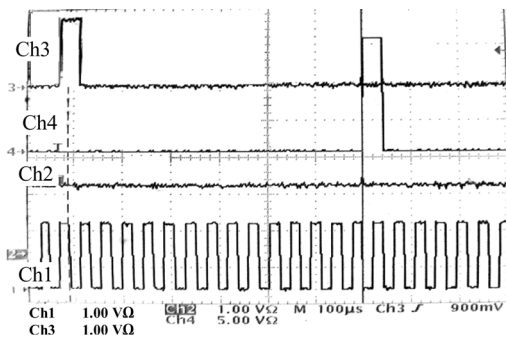


Fig. 13. Test results on the scope. Ch3 is the TDIA to the first ASIC channel. Ch4 is the HV pulse output of A15 when AI is logic high. Ch2 is the reset signal (-RST); Ch1 is the clock signal (CLK).

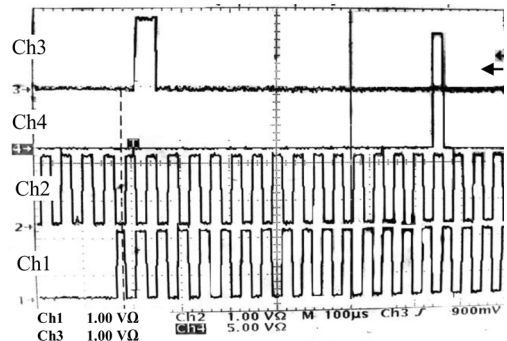


Fig. 14. Test results on the scope. Ch3 is the TDIA to the first ASIC channel. Ch4 is the HV pulse outputs of A15 when AI is the pulse displayed in Ch2; Ch1 is the clock signal (CLK). Comparing with Fig. 13, the pulsewidth of A15 here is adjusted by the AI signal.

when PA and PB is connected to logic low and the pulsewidth can be adjusted to the same width of the AI pulse. All functions of these ports work as simulated.

The output pulse rising time vs. capacitor load was also checked, the results are listed in Table I as follows.

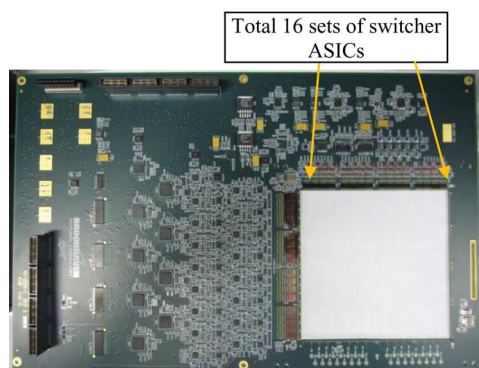
The total power consumption of the die was about 4 mW when input clock period was 42.2 μ s, where 16 out of 128 ports were connected to capacitor loads (one for 10 pF, one for 100 pF, one for 470 pF and the rest are for 1 nF).

More tests of Switcher ASIC are done on X-ray Pump Probe detectors system (XPP) [10] which is designed to support

TABLE I
RESPONSE SPEED TEST VS. LOAD CAPACITANCE

Port under test	Load capacitance	Pulse magnitude change	Rise time
A15	10 pF	0->15 V	12 ns
A16	100 pF	0->15 V	43.6 ns
B17	470 pF	0->15 V	216 ns
B18	1 nF	0->15 V	480 ns

(a)



(b)

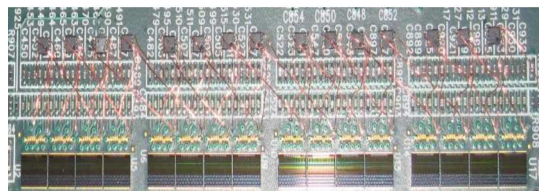


Fig. 15. On XPP detector circuit board, 16 pieces of Switcher ASIC are used to control charge transferring from 1024×1024 detectors. (a) The XPP detector analog board which includes the 1024×1024 detectors (not bonded on the figure), 16 sets of readout ASICs, 16 sets of ADC and 16 sets of Switcher ASICs. (b) Expanded view of area where 16 Switcher ASICs is placed.

the X-ray Pump Probe experiment in LCLS [11]. The XPP detectors system [12] analog board consists of 1024×1024 X-ray Active Matrix Pixel Sensors (XAMPS), 16 sets each of the following, 1) 64 channels readout ASICs, 2) ADCs, and 3) Switcher ASICs, which are displayed in Fig. 15. Fig. 15(b) shows the expanded view of the area where the 16 sets of Switcher ASICs are placed. Unlike XCS detectors, the XPP detectors require every row or column readout in less than 5 μ s, the single sensor size of XAMPS is 90 μ m and each pixel requires one voltage control to turn off or on the Junction Field Effect Transistor (JFET) [11] for charge transferring. The “turn off” voltage provided by the switcher ASIC is less than -3 V. The “turn on” voltage is larger than $+2$ V. The row readout and JFET gate control functions of Switcher ASIC are verified on XPP detectors and meet our expectations.

VII. CONCLUSION

Following the simulation and bench test results, we conclude that the 64 channels (128 HV outputs) switcher ASIC operates as expected. There was a problem described in Section V with the token propagation from chip to chip. It is simply rectified by adding an external additional Flip-Flop to provide a one clock delay, which we have done in our applications of the chip.

The ASIC provides high sequential voltage control at given clock rate for 64 channels, each channel can provide two pulse with maximum voltage and driving current of 32 V and 200 mA, the pulsewidth and polarity is adjustable. In addition to be used with the charge pump XCS detector, the latest version of ASIC (revision 2) can be utilized in other applications, such as XPP detector since this application only requires one bias pulse to control the switches for charge transferring of the row pixels. Both revisions were verified by tests and meet the requirements.

ACKNOWLEDGMENT

The authors wish to thank A. Kuczewski for design of the test PCB, and D. Pinelli for wire bonding the ASICs to the test boards.

REFERENCES

- [1] R. H. Richter *et al.*, “Design and technology of DEPFET pixel sensors for linear collider applications,” *Nuclear Instrum. Meth. Phys. Res. A*, vol. 511, pp. 250–256, 2003.
- [2] M. Trimpl *et al.*, “A DEPFET pixel matrix system for the ILC vertex detector,” *Nucl. Instrum. Meth. Phys. Res. A*, vol. 560, pp. 21–25, 2006.
- [3] G. A. Carini *et al.*, “Charge-pump detector for X ray correlation spectroscopy,” *Nucl. Instrum. Meth. Phys. Res. A*, vol. 649, pp. 75–77, 2011.
- [4] [Online]. Available: https://slacportal.slac.stanford.edu/sites/lcls_public/instruments/xcs/Pages/default.aspx Apr. 10, 2012
- [5] H. Kruger, “Front-end electronics for DEPFET pixel detectors at SuperBelle (BELLE II),” *Nucl. Instrum. Meth. Phys. Res. A*, vol. 617, pp. 337–341, 2010.
- [6] P. Fischer *et al.*, “Steering and readout chips for DEPFET sensor matrices,” presented at the Topical Workshop on Electronics for Particle Physics, Prague, Czech Republic, Sep. 03–07, 2007 [Online]. Available: <http://cdsweb.cern.ch/record/1091457>, presented at., Apr. 10, 2012, pp. 282–286
- [7] N. H. E. Weste and D. Harris, *CMOS VLSI Design*, 3rd ed. Reading, MA: Addison Wesley, May 21, 2004, ch. 4, pp. 178–181.
- [8] D. Pan *et al.*, “A low voltage to high voltage level shifter circuit for MEMS application,” in *Proc. Univ./Government/Industry Microelectron. Symp.*, pp. 128–131.
- [9] B. Razavi, *Design of Analog CMOS Integrated Circuits*. New York: McGraw-Hill, 2001, ch. 5, pp. 135–139.
- [10] [Online]. Available: <http://lcls.slac.stanford.edu/xpp> Apr. 10, 2012
- [11] G. A. Carini, W. Chen, Z. Li, P. Rehak, and D. P. Siddons, “X-ray active matrix pixel sensors based on J-FET technology for the linac coherent light source,” in *Proc. IEEE Nucl. Sci. Symp. Conf. Rec.*, 2007, vol. 2, p. 1603.
- [12] G. A. Carini *et al.*, “Tests of small X-ray active matrix pixel sensor prototypes at the national synchrotron light source,” in *Proc. PIXEL Int. Workshop FERMILAB*, Batavia, IL, Sep. 23–26, 2008, doi:10.1088/1748-0221/4/03/P03014.