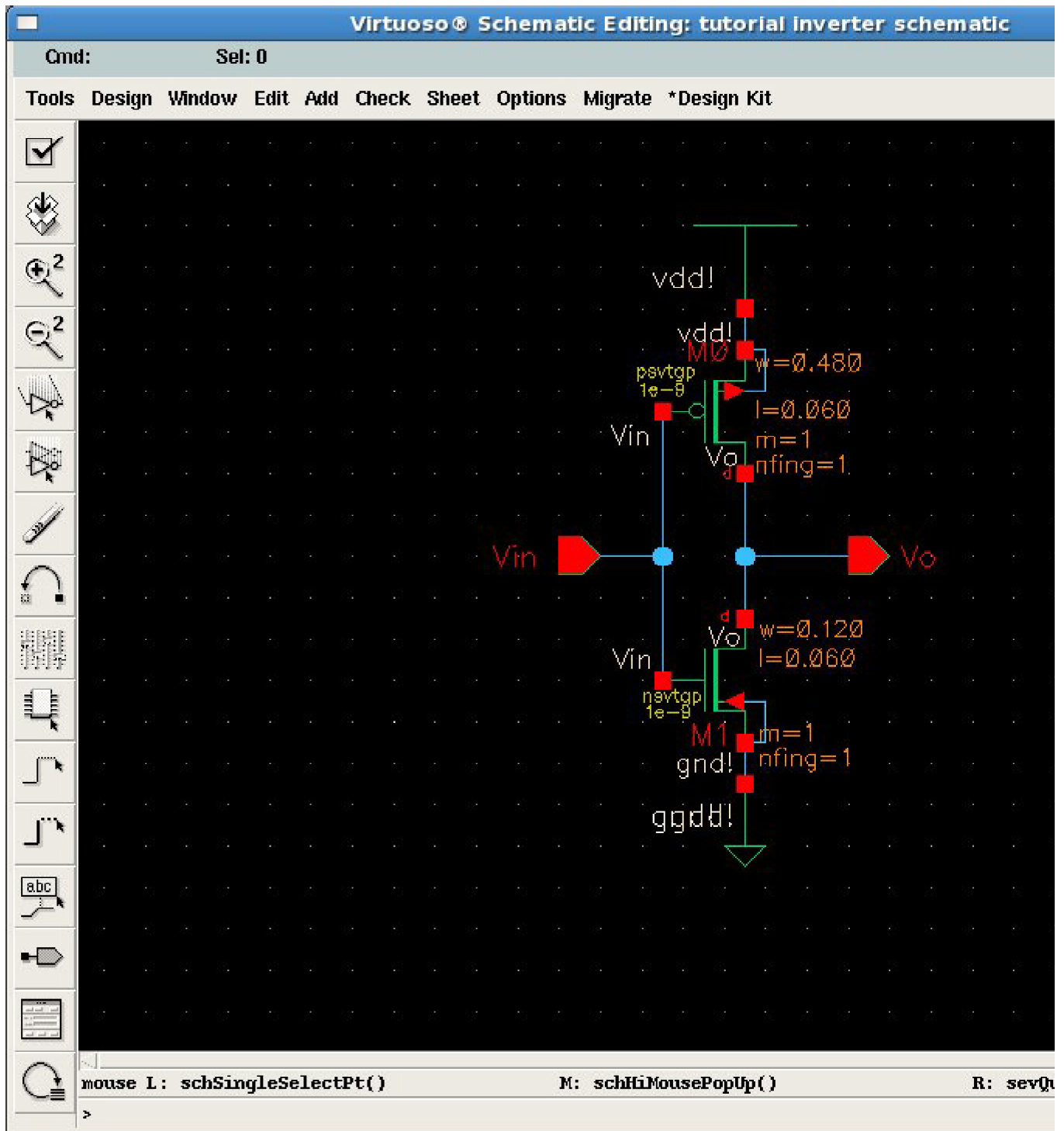# CADENCE LAYOUT TUTORIAL
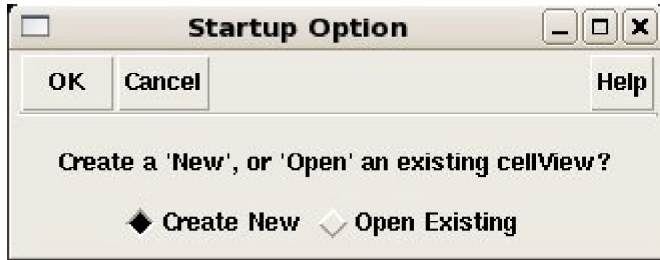
Creating Layout of an inverter from a Schematic:

Open the existing Schematic

From the schematic editor window
Tools─>Design Synthesis─>Layout XL

A window for startup Options comes up

Startup Option

OK | Cancel | Help

Create a 'New', or 'Open' an existing cellView?

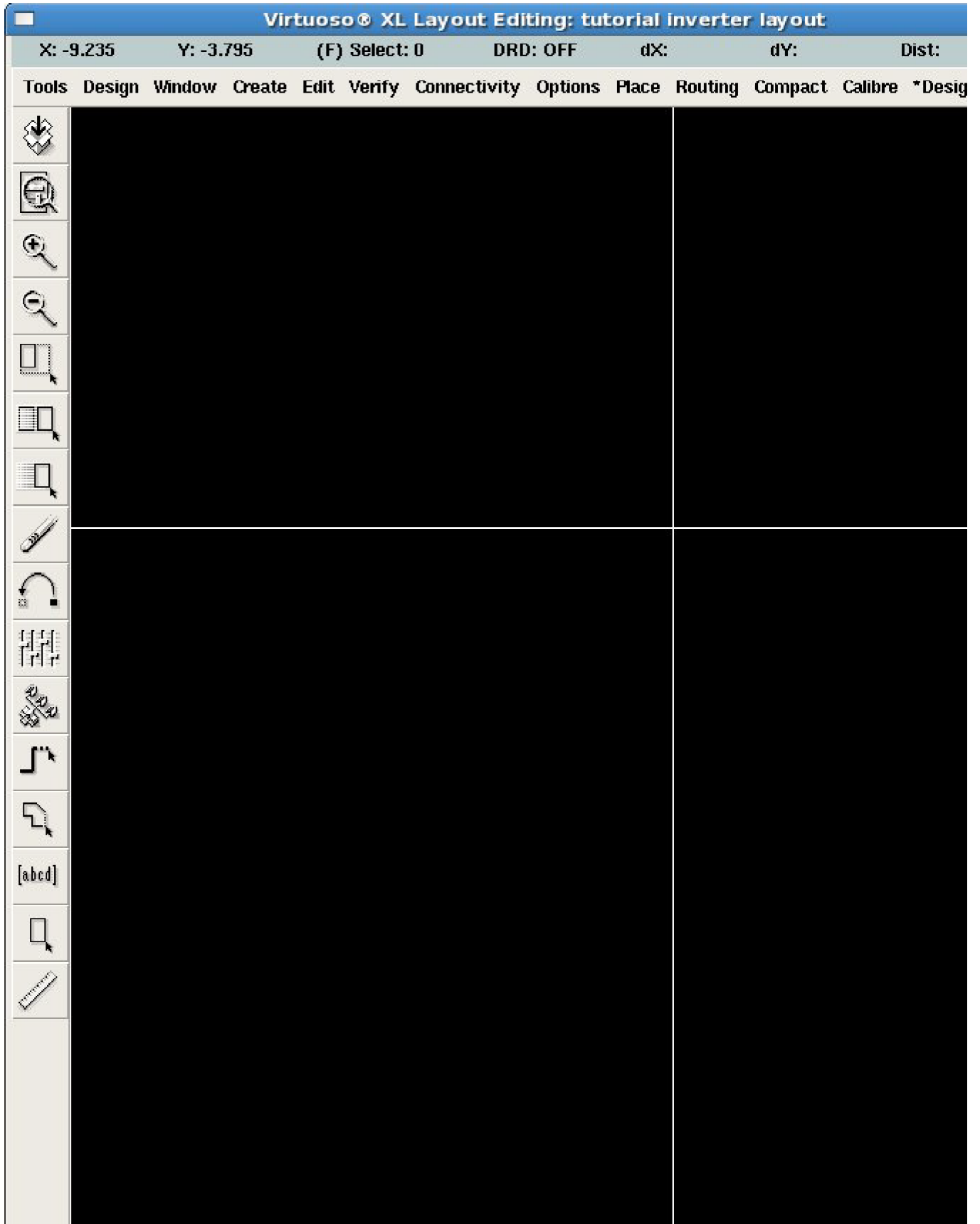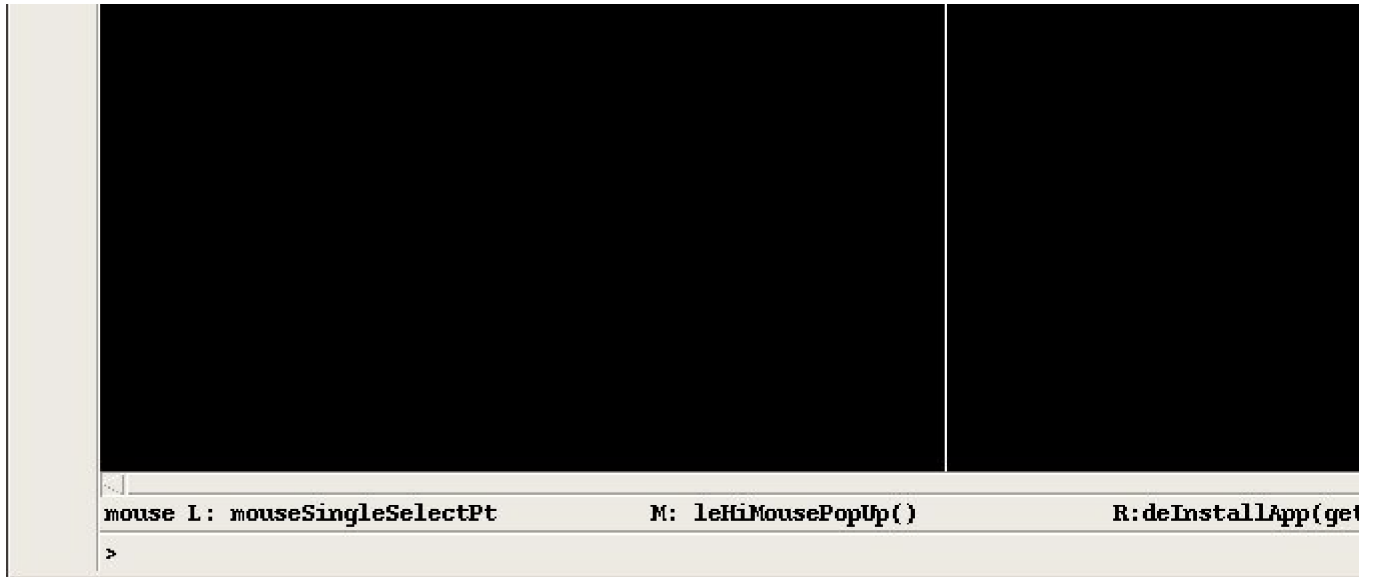◆ Create New ◇ Open Existing

Select the button corresponding to the Create New text as shown

A Create New File window comes up. The Cell Name corresponds to the schematic name, leave it that way.
The field corresponding to the View Name label should read Layout.
Click OK and see the layout window come up.

Virtuoso® XL Layout Editing: tutorial inverter layout

X: -9.235   Y: -3.795   (F) Select: 0   DRD: OFF   dX: dY: Dist:

Tools   Design   Window   Create   Edit   Verify   Connectivity   Options   Place   Routing   Compact   Calibre   *Desig

From the layout window menu select:
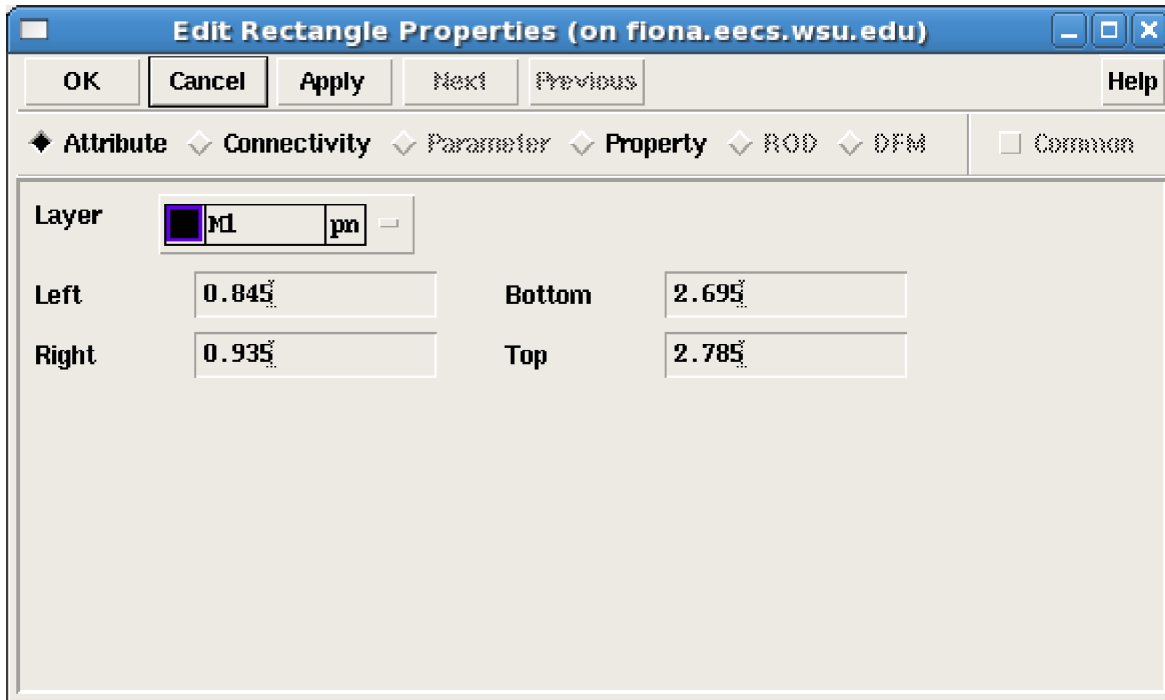Create—>pick from Schematic and the window below comes up
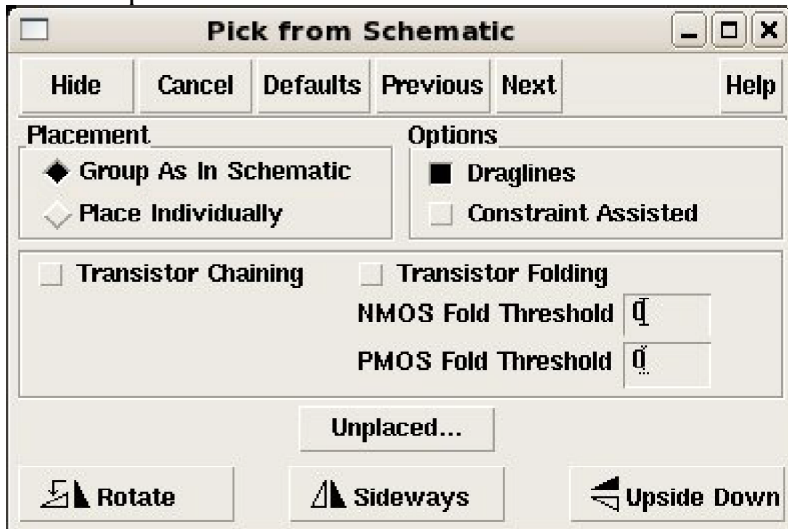
Highlight/Select the entire circuit from the schematic window and move the mouse onto the layout window. The layout components of your circuit show on the layout window. Place them with a click of the mouse. If the layers do not show; simultaneously press the SHIFT key and the letter F and the layers will show. Now connect the Poly layers using the drawing tool. This is achieved by selecting from the LSW window the P0 drawing layer and drawing a rectangle that joins the nMOS and pMOS gates (red layer on each transistor}.

Connect the drains using the M1 drawing layer selected from the LSW window. Draw the ground and vdd nets. They will be of 0.36microns wide. See the picture below for dimensions. Use the *hot key* "i" to insert the NTAP_J instance on the vdd net, making sure the contact is directly on the net. Insert the PTAP_J instance on the gnd net.

VERY IMPORTANT

Labels must use the pin layers instead of the text. See diagram below. To view the properties and connectivity of the pin: select the pin and click the middle mouse button to select properties. The same should be done with the text box.

Make sure the pin and the text are of the corresponding layer e.g if the pin is a P0 pin make sure it is placed on P0 layer and the text must be of P0 material.

The layout is now complete and needs to be checked for design rule violations. On the layout window click on the Calibre menu item:
Caliber—>Run DRC

Customization Settings (calibrelswitchdef in /net/ictools/pdk/CMOS06! ✕

For Help on ST SWITCHES type unix command : calibreSTSwitchesHelp -lvs

SWITCHES FOR LVS OPTIONS

☐ Skip ERC1 to ERC12 rules check (Wells biasing) (sign-off)

☑ Check ERC13 and ERC14 rules check (Connections through OD/PO)

☑ Check ERC15 rules check (Floating OD-PO intersection)

☐ Sense extraction and comparison

☐ Analog mode (no parallel/series reduction performed)

☐ Do not compare ESU and EDU of non salicided MOS transistors

☑ Compare area and perimeter of isolated PW to DNW diode

Hier depth for reading port objects from the layout db   PRIMARY ▭

Hier depth for selecting text objects from the layout db   PRIMARY ▭

Tolerance for mos width comparison (%)   1

Tolerance for mos length comparison (%)   0

Tolerance for resistor width comparison (%)   0

Tolerance for resistor length comparison (%)   0

OK	Cancel	Reset	Save...

We will use the default selection. Click OK on the window above.

Calibre Interactive - nmDRC : calibreIrunsetdrc [/net/ictools/pdk/CMOS065 ▭ ☐ ✕

<u>F</u>ile <u>T</u>ranscript <u>S</u>etup   <u>H</u>elp

- <u>R</u>ules
- <u>I</u>nputs
- <u>O</u>utputs
- Run <u>C</u>ontrol
- T<u>r</u>anscript
- C<u>u</u>stomization
- Run <u>D</u>RC
- Start R<u>V</u>E

```
Layer RNr_H1::<1> DELETED -- LVHEAP = 4/6/8

WRITE to ASCII DRC Results Database inverter1.drc.results COMPLETED

DRC RuleCheck RNr_H1 COMPLETED. Number of Results = 0 (0)

Cumulative ONE-LAYER BOOLEAN Time: CPU = 0   REAL = 0
Cumulative TWO-LAYER BOOLEAN Time: CPU = 0   REAL = 0
Cumulative POLYGON TOPOLOGICAL Time: CPU = 0   REAL = 0
Cumulative POLYGON MEASUREMENT Time: CPU = 0   REAL = 0
Cumulative SIZE Time: CPU = 0   REAL = 0
Cumulative EDGE TOPOLOGICAL Time: CPU = 0   REAL = 0
Cumulative STAMP Time: CPU = 0   REAL = 0
Cumulative ONE-LAYER DRC Time: CPU = 0   REAL = 0
Cumulative TWO-LAYER DRC Time: CPU = 0   REAL = 0
Cumulative NET AREA (RATIO) Time: CPU = 0   REAL = 0
Cumulative DENSITY Time: CPU = 0   REAL = 0
Cumulative MISCELLANEOUS Time: CPU = 0   REAL = 0
Cumulative CONNECT Time: CPU = 0   REAL = 0
Cumulative RDB Time: CPU = 0   REAL = 0

--- CALIBRE::DRC-H EXECUTIVE MODULE COMPLETED.  CPU TIME = 0   REAL TIME
--- TOTAL RULECHECKS EXECUTED = 1089
--- TOTAL RESULTS GENERATED = 2 (2)
--- DRC RESULTS DATABASE FILE = inverter1.drc.results (ASCII)

--- CALIBRE::DRC-H COMPLETED - Fri Sep  7 20:50:44 2007
--- TOTAL CPU TIME = 1   REAL TIME = 1
--- PROCESSOR COUNT = 1
--- SUMMARY REPORT FILE = inverter1.drc.summary
```

Click on Run DRC and two more windows will show up. The one that shows first does not contain information of interest. The second one is key.

The window below shows results of a layout that has an error. Watch the comments at the bottom of the window, they give the specifics on what the error is.
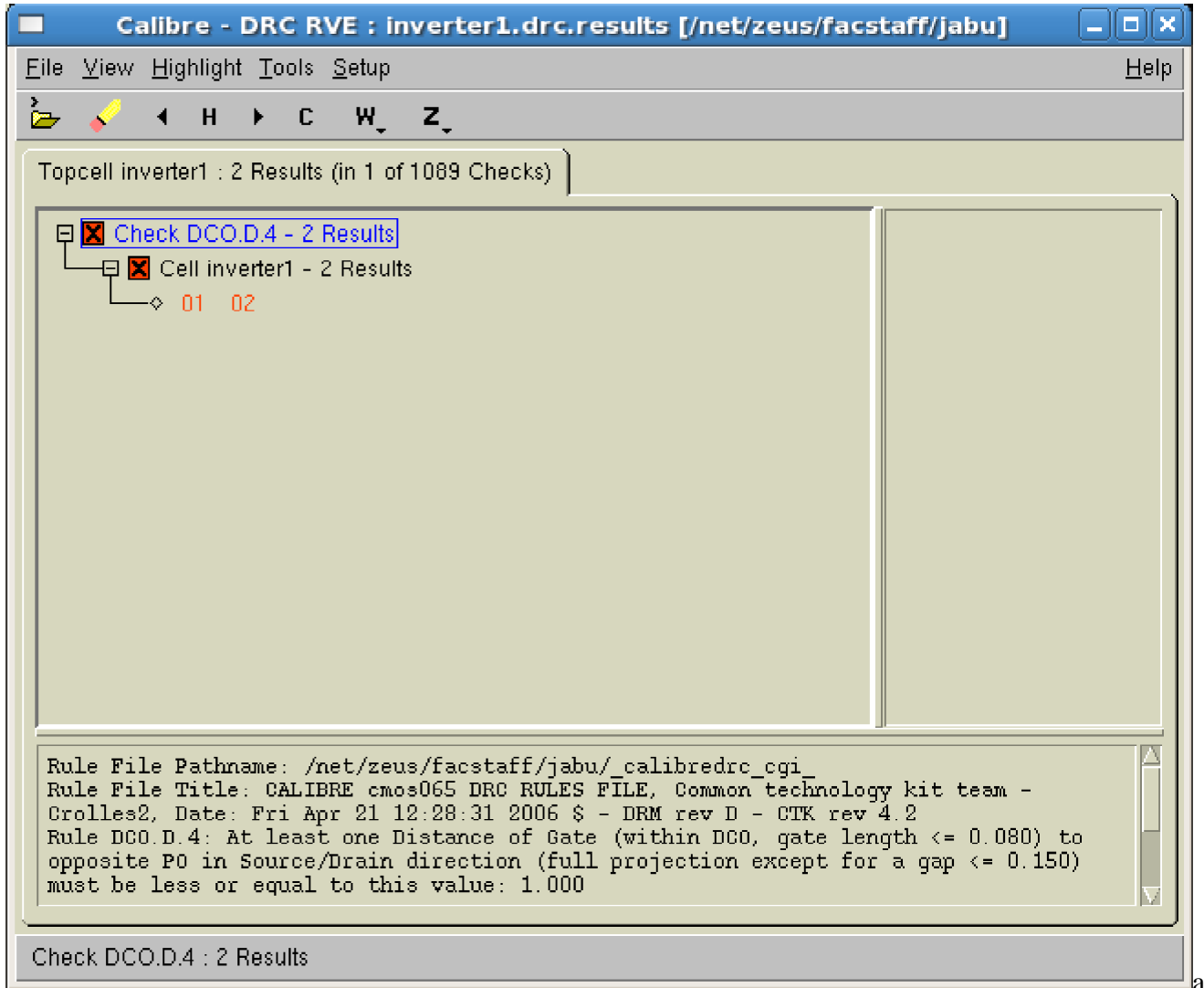
Create Library form appears, fill it as

Right Click on top of the lettering highlighted in blue on the window above and watch the layout window closely. The area that has the error gets highlighted. Sometimes the color used to highlight is the same as the color of the material making it difficult to see where the error is. If you click on the numbers 01 or 02, you will see on the right hand column of this window the coordinates and you can thus click on these coordinates and watch the response on the layout window.
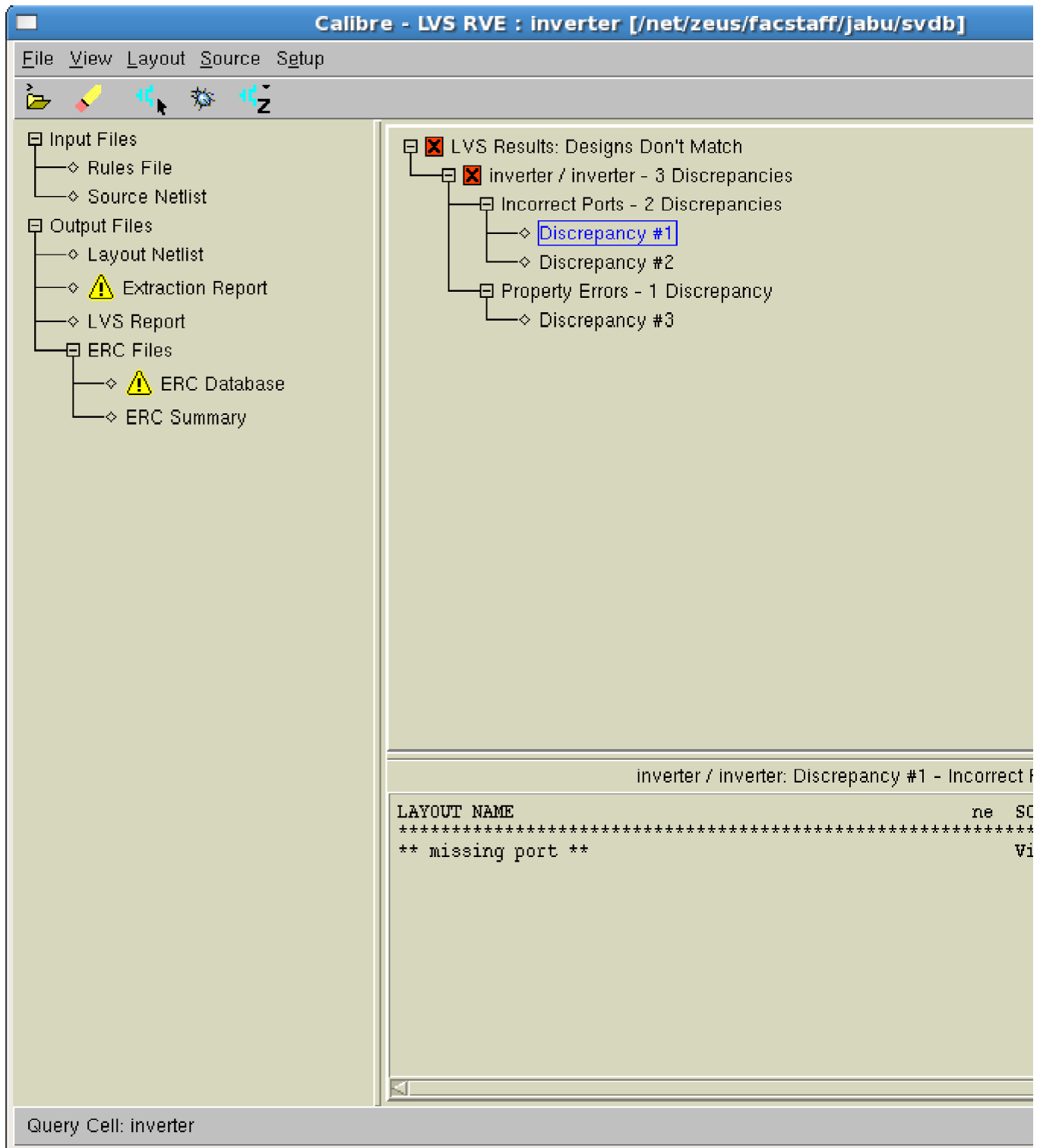
Correct the error and run DRC again to see if an more violations exist. The DRC Window below shows results of an error free layout, one in which no design rules have been violated.
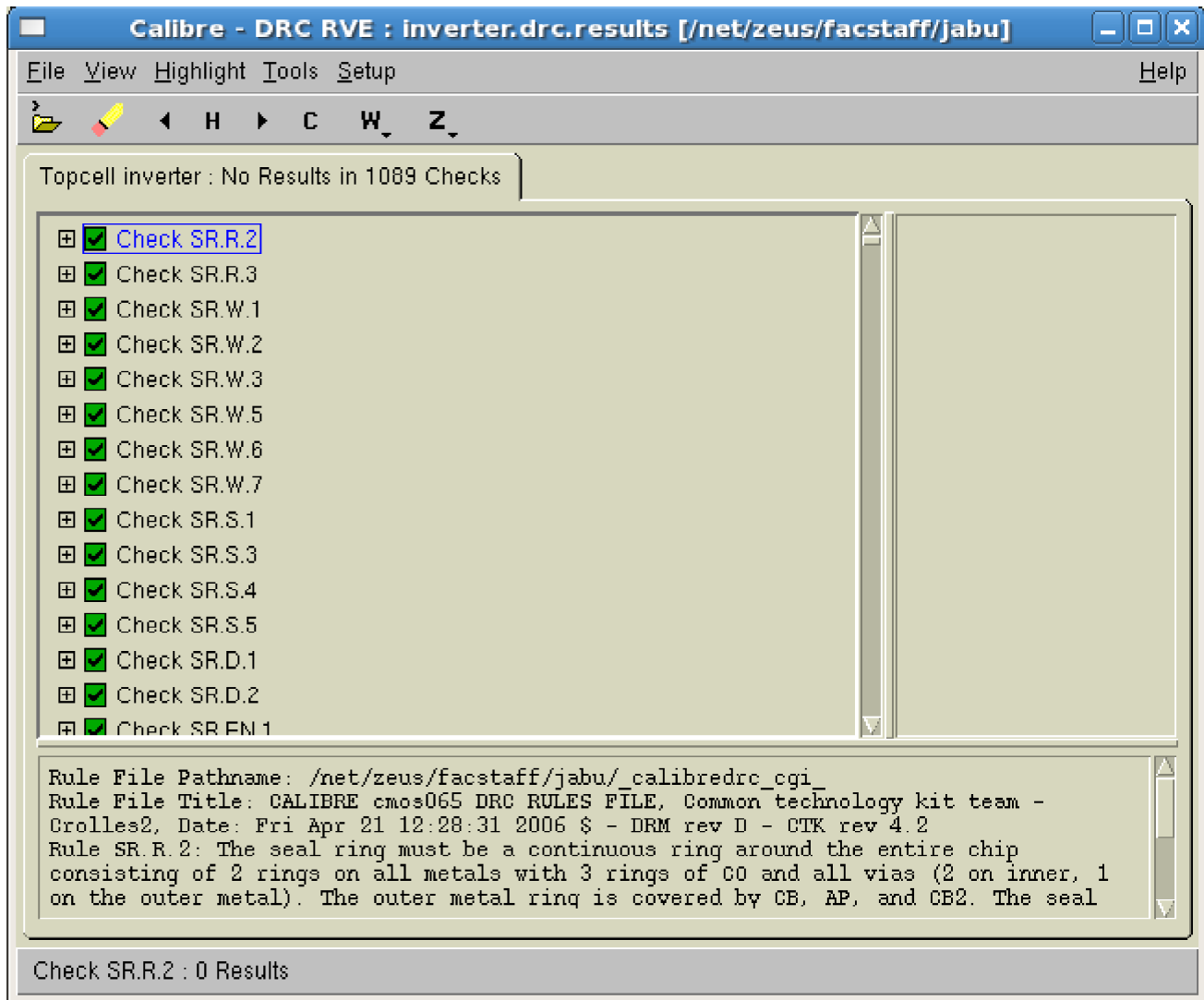
Once we have succeeded with DRC we need to compare the layout vs the schematic using LVS. Click on the Caliber menu item:
on the Caliber menu item:
Caliber→Run LVS

The window below shows a failed LVS. Clicking on the lettering highlighted in blue shows what the problem is.

Calibre - LVS RVE : inverter [/net/zeus/facstaff/jabu/svdb]

File View Layout Source Setup

- Input Files
  - Rules File
  - Source Netlist
- Output Files
  - Layout Netlist
  - ⚠ Extraction Report
  - LVS Report
  - ERC Files
    - ⚠ ERC Database
    - ERC Summary

- ☒ LVS Results: Designs Don't Match
  - ☒ inverter / inverter - 3 Discrepancies
    - Incorrect Ports - 2 Discrepancies
      - Discrepancy #1
      - Discrepancy #2
    - Property Errors - 1 Discrepancy
      - Discrepancy #3

inverter / inverter: Discrepancy #1 - Incorrect F

```
LAYOUT NAME                                      ne  SO
***************************************************
** missing port **                                Vi
```

Query Cell: inverter

Fix the errors and re-run LVS, Note the green faces indicating success.
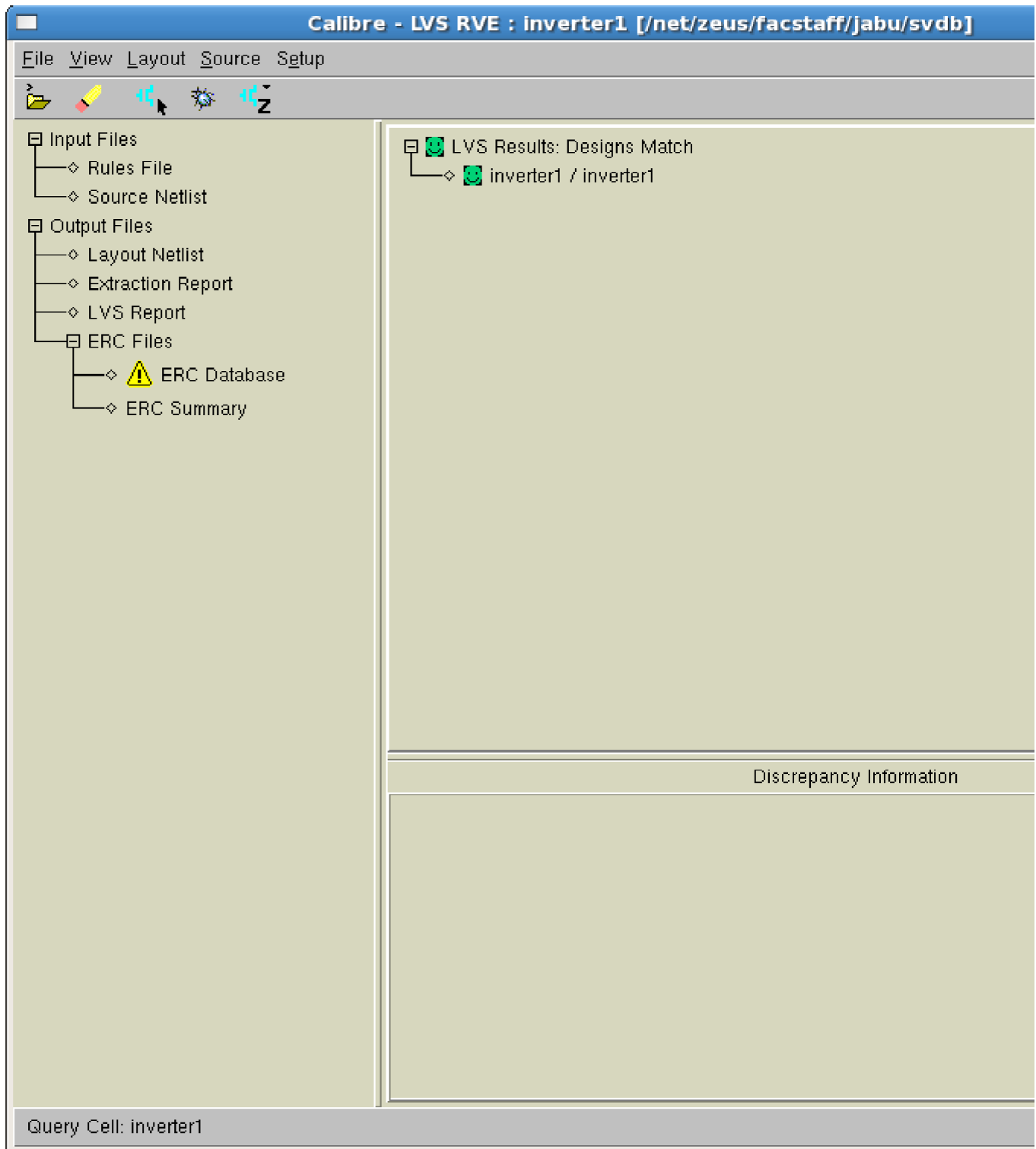
Now that DRC and LVS have passed close these windows and on the Layout window click on the Tools menu item:
Tools→Post-Layout Simulation→Schematic With Skipped Cells.

The Window below comes up.

The window below comes up.

Post-Layout Simulation (Schematic with Skipped Cells) (on fiona ☐ ☐ ✕

Status: Ready Results: pls1   15

Session Tools Commands Outputs Run Log Results   Help

Top Schematic –

Library	tutorial
Cell Browse	inverter1
View	schematic

Top Layout

Library	tutorial
Cell	inverter1
View	layout

| Run PLS | PLS 1.4.1 (C) STMicroelectronics (2007) | Nets Browser |

| LVS & Skipped Cells | Extraction | Reduction | Back-Annotation |

Open Schematic

List of Nets   ◆ all
  ◇ all but powers and grounds
  ◇ only powers and grounds
  ◇ only selected set   Select
  ◇ all but selected set   Select

Ground Net Name for Lumped Parasitic Capacitances   gnd!

Extraction Methodology   RCc –

Cc threshold - unit: F	1e-15
Cc percentage - unit: %	1
Cg threshold for filtering - unit: F	0
Rel accuracy goal - unit: %	1
Cap accuracy goal - unit: fF	1
Run time limit - unit: hours	24

Extraction Strategy   RCMAX –

Change Default Temperature ? ■

Temperature (deg. C)   25

Metal Fill Polygon Handling   floating

Select the Extraction Button and then Click on Run PLS

Watch the icfb window. If the extraction is completed successfully you will see the text in the figure below otherwise a message that reads: "pls:PLS Failed" will be displayed and you will have to determine the problem and fix it. If your design had not passed LVS you will get a Warning Message that states that the Schematic and the Layout are not compatible. You can proceed with the subsequent steps even though LVS failed.

icfb - Log: /net/zeus/facstaff/jabu/CDS.log (on fiona.eecs.wsu.edu)

File Tools Options *Tag *Switch analogLib *Design Kit

```
pls:moving /net/zeus/facstaff/jabu/CMOS065/DSPF.SPF into ./plsimulation/tutorial-inverter1-schem
        ...successful.
pls:read global net file ./plsimulation/tutorial-inverter1-schematic/tutorial-inverter1-layout/p
pls:create Schematic and Layout Extracted views on cell inverter1 of library tutorial ...
        ...successful.
pls:PLS FLOW COMPLETED SUCCESSFULLY
```

mouse L: M: R:

>

Now you have extracted schematic and layout views of your layout with all the parasitics. The library manager quits automatically at this point (should not happen but ....). Close the schematic and layout editing windows.

Open the library manager and select your library.
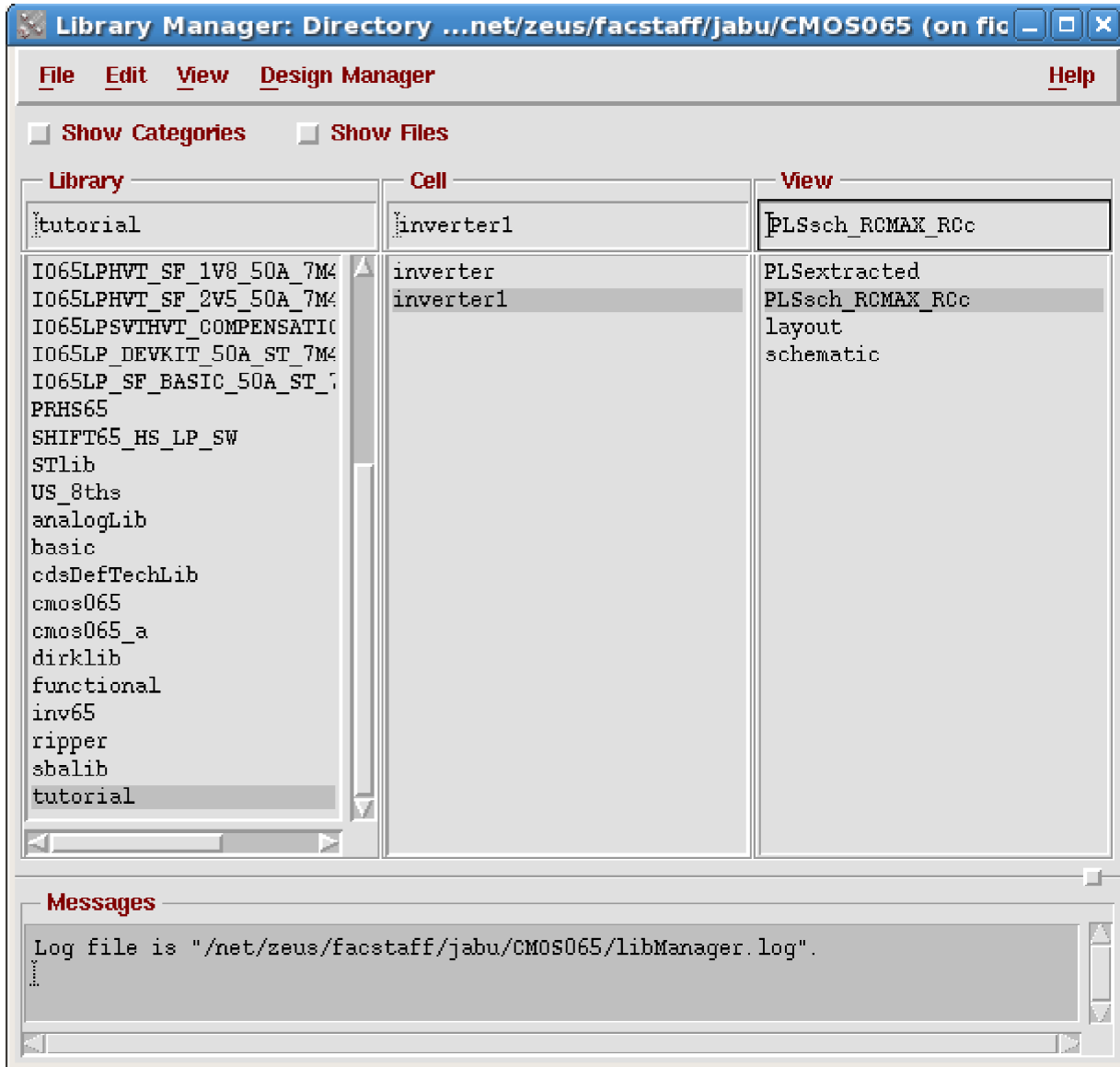
Notice the additional files that have been created (PLSextracted and PLSsch_RCMAX_RCc), open the PLSsch_RCMAX_RCc fil). It contains the schematic of your transistors as extracted from the layout with all the paracitics (capacitances and resistances). From this schematic window select the Tools menu item as shown in the figure below:

Tools→Analog Environment