

# Charge Trapping in Ultrathin Hafnium Silicate/Metal Gate Stacks

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**Abstract**—Charge trapping characteristics of MOCVD  $\text{HfSi}_x\text{O}_y$  (20%  $\text{SiO}_2$ ) gate stack of n-MOSFETs during substrate injection have been investigated. Positive constant voltage stress (CVS) and constant current stress (CCS) were applied at the gate of  $\text{TiN-HfSi}_x\text{O}_y\text{-SiO}_2/\text{p-Si}$  n-MOSFETs having EOT of 2 nm. Significant electron trapping is observed from the positive shift of threshold voltage ( $\Delta V_t$ ) after stress. Curve fitting of the threshold voltage shift data confirms power law dependence for Hf-silicate gate stacks. Charge pumping measurements for both cases showed significant electron trapping at bulk Hf-silicate while interface trap generation was comparatively insignificant. A turn-around effect is noticed for  $\Delta V_t$  as the stress current and voltage increases under CCS and CVS. Dependence of spatial distribution of charge trapping at shallow traps on stress level in the Hf-silicate film and redistribution of trapped charges during and after removal of stress is possibly responsible for the turn-around effect.

**Index Terms**—Charge pumping, charge trapping, hafnium silicate, high- $\kappa$ , metal gate, substrate injection.

## I. INTRODUCTION

**H**AFNIUM-BASED dielectrics are under intense investigation to replace the conventional  $\text{SiO}_2$  [1], in order to meet the ITRS requirements for leakage current and oxide thickness. Charge trapping is an area of concern for these devices.  $\text{HfO}_2$ , a potential candidate for replacement, suffers from significant charge trapping as reported by Zhu [2] and Zafar [3] *et al.*, when used with poly-Si gate. Hafnium silicate, another potential candidate, though has lower dielectric constants, has better leakage characteristics, improved  $\Delta V_t$ , lower mobility degradation, and allow larger thermal budgets during processing than  $\text{HfO}_2$  [4]. We have investigated the charge trapping characteristics of MOCVD  $\text{HfSi}_x\text{O}_y$  (20%  $\text{SiO}_2$ ) gate stack with TiN gate by applying CVS and CCS on n-MOSFETs, in substrate injection mode.

## II. EXPERIMENTAL

Transistors were fabricated by standard CMOS process flow where MOCVD was used to deposit the gate dielectric. The stack was formed with a thin interfacial layer of 1.0-nm  $\text{SiO}_2$  followed by 3.5-nm-thick 20%  $\text{SiO}_2$ -hafnium silicate layer with physical thickness of  $t_{\text{ox}} = 4.5$  nm (EOT =  $2 + / - 0.03$  nm). These devices were subjected to  $\text{NH}_3$  PDA at 700 °C for 60 s,

to improve the leakage performance. Physical characterization details of these structures can be found elsewhere [5].

n-MOSFETs with  $W/L = 10/0.25$  were considered for stress, which were performed on fresh devices with uniform threshold voltages. Constant voltage stress (CVS) was applied with gate bias  $V_g = 1, 1.5, 2$ , and 3 V while constant current stress (CCS) [6] with current densities of 2, 4, 10, and 20 A/cm<sup>2</sup> ( $I_g = 50, 100, 250$ , and 500 nA) were applied at the gate using a semi-automated test measurement setup with HP4156 semiconductor parameter analyzer controlled by a LabVIEW program.

Threshold voltage ( $V_t$ ) and transconductance ( $g_m$ ) were measured at regular stress intervals during 5, 10, 100, and 400 s of stress. The substrate current was measured manually (within 1–2 min) using fixed amplitude charge pumping (FACP) method with amplitude of 1.0 V. The de-trapping time was also found to be longer ( $\sim$  hours) on similar MOS capacitor devices measured in the same die of the wafer [7]. The base voltage of the pulse applied at the gate was swept from 0 to 1.2 V, while the source and the drain were reverse biased by a small voltage of 50 mV. Constant rise and fall times  $t_r = t_f = 100$  ns were maintained when a rectangular pulse of frequency  $f = 1$  MHz at the gate were applied during the measurement. The interface trap density was calculated from the charge pumping current ( $I_{\text{cp}}$ ) measured before and after the stress [4] using the formula  $N_{\text{it}} = I_{\text{cp}}/qAf\#/\text{cm}^2$ , where  $q$  is the electronic charge,  $A$  is the area, and  $f$  is the frequency of the pulse applied.

## III. RESULTS AND DISCUSSION

From Fig. 1(a), a positive shift in threshold voltage ( $\Delta V_t$ ) is observed as the stress time increases, suggesting that electron trapping is dominant in CVS [Fig. 1(a)] and CCS [inset of Fig. 1(a)]. The electron trapping rate increases as the slope of the threshold voltage shift ( $\Delta V_t$ ) also increases with the applied stress time [6]. Curve fit of the data was done using the equation [3]  $\Delta V_t(N_{\text{inj}}) = \Delta V_{\text{max}} \times (1 - \exp(-\sigma_0 \times N_{\text{inj}}))^\beta$  where  $\Delta V_{\text{max}}$  is proportional to total trap density ( $qN/C = V_{\text{max}}$ ),  $\sigma_0$  and  $\beta$  are model parameters [8]. A value of  $1 \times 10^{12}\#/\text{cm}^2$  was taken [8] based on experimentally calculated values, and  $\sigma_0$  and  $\beta$  were fitted for the values of  $1 \times 10^{-14} \text{ cm}^2$  and 0.37~0.45, respectively. As  $N_{\text{inj}} < 1/\sigma_0$ , it confirms that  $\Delta V_t$  follows the power law.

During CVS and CCS, as the injected charge in the oxide increases, increased threshold voltage variation is observed as shown in Fig. 1(b) of  $\Delta V_t$  versus  $Q_{\text{inj}}$  plot. It is seen that the slope  $\delta V_t/\delta Q_{\text{inj}}$  increases as the applied stress voltage (1.5, 2, and 2.5 V) and stress current (inset) increase. The slope variation is higher for 2.5 V compared to that of 2 or 1.5 V. A similar

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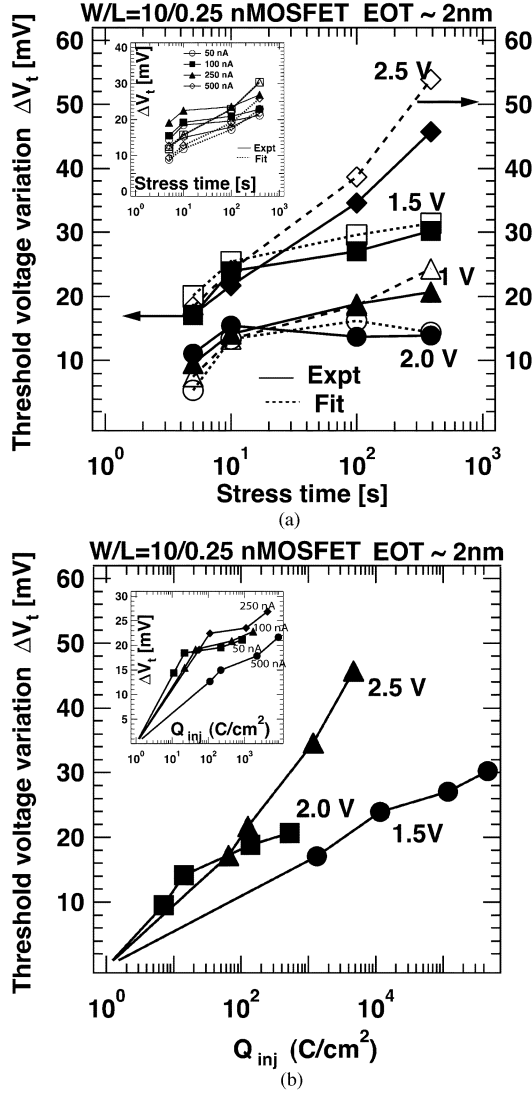


Fig. 1. (a) Change in threshold voltage ( $\Delta V_t$ ) versus stress time during CVS. Inset: change in threshold voltage ( $\Delta V_t$ ) versus stress time during CCS. Thick lines are experimental data and dotted lines indicate model fit. Filled symbols indicate the data obtained from the experiment while the open symbols indicate the data obtained from the equation. (b) Injected charge  $Q_{inj}$  versus change in threshold voltage ( $\Delta V_t$ ) for applied CVS. Inset: injected charge  $Q_{inj}$  versus change in threshold voltage ( $\Delta V_t$ ) for applied CCS. Thick lines are experimental data and dotted lines indicate model fit.

case is observed for CCS, where stress current of 10 A/cm<sup>2</sup> induces greater change compared to 2 A/cm<sup>2</sup>. This suggests that the electron trapping rate increases with the stress voltage and current levels.

Gate current and gate voltage measured during CVS and CCS showed that neutral bulk trap generation might be ruled out as gate current shows negligible change during CVS [9]. Moreover, significant electron trapping might have occurred near the substrate as gate current shows slight decrease for high stress voltages [9], which possibly induced significant positive shift of  $\Delta V_t$  (Fig. 1). The transconductance ( $g_m$ ) and subthreshold slope was seen to degrade over the stress time, suggesting the possibility of interface trap generation.

The charge pumping current, measured before and after CVS and CCS, is found to increase with stress voltage (not shown) and current. A shift in the base voltage level of the curve was

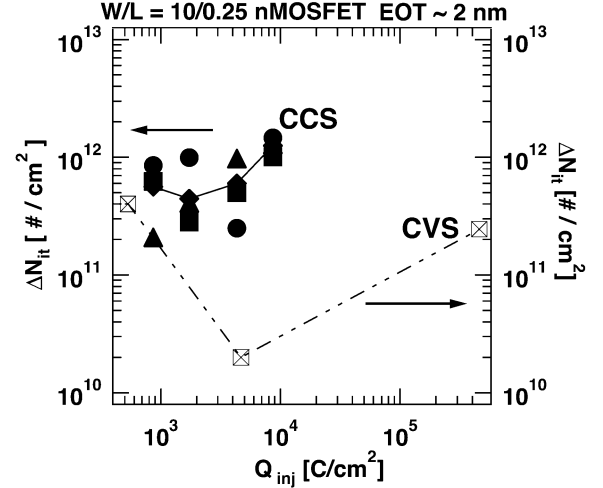


Fig. 2. Change in interface trap density  $\Delta N_{it}$  calculated using FACP during CCS (1° Y axis) and CVS (2° Y axis) before and after CVS.

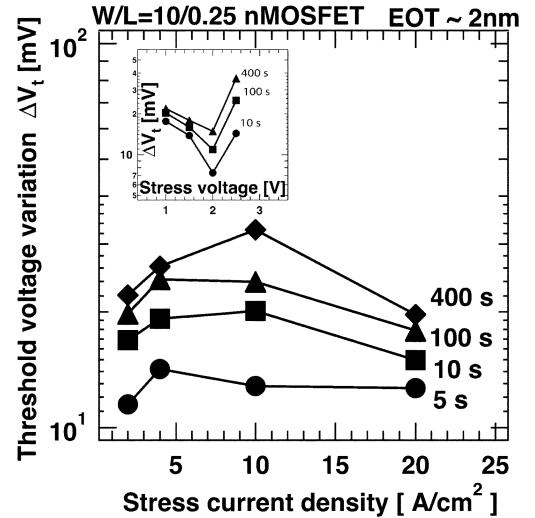


Fig. 3. Change in threshold voltage ( $\Delta V_t$ ) versus stress current density for constant stress times during CCS. Inset: change in threshold voltage ( $\Delta V_t$ ) versus stress voltage for constant stress times during CVS. A turn-around effect is noticed at higher values in both cases.

observed for both the cases. A greater change in oxide trap densities ( $\Delta Q_{ot}$ ) near the IL/high- $\kappa$  and substrate/IL interface (or bulk traps) than a smaller change in interface traps ( $\Delta Q_{it}$ ) was observed [10]. An increase in  $I_{cp}$  after the applied stress also suggests a possible increase in interface traps.

Fig. 2 shows the change in interface trap densities  $\Delta N_{it}$ , calculated before and after the stress of 400 s. A little increase in  $\Delta N_{it}$  with  $Q_{inj}$  during CCS is noticed, suggesting insignificant interface trap generation.  $\Delta N_{it}$  is almost constant during CVS, except for a decrease around 2 V for  $Q_{inj} \sim 4 \times 10^3$  C/cm<sup>2</sup>, showing insignificant trap generation for the applied stress voltages. We also observed from conductance measurements on capacitors with identical gate stack [11] that interface state generation is comparatively insignificant even for higher CVS. Therefore, variation of positive  $\Delta V_t$  for different stress levels is mostly due to electron trapping at bulk hafnium silicate, which also supports our earlier assertions.

The threshold variation is also plotted with applied stress voltage and current densities (Fig. 3). At  $V_g = 1$  V, the electrons

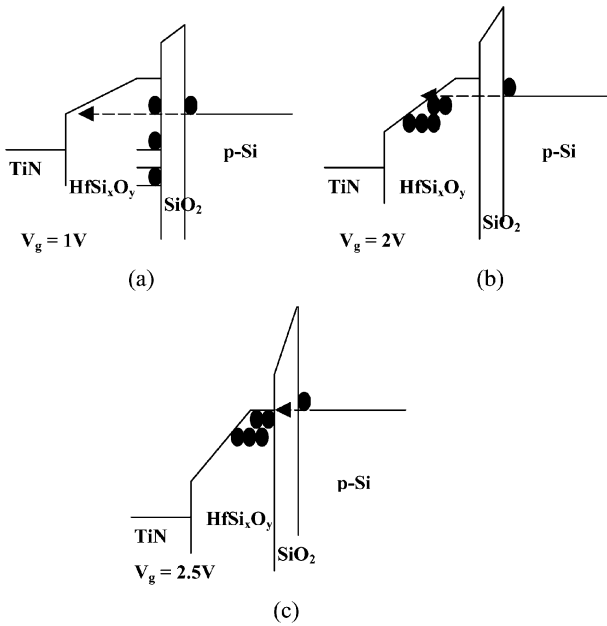


Fig. 4. (a) Band bending induces interface traps at the  $\text{HfSi}_x\text{O}_y/\text{SiO}_2$  interface to be filled. (b) Shallow traps toward the  $\text{TiN}/\text{HfSi}_x\text{O}_y$  interface are filled due to band alignment. (c) Shallow traps near the  $\text{HfSi}_x\text{O}_y/\text{SiO}_2$  interface are filled during stress.

tunneling through the IL from the substrate cannot fill shallow traps due to band alignment [12], but the high- $\kappa$ /IL states at different energy levels [13] are filled [Fig. 4(a)]. This induces a change in  $V_t$ , as the charge centroid resides near the substrate. However, at  $V_g = 2$  V, electrons fill shallow traps [12] from the high- $\kappa$ /IL interface [Fig. 4(b)], which induces comparatively lower  $\Delta V_t$ , as the trapped charge centroid moves away from substrate. However, at  $V_g = 2.5$  V, electrons fill shallow traps near the high- $\kappa$ /IL states [Fig. 4(c)] and moves the charge centroid back to near high- $\kappa$ /IL interface, which induces significant change in  $V_t$ . Such a shift in the charge centroid was earlier observed in silicon dioxide-based devices at low temperatures [14].

At lower current stress ( $I_g = 50$  nA), the gate voltage may induce charge trapping phenomenon as shown in Fig. 4(b). As the stress level is increased ( $I_g = 100$  nA), the gate voltage increases and induces higher  $\Delta V_t$ , which may be due to higher charge trapping near the high- $\kappa$ /IL interface [Fig. 4(c)]. However, at stress levels of  $I_g = 500$  nA, the charge centroid moves toward the gate, as trapped charge redistribution [15] may occur during stress under high electric field, which induces low  $\Delta V_t$ .

#### IV. CONCLUSION

Charge trapping characteristics of an MOCVD  $\text{HfSi}_x\text{O}_y$  (20%  $\text{SiO}_2$ ) gate stack of n-MOSFETs during substrate injection were investigated. Electron trapping is observed from the positive shift of the threshold voltage ( $\Delta V_t$ ) during CVS and CCS. Curve fit of the data confirmed the power law dependence of stress-induced threshold voltage shift. Charge pumping measurements for both cases showed significant electron trapping

at bulk Hf-silicate while interface trap generation was comparatively insignificant. A turn-around effect is noticed for  $\Delta V_t$  as the stress current density increases during CCS. Dependence of spatial distribution of charge trapping at shallow traps in bulk Hf-silicate film on band bending at different gate voltages and redistribution of trapped charges during and after removal of stress may be responsible for turn-around effect.

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