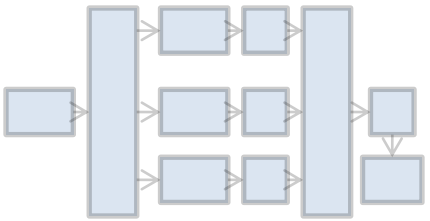
ECE 641 Project
3 Element Frequency Domain Direction of Arrival estimator

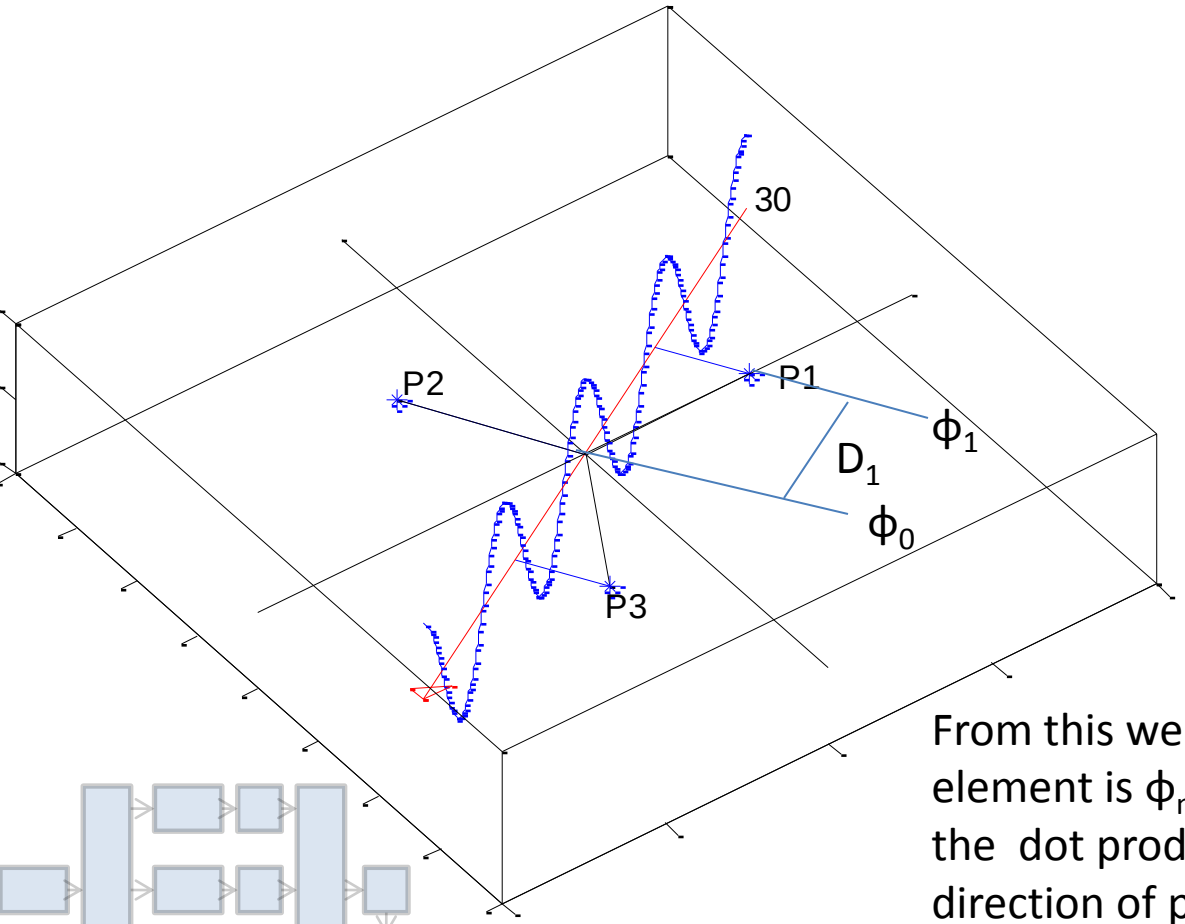
Anthony Rotolo

December 8, 2010



Concept

An array of receivers can be used can be used to determine the direction of arrival of a periodic source. There are many approaches but, this approach based on the relative phases measured at each receiver at a time t_0.



The figure shows a planar wave frozen at time t_0, and the projection of the position vectors of each element onto the direction of propagation. Letting r equal a unit vector in the direction of propagation we can write;

$P_n \cdot r = D_n = (\phi_n - \phi_0)/k$,
where ϕ_0 is the phase at the origin, ϕ_n is the phase measured at the nth element and, $k=2\pi/lambda$.

From this we can see that the phase at each element is $\phi_n = \phi_0 + D_n * k$, and is proportional to the dot product of the position vector and the direction of propagation.

Important Condition

Given N arbitrary equally spaced points P on a circle of radius r, where N>2

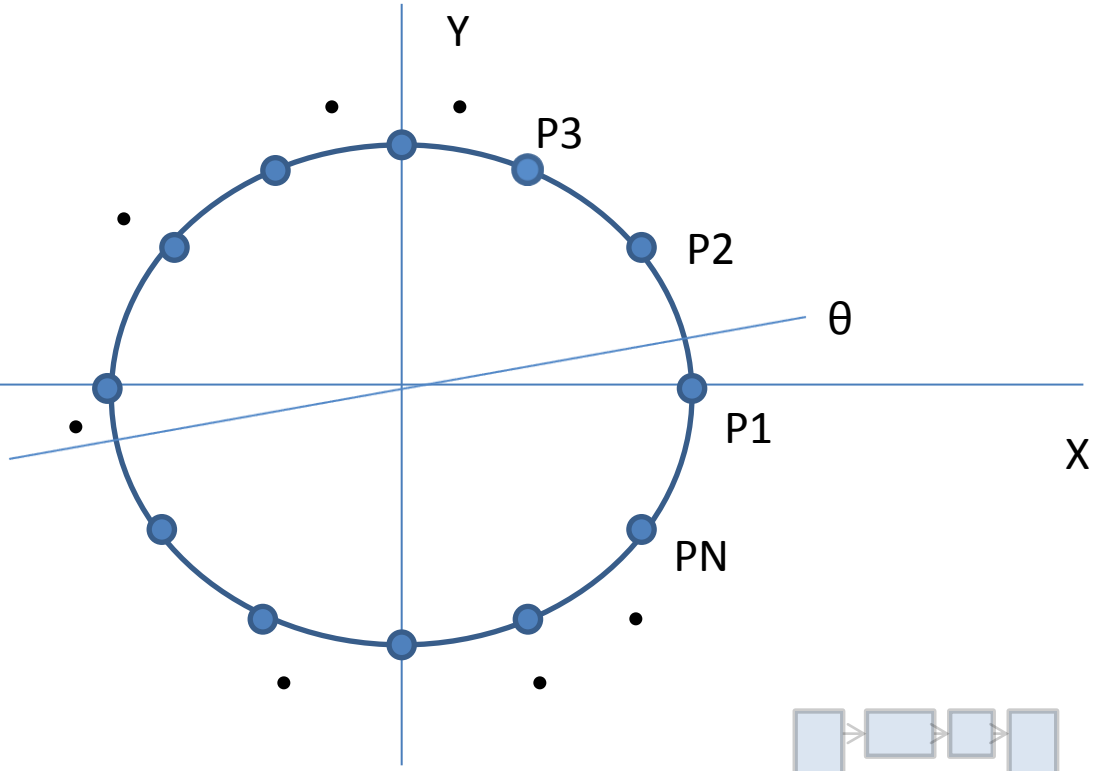
The Matrix of direction vectors defined by;

$$P=\begin{bmatrix} P1x, P2x, P3x \ldots\ldots PNx \\ P1y, P2y, P3y, \ldots\ldots PNy \end{bmatrix}$$

Exhibits orthogonal properties, because it is made up of sines and cosines, such that:

$$P*P^{T} = R^{2}N/2*\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$$

This property will allow the dot product to be preserved, and avoid the computation of an inverse.



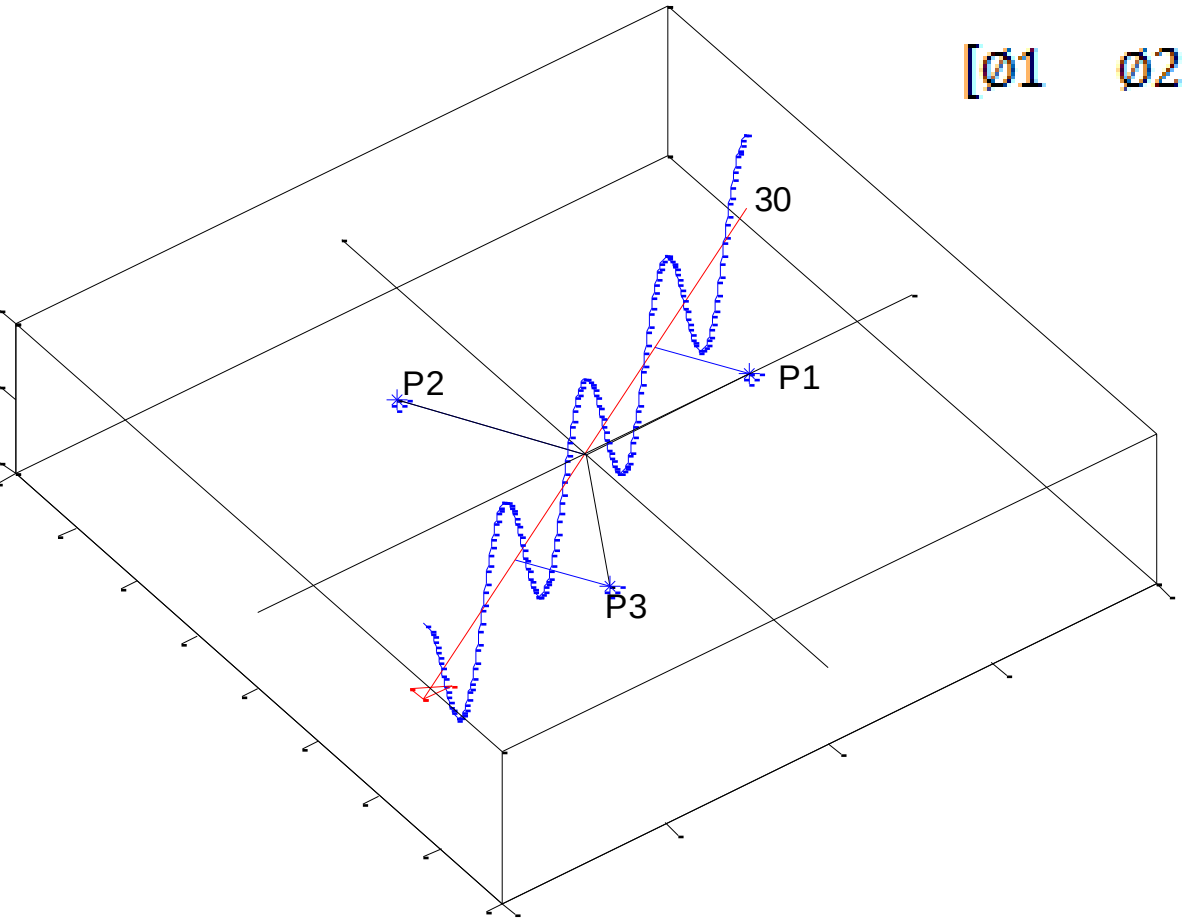
Concept Continued

Given the previous condition:

$$[P1 \cdot r \quad P3 \cdot r \quad P3 \cdot r] * \begin{matrix} P1 \\ [P2] \\ P3 \end{matrix} = c * r$$

and thus:

$$[\emptyset 1 \quad \emptyset 2 \quad \emptyset 3] * \begin{matrix} P1 \\ [P2] \\ P3 \end{matrix} \propto c * r$$



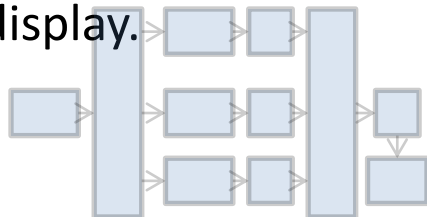
This result is sufficient to calculate DOA as the arctangent of the sum of the x and y components of c · r, given some important conditions:

1. The diameter of the circle on which the array lies, in less then lambda /2.
2. None of the measured phases exceed π.

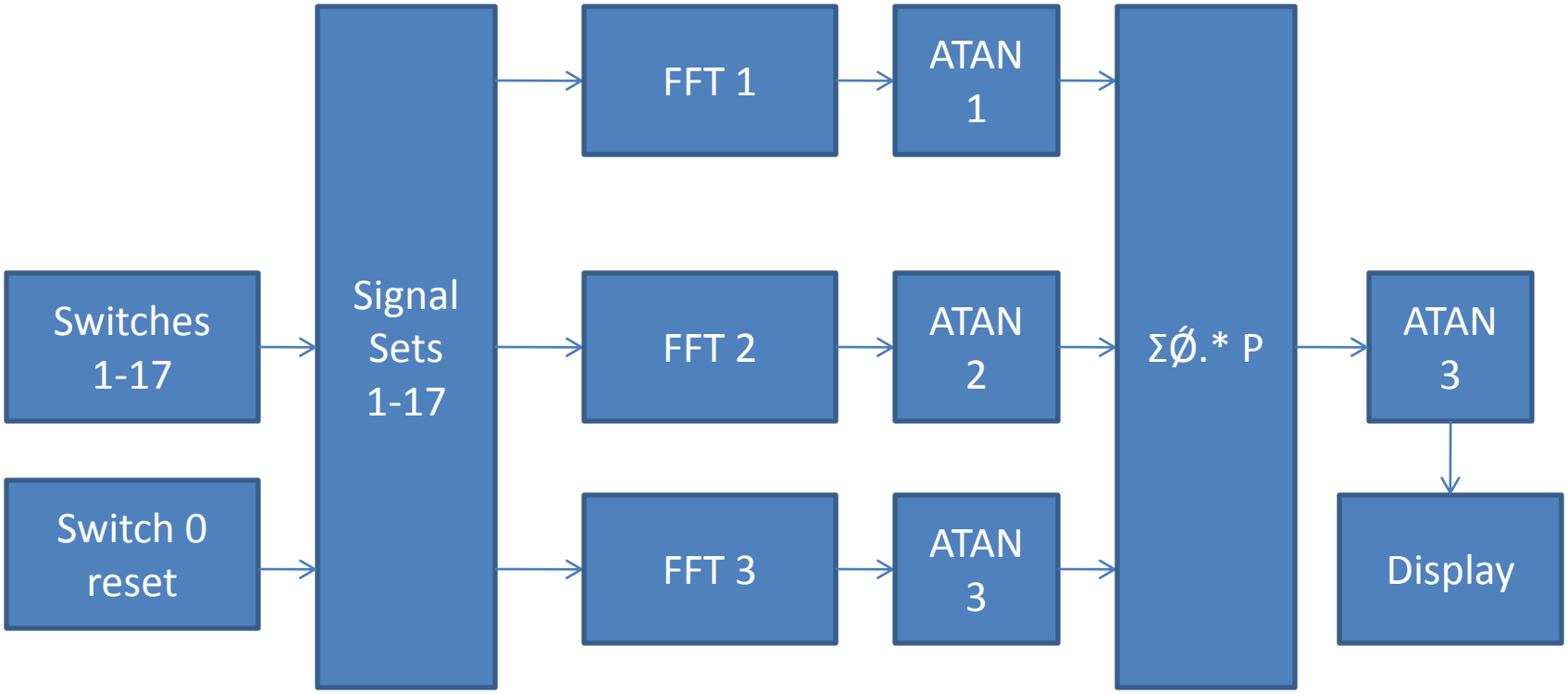
Code Description

The project code consists of a main program and three functions.

- The main routine reads the input, maps and calls functions and computes corrections to the ARCTAN.
- The functions are:
  - A radix-2 length 16 fft (modified from the provided fft)
  - An polynomial arctangent estimation function that was provided with the course material, and takes 9 bit inputs from -256 to 255 representing (255:-256)/256.
  - And an output routine that takes 5 length 4 vectors,
    - 4 correspond to BCDs and are mapped to length 7 vectors to be connected to the segmented LEDs,
    - the fifth is mapped to the 4 dots on the segmented display.

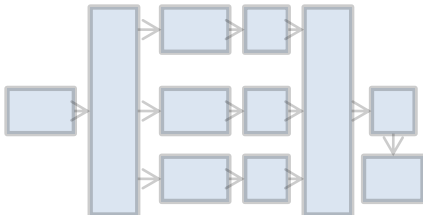


Process Flow Chart

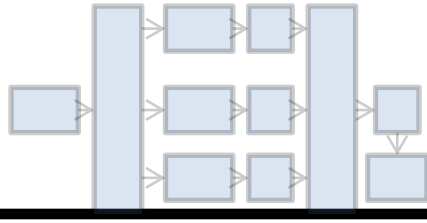


Process Flow

- Read switches 1-17
- Write signal data (1-3) corresponding to switch selection into FFTs (1-3) if reset is low.
- Compute the phase of each output at the appropriate frequency using arctan.
- Correct phase values resulting from arctan limitation .
- Compute $r=C \cdot \Sigma -\phi_n \cdot P_n$ for $C \cdot rx$ and $C \cdot ry$.
- Compute direction of source with arctan using ry/rx
- Correct direction of source based on arctan limitation.
- Convert direction of the source to Binary Coded Decimal
- Map BCD values to segmented display values.



Fitter Summary



Quartus II - C:/Users/Sara/Desktop/ece641/ECE641_Materials_new/VHDL/project/project_main - project_main - [Compilation Report - Fitter Summary]

File Edit View Tools Window

- Compilation Report
  - Legal Notice
  - Flow Summary
  - Flow Settings
  - Flow Non-Default Global Se
  - Flow Elapsed Time
  - Flow OS Summary
  - Flow Log
  - Analysis & Synthesis
  - Fitter
    - Summary
    - Settings
    - Parallel Compilation
    - Netlist Optimizations
    - Incremental Compilatio
    - Pin-Out File
    - Resource Section
    - Device Options
    - Operating Settings and
    - Estimated Delay Added
    - Messages
  - Assembler
  - Timing Analyzer

Fitter Summary

Fitter Status	Successful - Mon Dec 06 11:58:34 2010
Quartus II Version	9.1 Build 222 10/21/2009 SJ Web Edition
Revision Name	project_main
Top-level Entity Name	project_main
Family	Cyclone II
Device	EP2C70F896C6
Timing Models	Final
Total logic elements	10,575 / 68,416 (15 %)
Total combinational functions	9,685 / 68,416 (14 %)
Dedicated logic registers	3,977 / 68,416 (6 %)
Total registers	3977
Total pins	69 / 622 (11 %)
Total virtual pins	0
Total memory bits	0 / 1,152,000 (0 %)
Embedded Multiplier 9-bit elements	84 / 300 (28 %)
Total PLLs	0 / 4 (0 %)

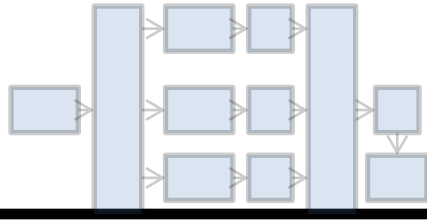
Worst-case tco 12.400 ns, svalout2[1], sout2[4], clk, -- 0

Fmax 8.91 MHz

For Help, press F1

Questions?

Worst-case tco



Quartus II - C:/Users/Sara/Desktop/ece641/ECE641_Materials_new/VHDL/project/project_main - project_main - [Compilation Report - Timing Analyzer Su...

File Edit View Tools Window

- Analysis & Synthesis
- Fitter
  - Summary
  - Settings
  - Parallel Compilation
  - Netlist Optimizations
  - Incremental Compila
  - Pin-Out File
  - Resource Section
  - Device Options
  - Operating Settings a
  - Estimated Delay Add
  - Messages
- Assembler
- Timing Analyzer
  - Summary
  - Settings
  - Clock Settings Summ
  - Parallel Compilation
  - Clock Setup: 'clk'
  - tsu
  - tco
  - tpd
  - th
  - Messages
- TimeQuest Timing Anal

Timing Analyzer Summary

	Type	Slack	Required Time	Actual Time	From	To	From Clock	To Clock	Failed Paths
1	Worst-case tsu	N/A	None	12.309 ns	reset	atfout2[9]	--	clk	0
2	Worst-case tco	N/A	None	12.400 ns	svalout2[1]	sout2[4]	clk	--	0
3	Worst-case tpd	N/A	None	11.575 ns	reset	resethigh	--	--	0
4	Worst-case th	N/A	None	-4.113 ns	mics40on	XRE3[7]	--	clk	0
5	Clock Setup: 'clk'	N/A	None	8.91 MHz (period = 112.241 ns)	YIMout[1]	xout[8]	clk	clk	0
6	Total number of failed paths								0

For Help, press F1

Results from MATLAB

