Length-4 DIT IFFT Design

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DFT & IDFT

$$X(k) = DFT[x(n)] = \sum_{n=0}^{N-1} x(n) W_N^{nk} \qquad (1)$$

$$X(n) = IDFT[X(k)] = \frac{1}{N} \sum_{k=0}^{N-1} X(k) W_N^{-nk} \qquad (2)$$

There are two FFT algorithms- DIF_FFT and DIT_FFT.

I. DIF (Decimation In Frequency)FFT

Cooley–Tukey FFT algorithm

$$Y(k) = \sum_{n=0}^{N/2-1} x(n)W_N^{kn} + W_N^{kN/2} \sum_{n=0}^{N/2-1} x(n+N/2)W_N^{kn}$$

$$= \sum_{n=0}^{N/2-1} [x(n) + (-1)^k x(n+N/2)]W_N^{kn}; \quad k = 0,1,\ldots,N-1$$

$$Y(2r) = \sum_{n=0}^{N/2-1} [x(n) + x(n+N/2)]W_{N/2}^{rn}$$

$$Y(2r+1) = \sum_{n=0}^{N/2-1} [x(n) - x(n+N/2)]W_N^n W_{N/2}^{rn}$$

I. DIF _FFT Butterfly Diagram

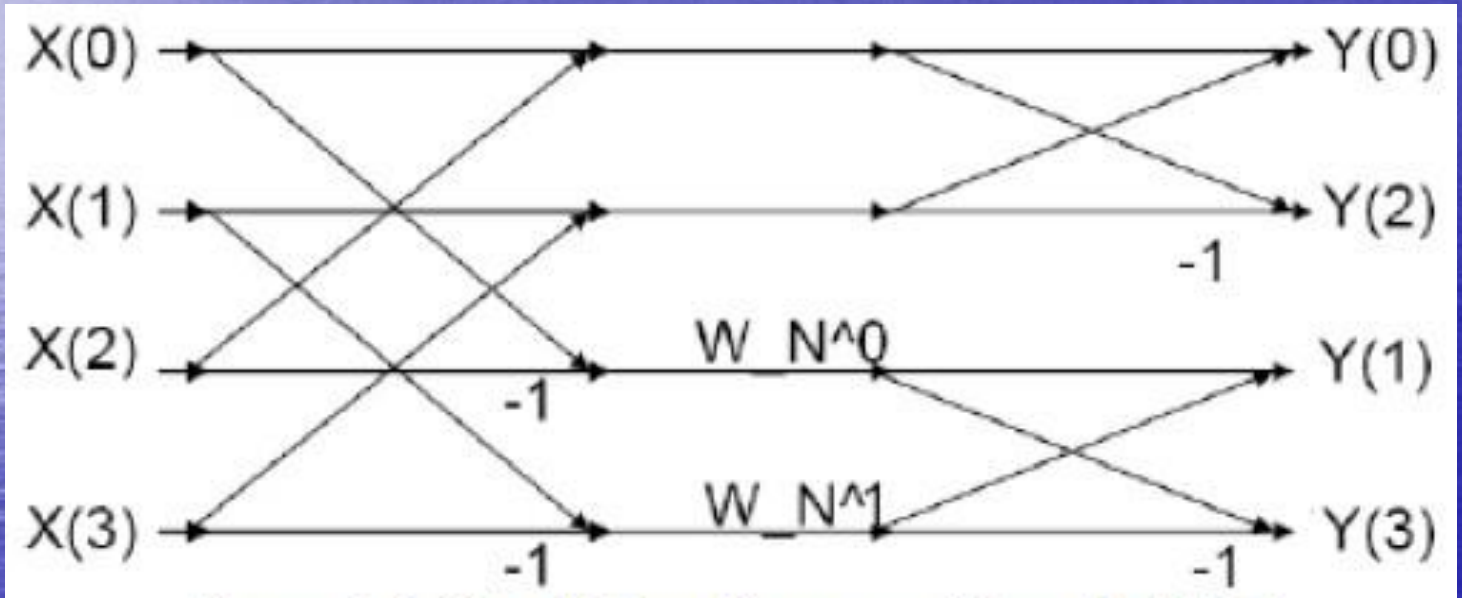


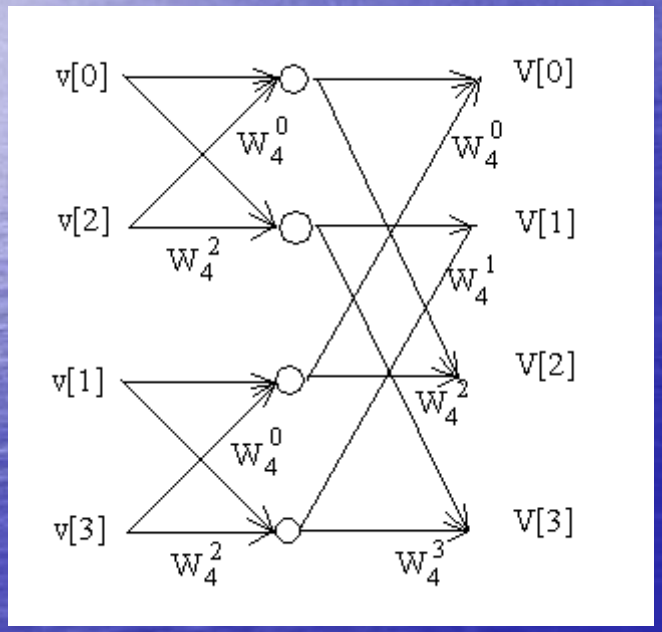
Figure 6.1: Signal Flow Diagram of length-4 FFT

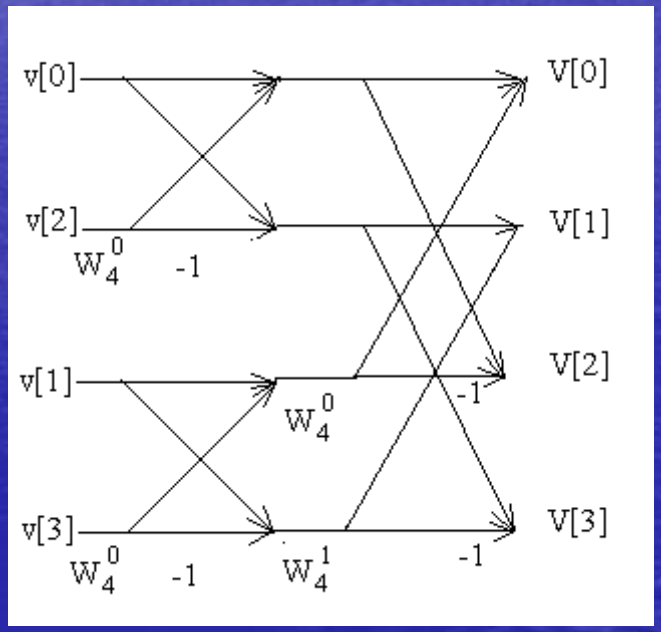
II. DIT (Decimation In Time)FFT

Decimation-in-time (DIT) Radix-2 FFT

$$
\begin{aligned}
X(k) &= \sum_{n=0}^{N-1}\left(x(n)\,e^{-\left(i\frac{2\pi nk}{N}\right)}\right) \\
&= \sum_{n=0}^{\frac{N}{2}-1}\left(x(2n)\,e^{-\left(i\frac{2\pi(2n)k}{N}\right)}\right)+\sum_{n=0}^{\frac{N}{2}-1}\left(x(2n+1)\,e^{-\left(i\frac{2\pi(2n+1)k}{N}\right)}\right) \\
&= \sum_{n=0}^{\frac{N}{2}-1}\left(x(2n)\,e^{-\left(i\frac{2\pi nk}{\frac{N}{2}}\right)}\right)+e^{-\left(i\frac{2\pi k}{N}\right)}\sum_{n=0}^{\frac{N}{2}-1}\left(x(2n+1)\,e^{-\left(i\frac{2\pi nk}{\frac{N}{2}}\right)}\right) \\
&= \mathrm{DFT}_{\frac{N}{2}}\left[\left[x(0),x(2),\ldots,x(N-2)\right]\right]+W_N^k\,\mathrm{DFT}_{\frac{N}{2}}\left[\left[x(1),x(3),\ldots,x(N-1)\right]\right]
\end{aligned}
$$

II. DIT_FFT Butterfly Diagram





III. DIF_FFT Derivation

DIF-FFT:

$k=0$ & $r=0$: $Y(0) = (x(0)+x(2))\cdot W_2^{0\cdot 0} + (x(1)+x(3))\cdot W_2^{0\cdot 1}$

$= [x(0)+x(2)] + [x(1)+x(3)]$

$k=1$ & $r=0$: $Y(1) = [(x(0)-x(2))W_N^0]\cdot W_2^{0\cdot 0} + [(x(1)-x(3))W_N^1]\cdot W_2^{0\cdot 1}$

$= (x(0)-x(2))W_N^0 + (x(1)-x(3))W_N^1$

$k=2$ & $r=1$: $Y(2) = (x(0)+x(2))\cdot W_2^{1\cdot 0} + (x(1)+x(3))\cdot W_2^{1\cdot 1}$

$= [x(0)+x(2)] - [x(1)+x(3)]$

$k=3$ & $r=1$: $Y(3) = [(x(0)-x(2))\cdot W_N^0]\cdot W_2^{1\cdot 0} + [(x(1)\pm x(3))\cdot W_N^1]\cdot W_2^{1\cdot 1}$

$= [x(0)-x(2)]W_N^0 - [(x(1)-x(3))W_N^1]$

bfproc1 cmul1 bfproc2 bfproc1 cmul2

III. DIT_FFT Derivation

DIT-FFT:

$$X(0) = (x(0)\cdot W_2^{0\cdot 0} + x(2) W_2^{0\cdot 1}) + W_N^0 (x(1)\cdot W_2^{0\cdot 0} + x(3)\cdot W_2^{0\cdot 1})$$

$$= (x(0)+x(2)) + (x(1)+x(3))$$

$$X(1) = (x(0)\cdot W_2^{1\cdot 0} + x(2) W_2^{1\cdot 1}) + W_4^1 (x(1)\cdot W_2^{1\cdot 0} + x(3) W_2^{1\cdot 1})$$

$$= (x(0) - x(2)) + W_4^1 (x(1) - x(3))$$

$$X(2) = (x(0)\cdot W_2^{2\cdot 0} + x(2) W_2^{2\cdot 1}) + W_4^2 (x(1)\cdot W_2^{2\cdot 0} + x(3) W_2^{2\cdot 1})$$

$$= (x(0)+x(2)) - (x(1)+x(3))$$

$$X(3) = (x(0)\cdot W_2^{3\cdot 0} + x(2) W_2^{3\cdot 1}) + W_4^3 (x(1)\cdot W_2^{3\cdot 0} + x(3) W_2^{3\cdot 1})$$

$$= (x(0) - x(2)) - W_4^1 (x(1) - x(3))$$

↓ bfproc1 ↓ bfproc2 ↓ cmul ↓ bfproc1

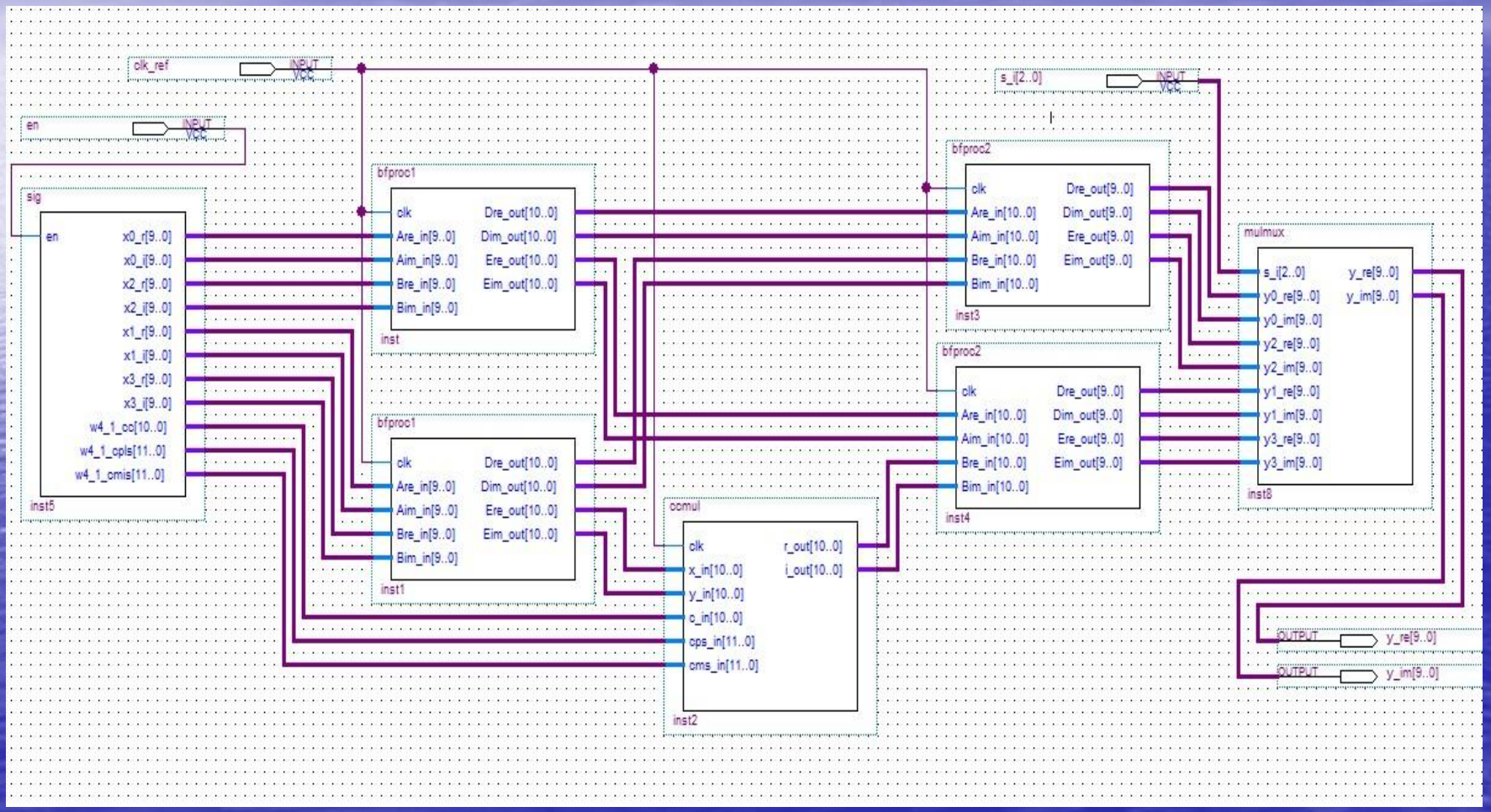
IV. Modify FFT to IFFT: Complex Multiplication

To improve the calculation precision, we expand the twiddle by 500 times, i.e. C+jS=500*Wn, and divide the final result by 500 at last.

```
For FFT:
    C=0, S=-1;
then
    C*500       =w4_1_cc=0;
    (C+S)*500   =w4_1_cps=-500;
    (C+S)*500   =w4_1_cms=500;


For IFFT:
    C=0, S=1;
then
    C*500       =w4_1_cc=0;
    (C+S)*500   =w4_1_cps=500;
    (C+S)*500   =w4_1_cms=-500;
```

V. DIT-IFFT(inverse of DIF-FFT)

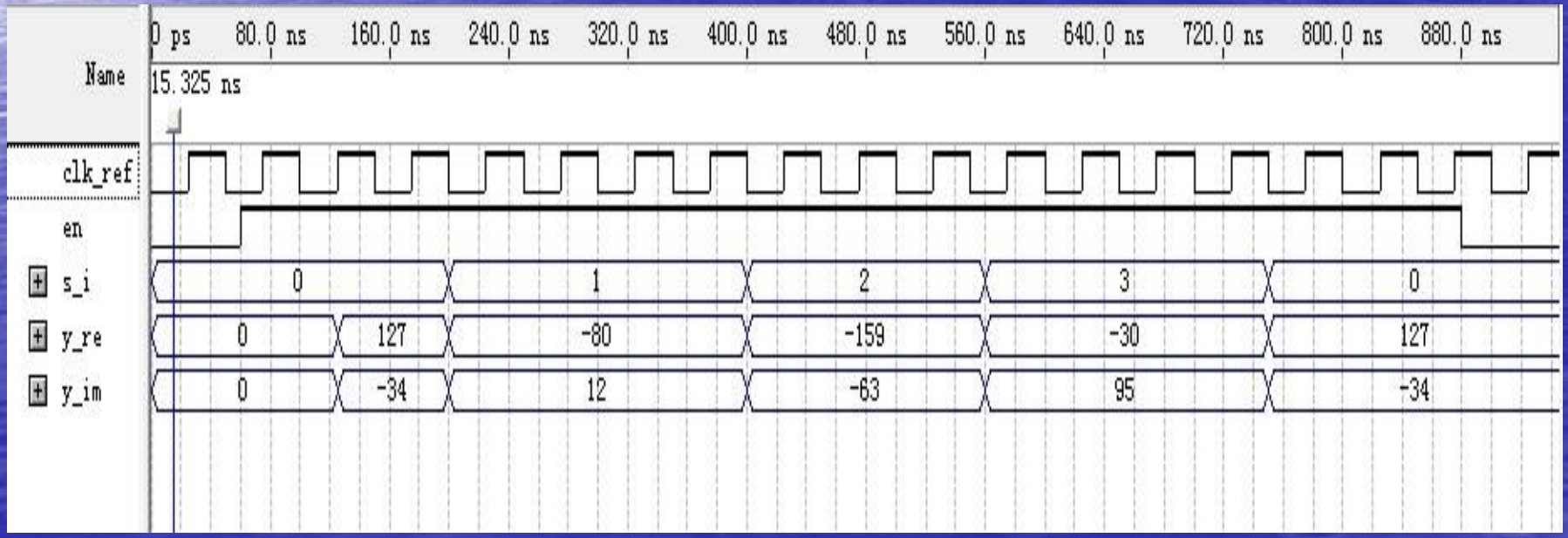


V. DIT-IFFT(inverse of DIF-FFT)

```
x=[127-34i, -80+12i, -159-63i, -30+95i]
y=fft(x)
```

The result is

```
y = -142 + 10i    203 + 79i    78 - 204i    369 - 21i
```



V. DIT-IFFT(inverse of DIF-FFT)

Flow Status	Successful - Thu Dec 15 06:51:03 2011
Quartus II Version	9.1 Build 222 10/21/2009 SJ Web Edition
Revision Name	ifft4_vhdl
Top-level Entity Name	ifft4_vhdl
Family	Cyclone II
Device	EP2C70F896C6
Timing Models	Final
Met timing requirements	Yes
Total logic elements	726 / 68,416 (1 %)
Total combinational functions	725 / 68,416 (1 %)
Dedicated logic registers	44 / 68,416 (< 1 %)
Total registers	44
Total pins	25 / 622 (4 %)
Total virtual pins	0
Total memory bits	0 / 1,152,000 (0 %)
Embedded Multiplier 9-bit elements	4 / 300 (1 %)
Total PLLs	0 / 4 (0 %)

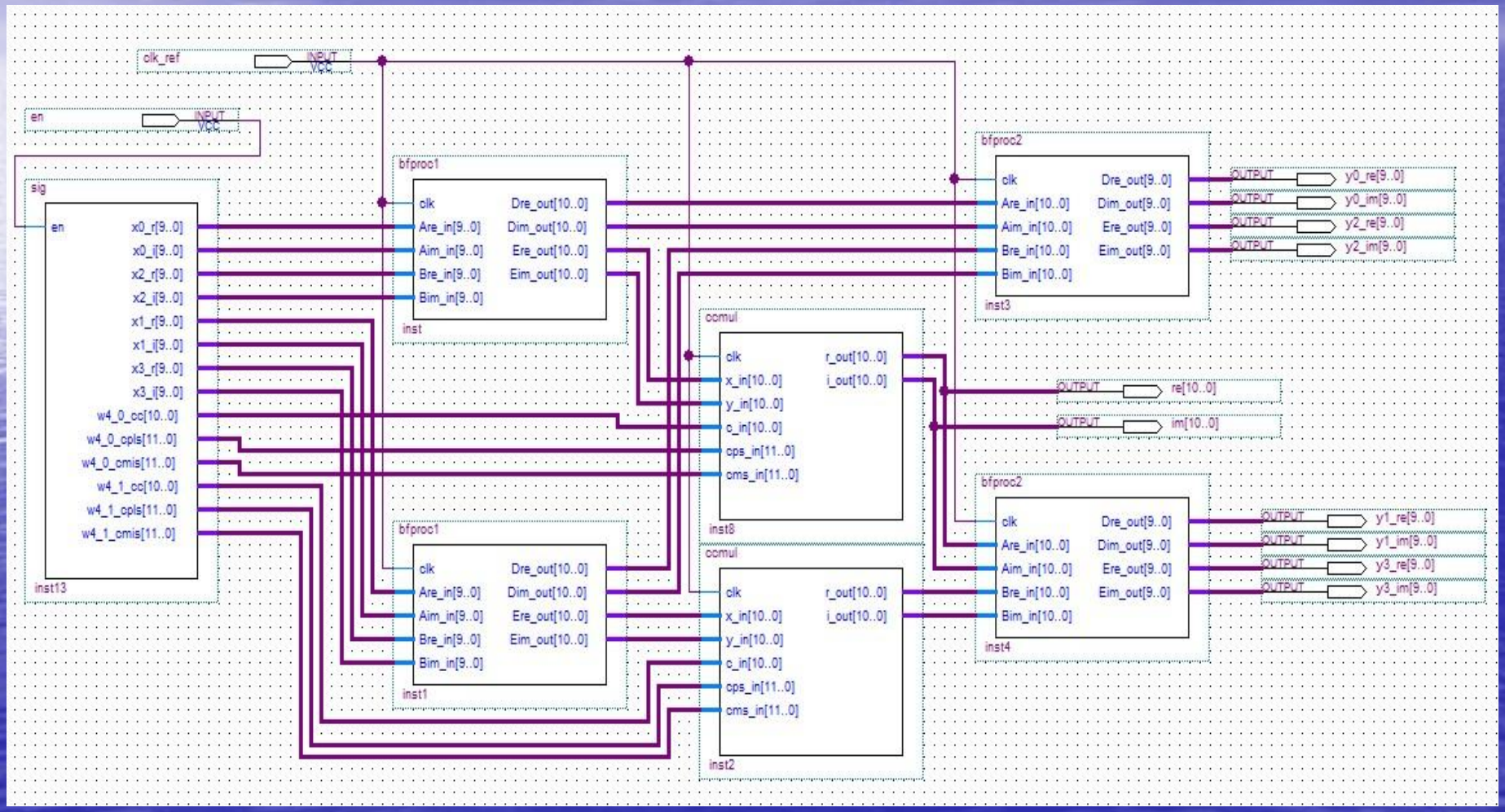
V. DIT-IFFT(inverse of DIF-FFT)

	Fmax	Restricted Fmax	Clock Name	Note	
1	22.27 MHz	22.27 MHz	clk_ref		

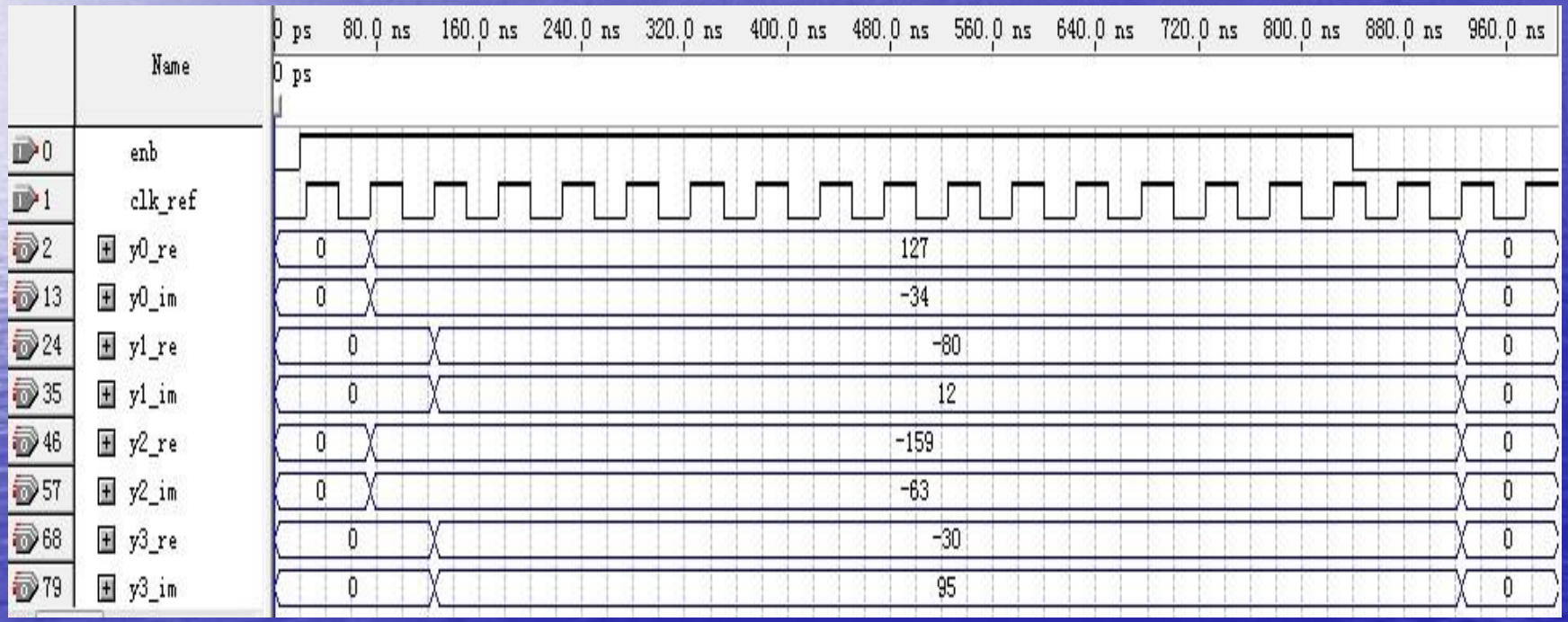
Timing Analyzer Summary

	Type	Slack	Required Time	Actual Time	From	To	From Clock	To Clock	Failed Paths
1	Worst-case tsu	N/A	None	4.783 ns	en	ccmul:inst2|cms[3]~_Duplicate_6	--	clk_ref	0
2	Worst-case tco	N/A	None	13.625 ns	bfproc2:inst4|Fim[1]	y_im[7]	clk_ref	--	0
3	Worst-case tpd	N/A	None	14.400 ns	s_i[2]	y_im[0]	--	--	0
4	Worst-case th	N/A	None	-4.039 ns	en	ccmul:inst2|cms[3]~_Duplicate_5	--	clk_ref	0
5	Clock Setup: 'clk_ref'	N/A	None	22.27 MHz (period = 44.904 ns)	ccmul:inst2|y[2]	bfproc2:inst4|Fim[11]	clk_ref	clk_ref	0
6	Total number of failed paths								0

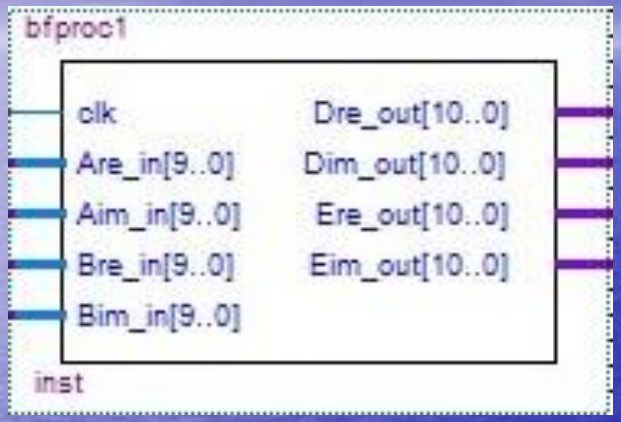
VI. DIF-IFFT(inverse of DIT-FFT)



VI. DIF-IFFT(inverse of DIT-FFT)



VII. Note

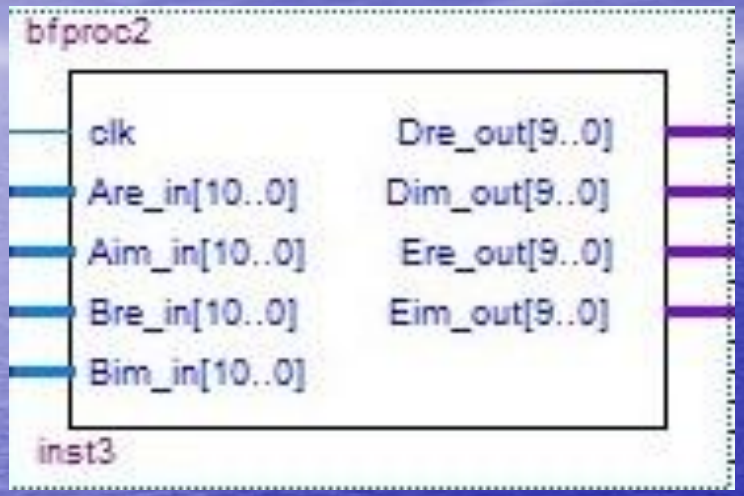


The max input value is "369";
"369" in binary form:

0 1 0 1 1 1 0 0 0 1 (10-bit: [9..0])

The most significant bit is set as sign bit.

VII. Note




```
Dre_out <= Fre/4;
Dim_out <= Fim/4;
Ere_out <= Gre/4;
Eim_out <= Gim/4;
```

- Thank You.