OFDM transceiver with QPSK modulation

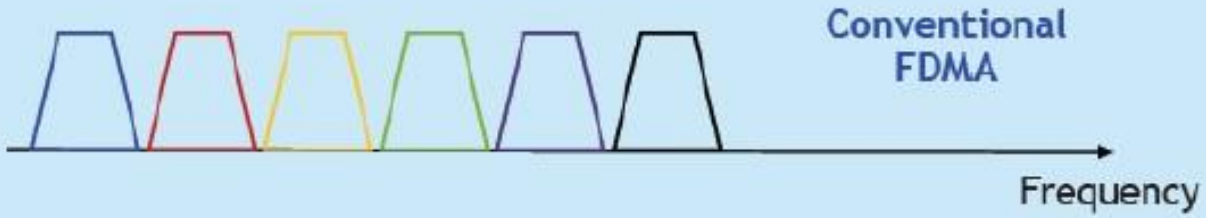
ECE 641 Project

Chen Li

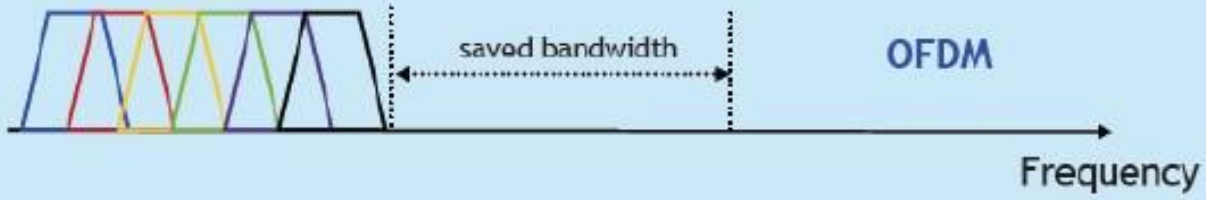
Dec 11, 2012

OFDM general description

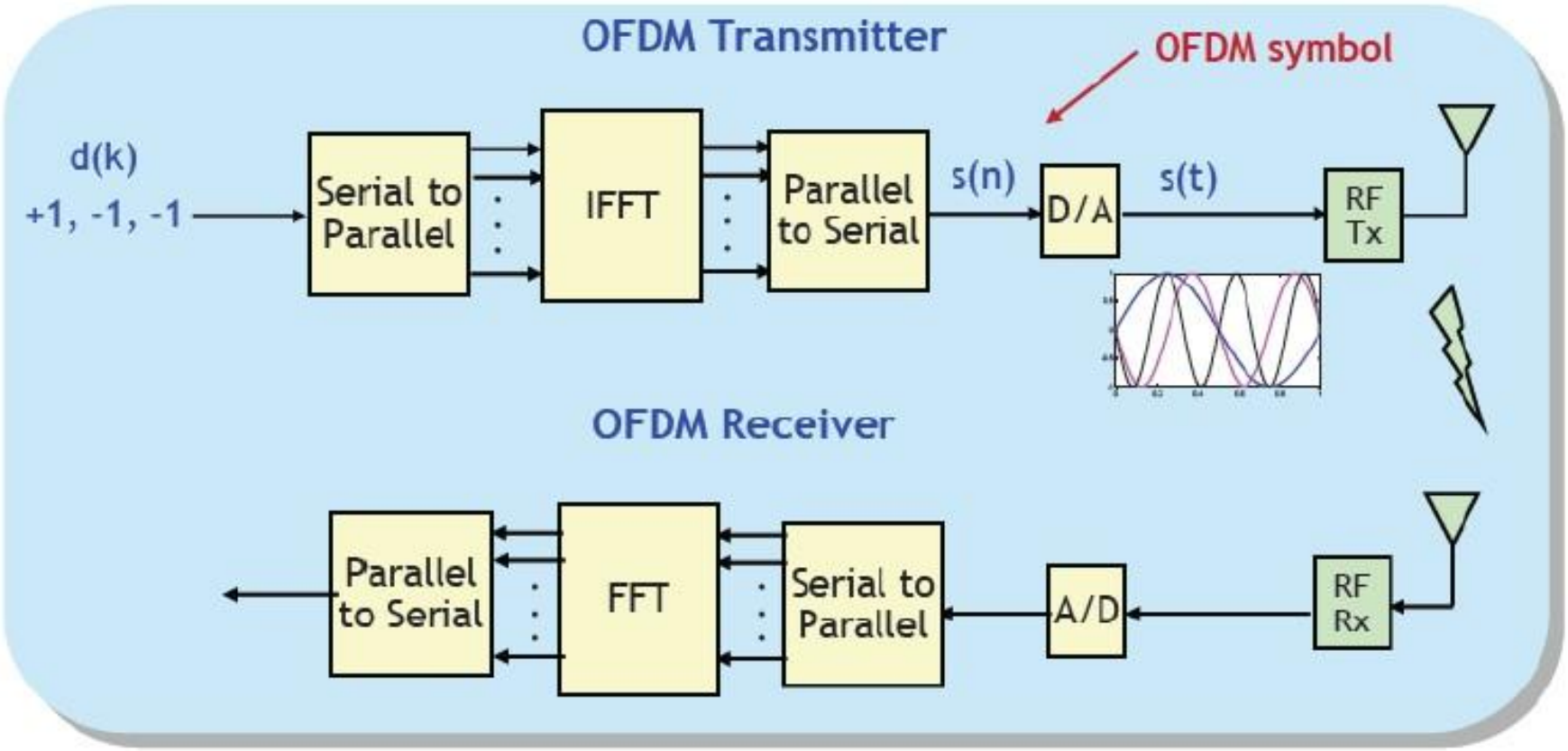
- OFDM: Orthogonal Frequency Division Multiplexing
- OFDMA: Orthogonal Frequency Division Multiple Access
- FDM is nothing new: carriers are separated sufficiently in frequency so that there is minimal overlap to prevent cross-talk



- OFDM: still FDM, but carriers can actually be orthogonal (no cross-talk) while actually overlapping, if specially designed → saved bandwidth!



OFDM transceiver block diagram



Major blocks in my design

- Serial-Parallel, Parallel-Serial convertor
- 4 points FFT(Fast Fourier Transform) and Inverse FFT
- D/A, A/D convertor
- QPSK modulator and demodulator

FFT and Inverse FFT

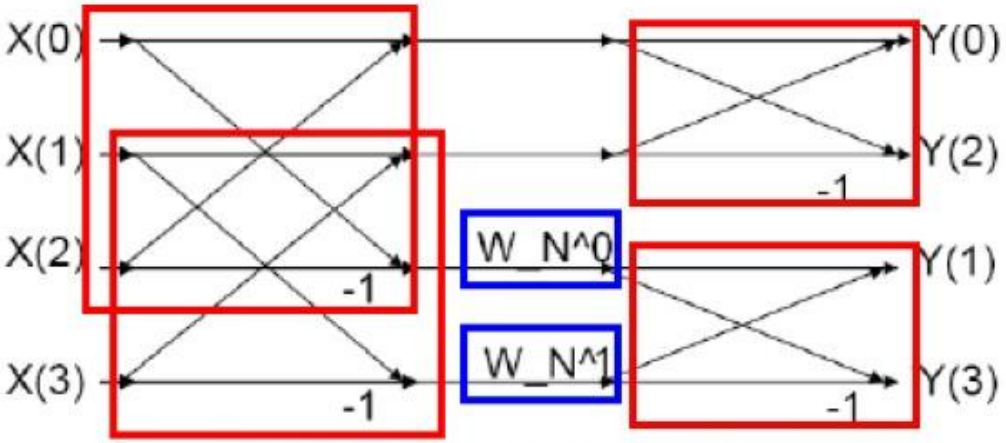


Figure 6.2: Six Blocks of length-4 FFT

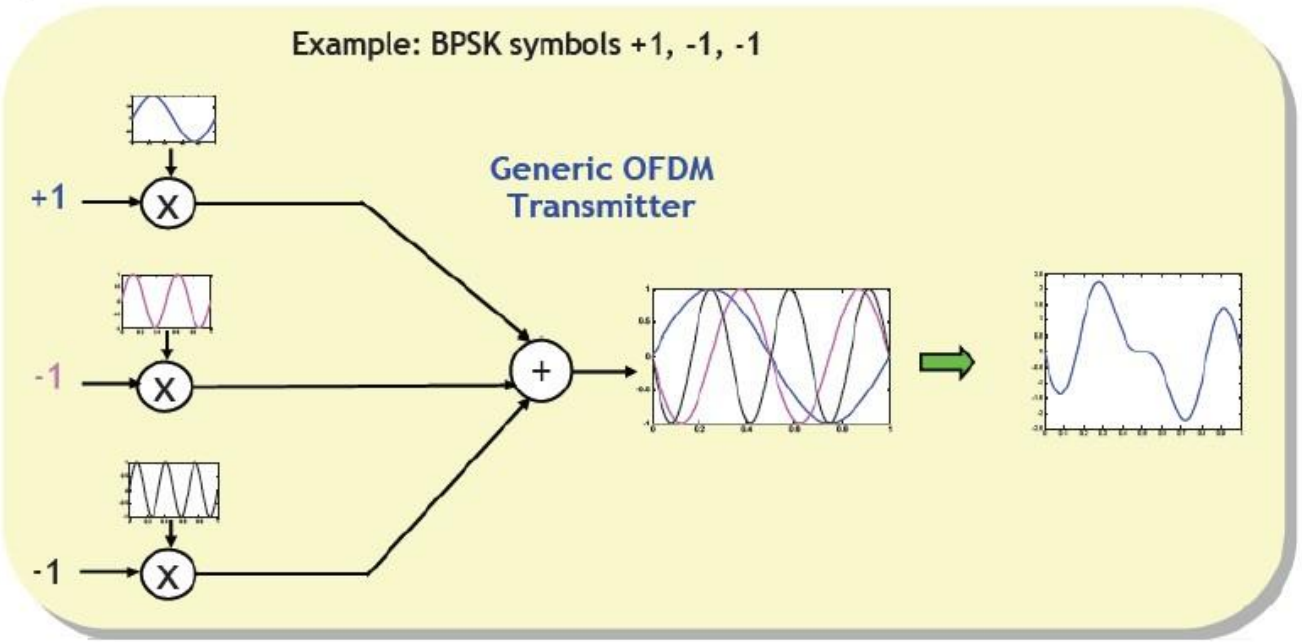
$DFT(FFT)$:

$$X(k)=\sum_{n=0}^{N-1}x(n)\cdot e^{-j\left(\frac{2\pi}{N}\right)nk}\ (k=0,1,\ldots,N-1)$$

$IDFT(IFFT)$:

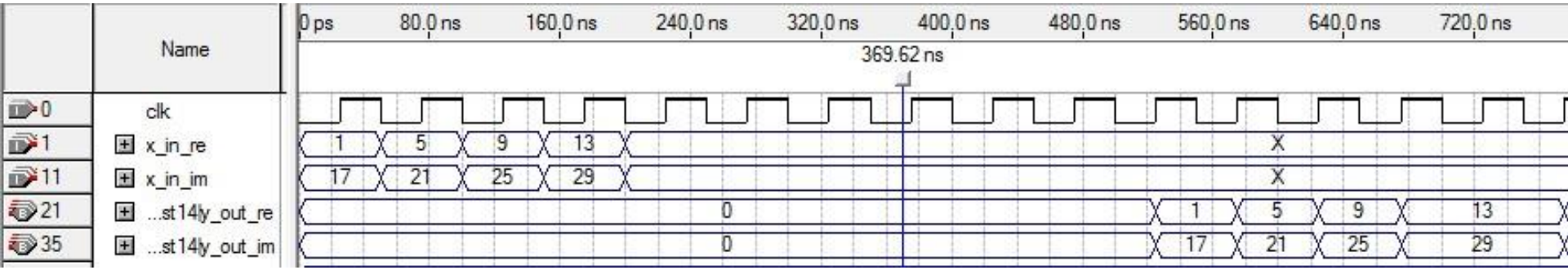
$$x(n)=\frac{1}{N}\sum_{k=0}^{N-1}X(k)\cdot e^{j\left(\frac{2\pi}{N}\right)nk}\ (n=0,1,\ldots,N-1)$$

QPSK modulation



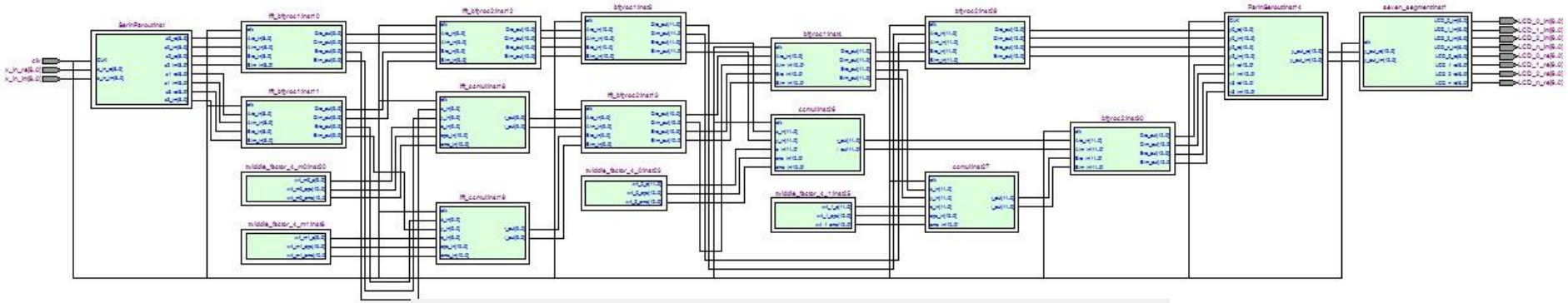
A channel	**1**	**0**	**0**	**1**
B channel	1	1	0	0
Phase A	0 degree	180degree	180degree	0 degree
Phase B	90 degree	90 degree	270degree	270degree
Modulated Phase	45 degree	135degree	225degree	315degree

Simulation result



- Serial data inputs every clock cycle, calculated and transmit data, the receiver collect data and reverse calculated, retrieve data after 8 clock cycles.

RTL and flow summary



Flow Status	Successful - Mon Dec 10 18:44:19 2012
Quartus II Version	9.1 Build 222 10/21/2009 SJ Web Edition
Revision Name	final_project
Top-level Entity Name	final_project
Family	Cyclone II
Device	EP2C70F896C6
Timing Models	Final
Met timing requirements	Yes
Total logic elements	6,311 / 68,416 (9 %)
Total combinational functions	6,161 / 68,416 (9 %)
Dedicated logic registers	653 / 68,416 (< 1 %)
Total registers	653
Total pins	75 / 622 (12 %)
Total virtual pins	0
Total memory bits	0 / 1,152,000 (0 %)
Embedded Multiplier 9-bit elements	20 / 300 (7 %)
Total PLLs	0 / 4 (0 %)

Inputs and outputs on DE2-70

