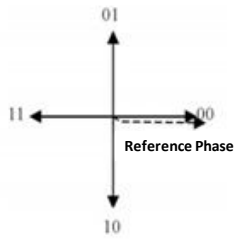
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QDPSK Modulation And Demodulation Processing

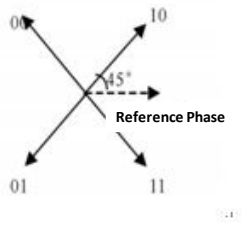
By Qi Liu (31086507)

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QDPSK -- Quadrature Differential Phase Shift Keying



A

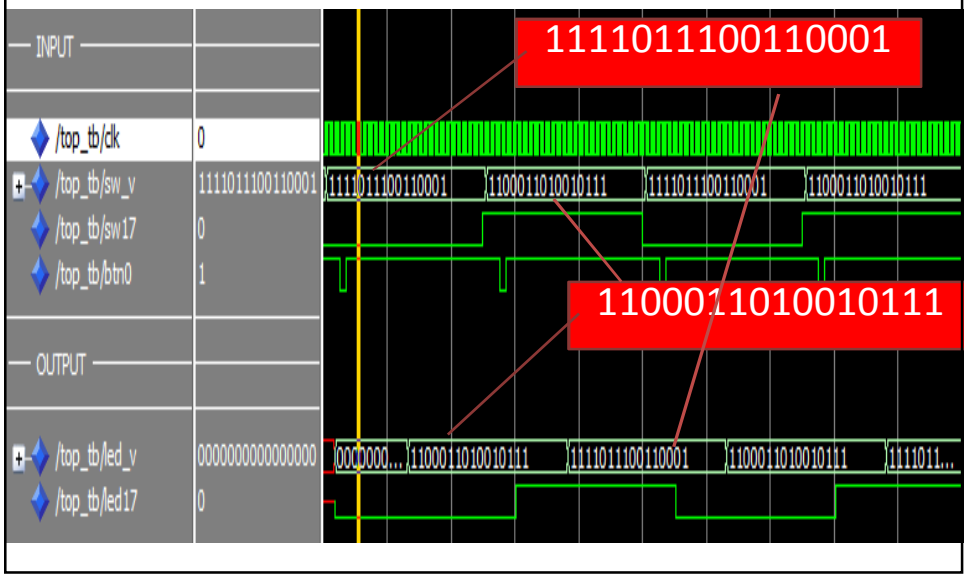


B..

The difference of input data phase Δϕ can be obtained by relative phase (fig. A), and then according to the differenceΔϕ, we can modulate the code by absolute phase (fig. B) and get the output code sequence.

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The Simulation Result By Modelsim



Previous code state and phrase			Current code state and phrase			Output code state and phrase		
C_{n-1}	d_{n-1}	ϕ_{n-1}	A_{n-1}	b_{n-1}	$\Delta\phi$	C_n	d_n	ϕ_n
0	0	135°	0	0	0°	0	0	135°
			0	1	90°	0	1	225°
			1	1	180°	1	1	315°
			1	0	270°	1	0	45°
0	1	225°	0	0	0°	0	1	225°
			0	1	90°	1	1	315°
			1	1	180°	1	0	45°
			1	0	270°	0	0	135°
1	1	315°	0	0	0°	1	1	315°
			0	1	90°	1	0	45°
			1	1	180°	0	0	135°
			1	0	270°	0	1	225°
1	0	45°	0	0	0°	1	0	45°
			0	1	90°	0	0	135°
			1	1	180°	0	1	225°
			1	0	270°	1	1	315°

The Truth Table Of The Modulation Section

Previous code state and phrase		Current code state and phrase		Output code state and phrase	
C_{n-1} d_{n-1}	ϕ_{n-1}	A_{n-1} b_{n-1}	$\Delta\phi$	C_n d_n	ϕ_n
0 0	135°	0 0	0°	0 0	135°
		0 1	90°	0 1	225°
		1 1	180°	1 1	315°
		1 0	270°	1 0	45°
0 1	225°	0 0	0°	0 1	225°
		0 1	90°	1 1	315°
		1 1	180°	1 0	45°
		1 0	270°	0 0	135°
1 1	315°	0 0	0°	1 1	315°
		0 1	90°	1 0	45°
		1 1	180°	0 0	135°
		1 0	270°	0 1	225°
1 0	45°	0 0	0°	1 0	45°
		0 1	90°	0 0	135°
		1 1	180°	0 1	225°
		1 0	270°	1 1	315°

Modulation Section

- **INPUT:**
- 11 11 01 11 00 11 00 01
- **OUTPUT:**
- 11 00 01 10 10 01 01 11

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The Logical Relation Equation

- **The modulation section**

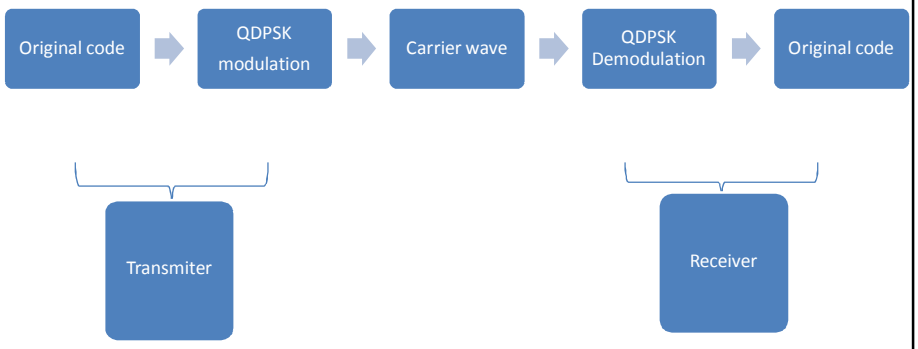
$$\begin{cases} c_n d_n = (a_n b_n) \overline{\oplus} (c_{n-1} d_{n-1}) & \text{when } (c_{n-1} d_{n-1} = 01 \text{ or } 10) \text{ AND } (a_n b_n = 01 \text{ or } 10) \\ c_n d_n = (a_n b_n) \oplus (c_{n-1} d_{n-1}) & \text{when others} \end{cases}$$

- **The de-modulation section**

$$\begin{cases} c_n d_n = (a_n b_n) \overline{\oplus} (c_{n-1} d_{n-1}) & \text{when } (c_{n-1} d_{n-1} = 01 \text{ or } 10) \text{ AND } (a_n b_n = 00 \text{ or } 11) \\ c_n d_n = (a_n b_n) \oplus (c_{n-1} d_{n-1}) & \text{when others} \end{cases}$$

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Signal Flow



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Implementation

Port	Item#	Item Value	Meaning
clk	Oscillator	50MHz	input
btn0	Button0	1, on	Default, no operation
		0, off	Confirm input
sw17	Switch17	0	input, modulation mode
		1	input, de-modulation mode
sw_v[0..15]	Switch0~Switch15	0	input, value 0
		1	input, value 1, first bit—switch 15
btn0	Button0	off	output, modulation mode
		on	output, de-modulation mode
led_v[0..15]	LED0~LED15	off	input, value 0
		on	input, value 1, first bit—LED 15

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Have A Try!

- **Input1: 11 11 01 11 00 11 00 01**
- **Output1:11 00 01 10 10 01 01 11**

- **Input2: 01 01 01 01 01 01 01 01**
- **Output2: 01 11 10 00 01 11 10 00**

- **Input3: ?**

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THANK YOU!