Final term presentation for Digital Signal Processing with FPGA's

CDMA transmitter and receiver implementation in FPGA

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Presentation plan

Chapter I: Presentation of the CDMA technology

Chapter II: Description of the implementation

Chapter III: Simulation and demonstration

CDMA

- CDMA: Code Division Multiple Access

- Multiplexage technique based on attribution of spreading codes to users

- New technology for high speed wireless networks

- Perfect reconstruction using Walsh cade used here mostly on the downlink

The CDMA Technology

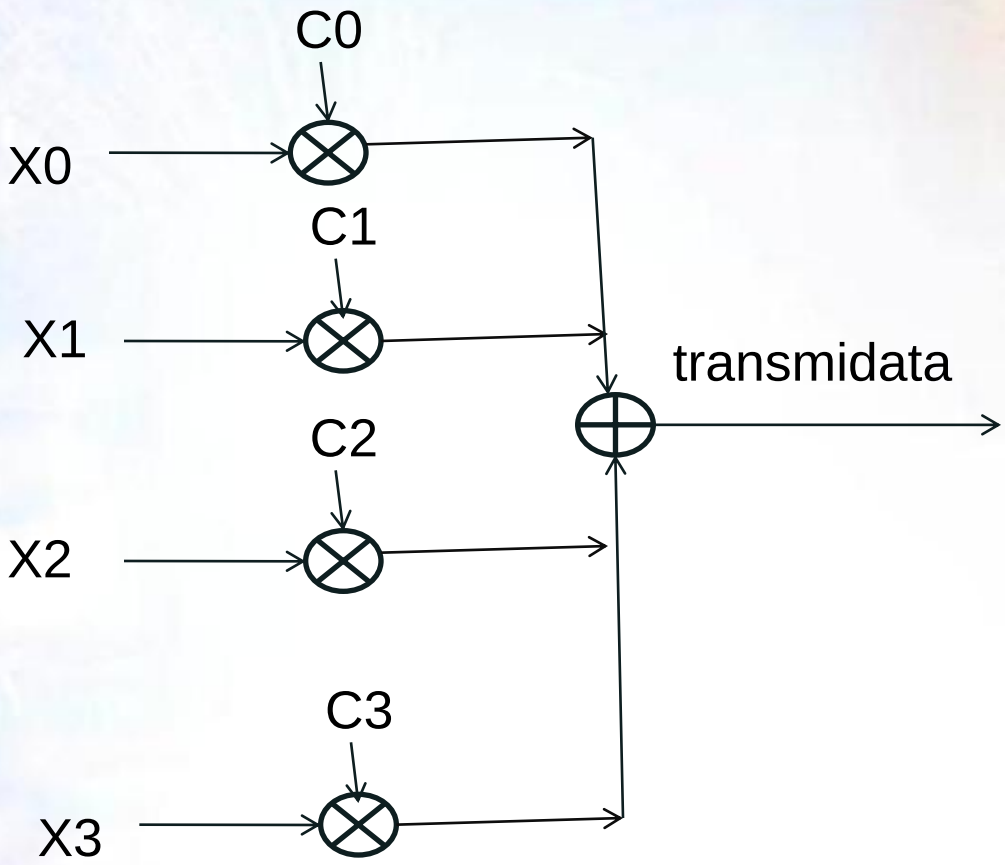
- **Orthogonal codes assigned to users for multiple access on all frequency**
- **Implementation for 4 users**
- **Perfect reconstruction with Walsh code**

Orthogonal Walsh codes

- Walsh codes for 4 users

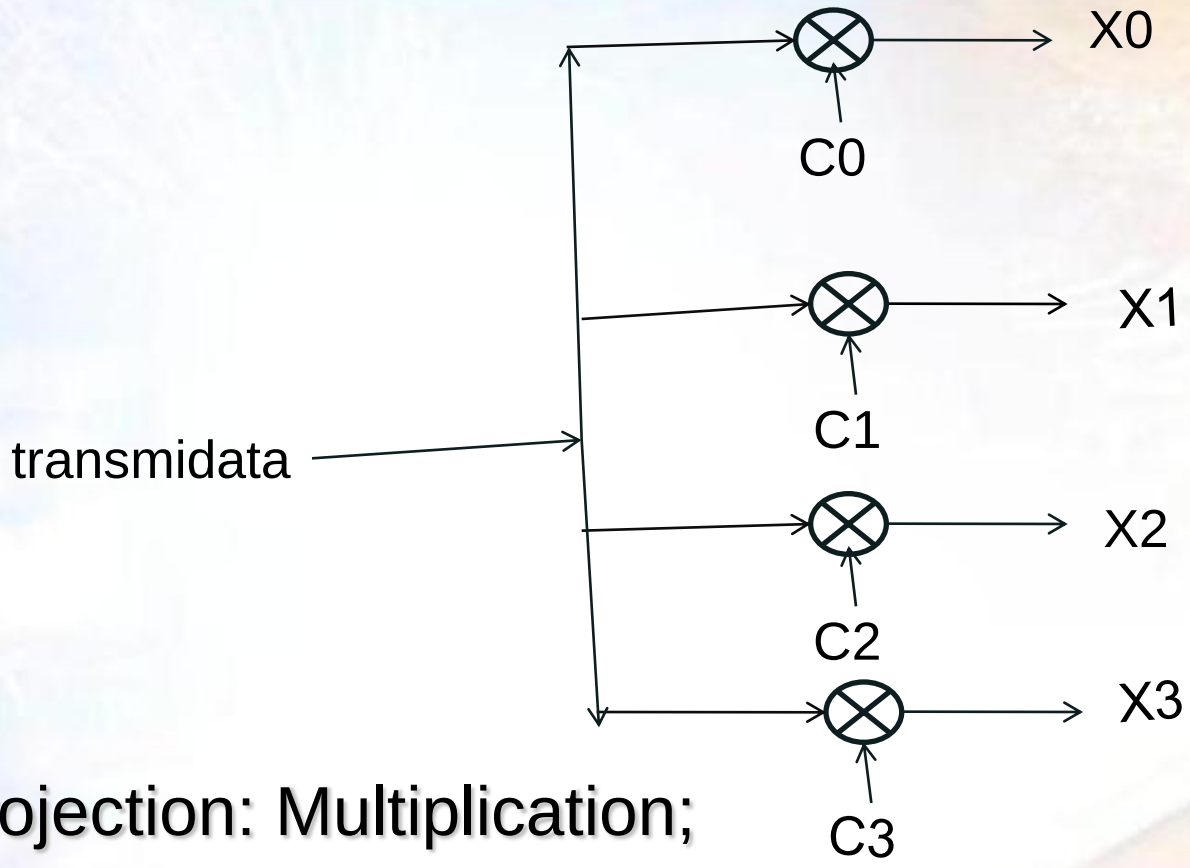
$$W(4) = \begin{bmatrix} 1 & 1 & 1 & 1 \\ 1 & -1 & 1 & -1 \\ 1 & 1 & -1 & -1 \\ 1 & -1 & -1 & 1 \end{bmatrix}$$

Modulation process



- Multiplication by vector

Demodulation process



- Projection: Multiplication;
- addition of vector coefficient
- Division by length of code

Description of design

- 4 bits data
- 8 bits codes
- Multiplication: 6bits
- Transmidata: 24 bits

$$W(4) = \begin{bmatrix} 01 & 01 & 01 & 01 \\ 01 & 11 & 01 & 11 \\ 01 & 01 & 11 & 11 \\ 01 & 11 & 11 & 01 \end{bmatrix}$$

Result

$$\begin{cases} x0 = 1 \\ x1 = -3 \\ x2 = 2 \\ x3 = 8 \end{cases}$$

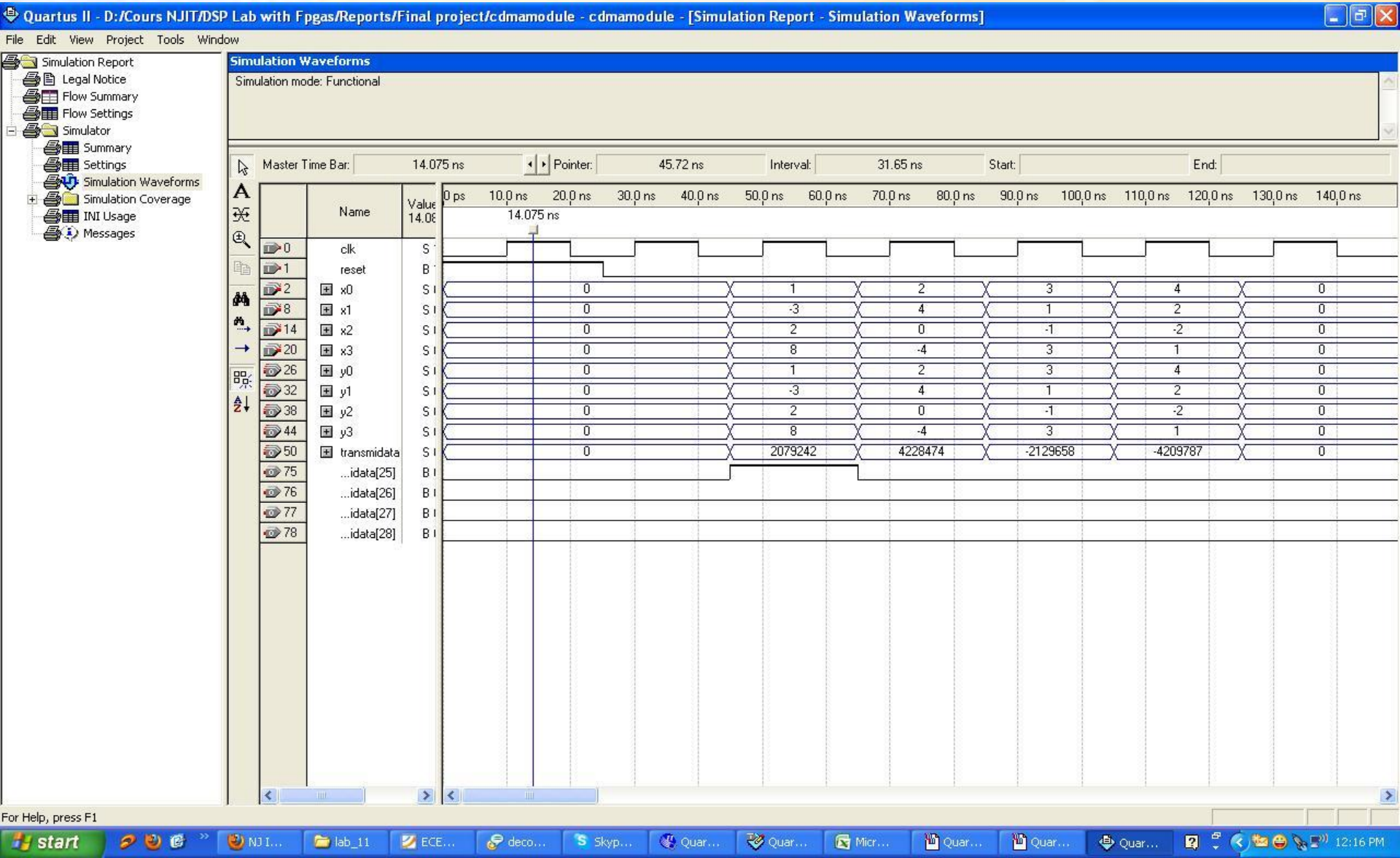
$$\begin{bmatrix} 1 & 1 & 1 & 1 \\ -3 & 3 & -3 & 3 \\ 2 & 2 & -2 & -2 \\ 8 & -8 & -8 & 8 \end{bmatrix}$$

$$8 \quad -2 \quad -12 \quad 10$$

Result

$$\left[\begin{array}{cccc} 8 & -2 & -12 & 10 \\ 8 & 2 & -12 & -10 \\ 8 & 2 & 12 & -10 \\ 8 & 2 & 12 & 10 \end{array}\right] \left| \begin{array}{l} x0 = \frac{4}{4} = 1 \\ x1 = \frac{-12}{4} = -3 \\ x2 = \frac{8}{4} = 2 \\ x3 = \frac{32}{4} = 8 \end{array}\right.$$

Simulation Result



Result

- Expected results got
- Perfect reconstruction of users' data
- High speed implementation in FPGA