# Quadrature Differential PSK Based on FPGA

ECE641 Term Project

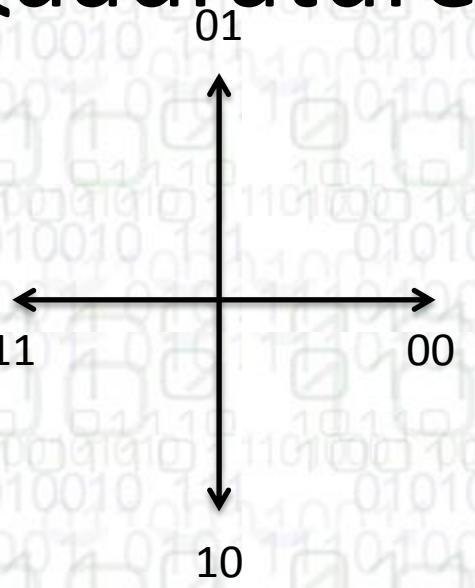
Instructor: Mustafa U. Torun

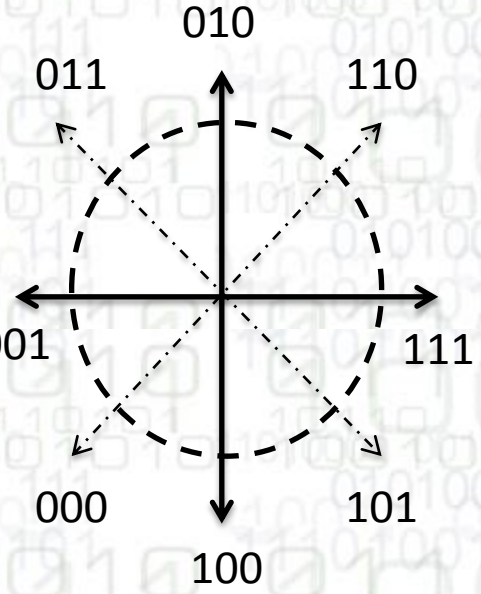
Qibin Zhu

31084690

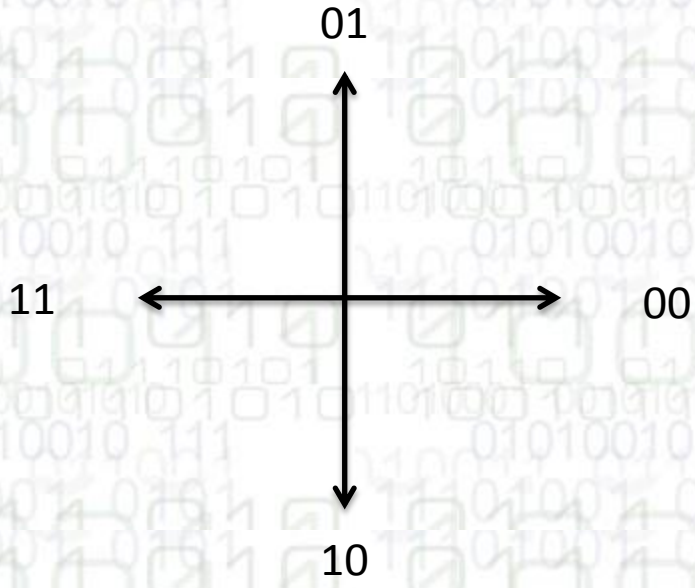
# Quadrature

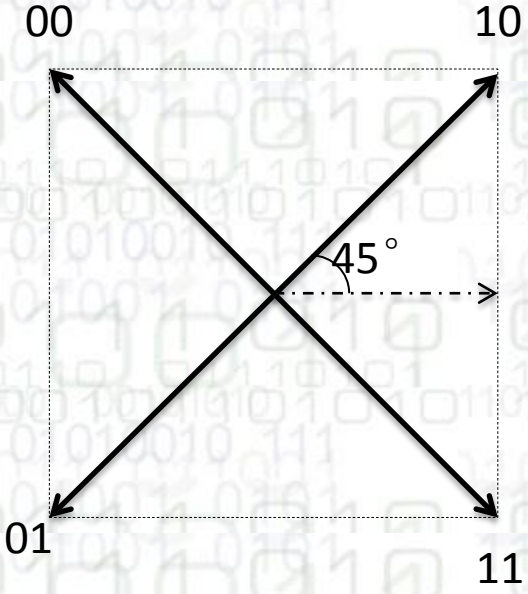


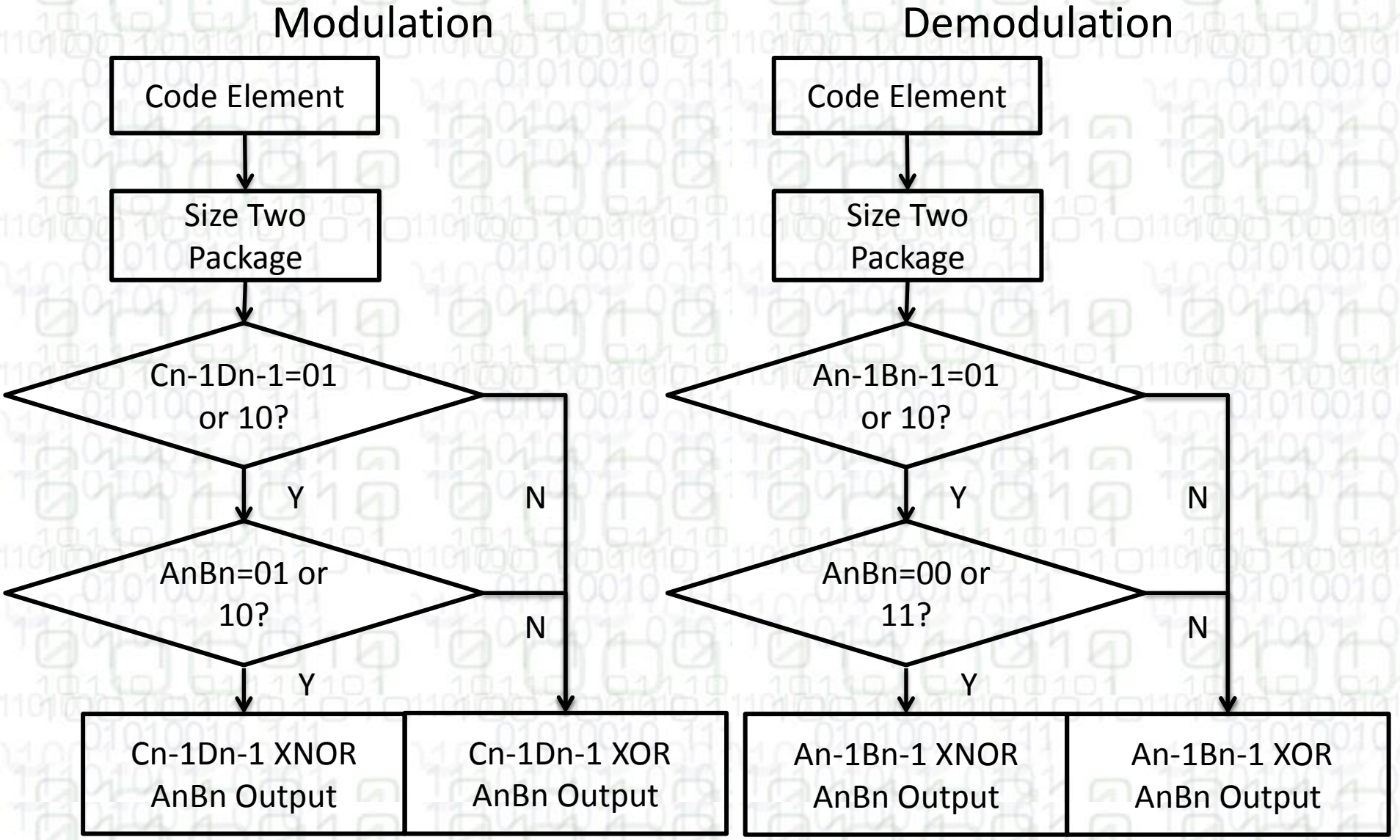




# Differential

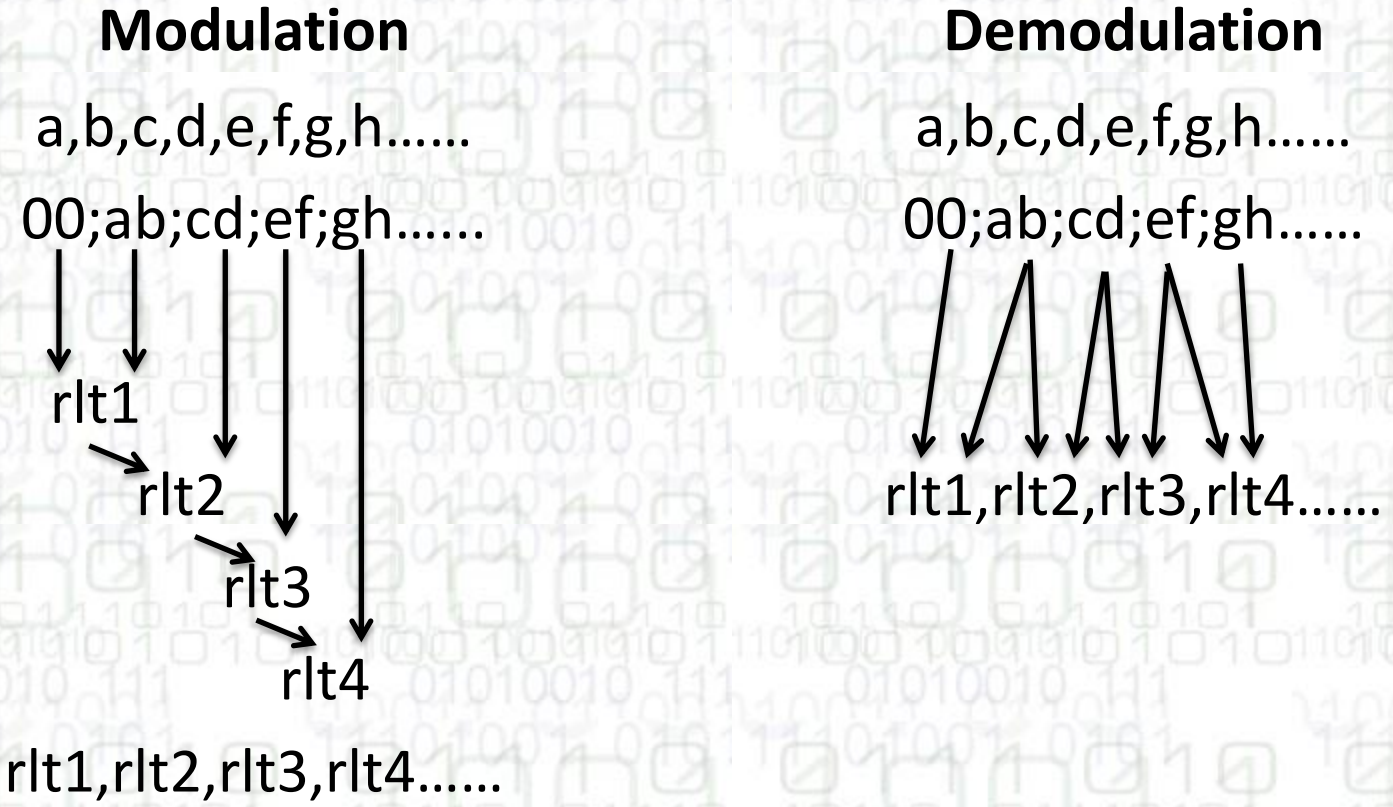


# Algorithm


Modulation
Code Element
Size Two Package
Cn-1Dn-1=01 or 10?
Y
N
AnBn=01 or 10?
N
Y
Cn-1Dn-1 XNOR AnBn Output
Cn-1Dn-1 XOR AnBn Output
Demodulation
Code Element
Size Two Package
An-1Bn-1=01 or 10?
Y
N
AnBn=00 or 11?
N
Y
An-1Bn-1 XNOR AnBn Output
An-1Bn-1 XOR AnBn Output

# Data Flow

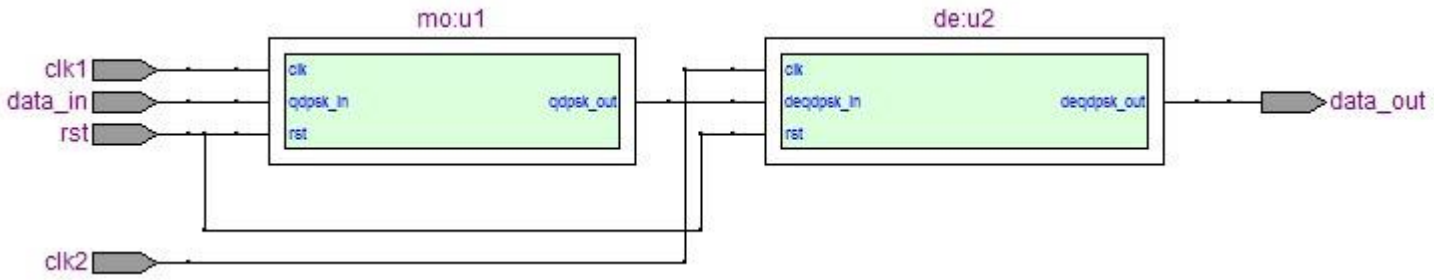

Modulation
a,b,c,d,e,f,g,h……
00;ab;cd;ef;gh……
rlt1
rlt2
rlt3
rlt4
rlt1,rlt2,rlt3,rlt4……
Demodulation
a,b,c,d,e,f,g,h……
00;ab;cd;ef;gh……
rlt1,rlt2,rlt3,rlt4……

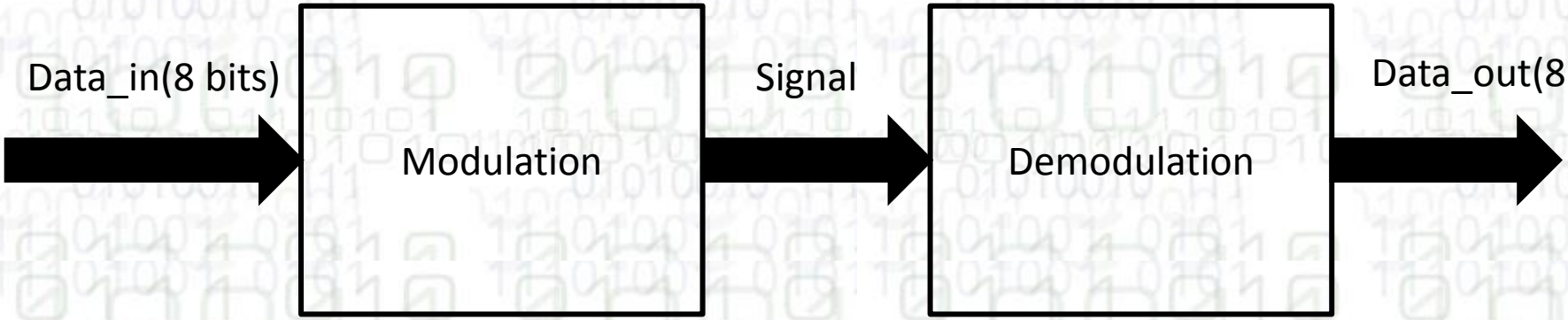
# Modulation VHDL

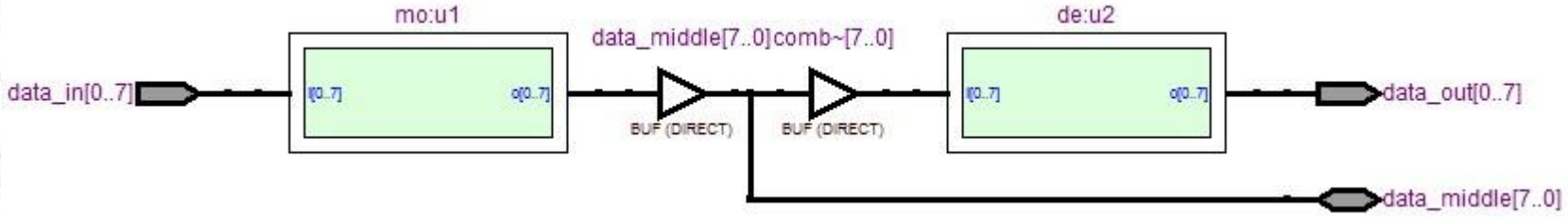
```
21  process(clk, rst, qdpsk_in)
22    begin
23      if rst='0' then
24        s    <= "00";
25        flag <= '0';
26      elsif qdpsk_in='0' or qdpsk_in='1' then
27        if clk'event and clk='1' then
28          s <= s(0) & qdpsk_in;
29          flag <= not flag;
30        end if;
31      end if;
32  end process;
33
34  process(flag, rst, s)
35    begin
36      if rst='0' then
37        fout <= "XX";
38      else
39        if flag'event and flag='0' then
40          if (fout(1) xor fout(0))='1' then
41            if (s(1) xor s(0))='1' then
42              fout(1) <= fout(1) xnor s(1);
43              fout(0) <= fout(0) xnor s(0);
44            else
45              fout(1) <= fout(1) xor s(1);
46              fout(0) <= fout(0) xor s(0);
47            end if;
48          else
49            if (fout(0)='X') or (fout(1)='X') then
50              fout(1) <= s(1);
51              fout(0) <= s(0);
52            else
53              fout(1) <= fout(1) xor s(1);
54              fout(0) <= fout(0) xor s(0);
55            end if;
56          end if;
57        end if;
58      end if;
59  end process;
```

```
60
61    process(clk, flag, fout)
62      begin
63        if clk'event and clk='1' then
64          if flag='0' then
65            qdpsk_out <= fout(1);
66          else
67            qdpsk_out <= fout(0);
68          end if;
69        end if;
70    end process;
71  end archi;
```

# Block Diagram



# Demo

| | |
|---|---|
| Data_in | SW17~SW10 |
| Signal (After Modulation) | LEDR7~LEDR0 |
| Data_out (After Demodulation) | LEDR17~LEDR10 |

Thank you!