ECE 758

Homework 06

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1. Introduction

In all given references for this homework a major conclusion can be made: for actual silicon technology, Moore's law is running out of room and new revolutionary technologies have to replace it. The 22 nanometer (22 nm) is the CMOS process step following 32 nm that is expected to be reached by semiconductor companies in the 2011–2012 timeframe. The industry acknowledges that it may be extremely hard to make features smaller than 22 nanometers using the lithography techniques that have improved for decades. It seems that the gap between transistor density and performance (Mega-instructions per second per watt) is increasing, showing our inability to use all chip transistors in an optimum way.

2. Future computing technologies

As first paper suggests [1], there are two paths to follow: *evolutionary* and *revolutionary*. First one refers on solutions applied to actual or near future silicon-based integrated circuit technology: parallel architectures (multiple cores, cloud computing, etc.) and power solutions (low power devices, new cooling technologies, etc.). The revolutionary path refers on finding alternative materials and designs like carbon nanotube transistors, graphene transistors, carbon nanotube memory devices, molecular electronics, spintronics, quantum-computing devices, magnetic memory devices, and optoelectronics. Also, a hybrid research path, which is more likely to produce results in near future, refers on combining CMOS technology with optical, molecular or quantum devices. These new materials could integrate with CMOS-based digital logic to produce hybrid systems.

Comparing with silicon, most of nanoscale devices have three main advantages: high speed, high density and low power. Of course, nothing comes for free. On the other side, researchers must address the main issue, i.e. **reliability**. For non-CMOS nanoscale electronics, operation uncertainties originate in the devices' inherent stochastic switching behavior. Also, devices will have more process variability—and thereby more nonuniform behavior across a chip. Therefore, designers will have to move from building deterministic circuits with predictable behavior containing deterministic base-building blocks to building deterministic circuits with high predictable behavior containing stochastic base-building blocks. In other words, building reliable computers from unreliable devices. Nanosystem reliability can be achieved by using temporal

redundancy (repeat computation, main disadvantage is the long delay), hardware redundancy (replicate hardware, main disadvantage is high area overhead), information redundancy (error-checking codes, hard to implement for general computations comparing with data transport) and hybrid solutions (HW + time, complicated control). Also, high defect and fault rates have to be considered as part of design considerations. In order to build reliable systems, there must be a tight synergy and well-designed interfaces between levels of technology abstraction.

Being the fact that nanodevices will work close to the thermal limit, researchers need to develop new computational models that take probabilistic implementation into account. The system itself and application that runs on it must be tolerant to hardware faults and incorrect operations. From architectural point of view, while the goal is to build reliable, cheaper, and high performance architectures from nano-electronic circuitry, it's not clear what aspects of current architectures will present the most serious constraints. There are few questions to answer: how the memory will be connected to the processing device in presence of high fault and defect rates; is it synchronous technique still cost effective or a globally asynchronous, locally synchronous (GALS) approach might be a better way? Today, the most demanding applications in terms of performance are multimedia, pattern-recognition and communication. For silicon technologies, there is a data flow bottleneck between sensing, memory and digital logic. Nonsilicon nanotechnologies provide opportunities to radically change the architectures employed for these applications in next generation integrated circuits. Integration of logic and memory will allow large-scale array computing with increased local storage. The availability of extensive local storage, fully integrated with logic, could offer new capabilities and increased performance for applications currently limited by the logic-memory communication overhead. Also, hybrid architectures might allow for integration of sensing with logic and memory. Applications that might benefit are vision systems and speech recognition. Therefore, nanotechnology will provide a high level of integration of sensing with memory and logic functions.

Nanoelectronics will add new challenges. Nanoscale provides trillions of devices per square centimeter and offers increased carrier mobility and reduced power per switching. New techniques for assembling efficiently, reliable and cost-effective of these devices have to be developed. Nanoscale devices will operate stochastically and require postfabrication correction. Thus these circuits are going to have hardware built-in fault detection and correction. Gates are

going to have small gain and low fan-out which implies additional hardware for level restoration. Citing from [1], "*the key challenge is how to build reliable systems from imperfect devices*".

Challenges in designing nanoelectronics can be classified into several domains: device characterization; simulation, design, and optimization; and system integration at the terascale. Current CAD tools can't scale to handle systems with tens of billions of components or more. Even today we cannot simulate in HSpice an entire state of the art microprocessor. Fortunately is not necessary to do that. However, future CAD tools have to take in consideration, as part of design constraints, the high level of defects and faults, noise, and resistivity of nanodevices. For CAD tools there are several issues to address:

- *Models*; the conventional methods for modeling devices for use in circuit simulation are built on deterministic models. Nanomodels should be based quantum physics and probably will be stochastic .
- *Logic Primitives*; Traditional logic primitives, i.e. sum-of-product or product-of-sums functions, have to be replaced by new logic primitives —for example, threshold, majority, and minority functions.
- *Circuit fabrics*; Nanodevices will likely be built in regular arrays of nanoblocks, each consisting of many locally connected nanodevices. Hybrid CMOS and nanodevices will probably be one solution. Crossbar-based circuit is one example.
- *Defects*; Researches must develop defects and fault models that accurately capture most behavioral effects these defects produce. Also, they have to develop tools for locating defects at a sufficient level of granularity on a manufactured nanocircuit fabric.
- *Design tools*; New tools must be suitable for the nanotechnology fabrication process and address the unique features of nanotechnology devices and fabrics.
- *Design flow*; Future nano-industry must address design and verification problems having to do with observability and controllability of the nanoblocks, dynamic reconfiguration of nanoblocks, and hybrid (silicon and nanodevices) and hierarchical circuit architectures.

Second paper [2] is an introductory paper to an ACM special section dedicated to non-silicon computing technologies. The paper classifies the articles in two subsections. First subsection refers to nanoscale technologies: the areas covered include computing schemes based on nanowires, carbon nanotubes, organic molecules, bio-DNA, and quantum physics. Second

subsection contains articles on special forms of computing including optical, micro/nanofluidic, and amoebabased chaotic.

Atomic and molecular computing refers to technologies where the switching element is on the order of around 10 nanometers on a side. Thus, the circuits can have a local density of one trillion of elements per square centimeter. These elements serve as memory or logic circuits and the major challenge is how to perform stable (reliable, predictable) computing using these so called “crummy” elements.

Carbon nanotubes with nanometer-sized diameter provide speeds in pico-second range and less electron scattering. Basic logic gates and memory cells have been constructed but integration of them in more complex digital circuits hasn’t been done yet.

Computing based on *organic and other types of molecules* is another research field. Techniques based on bulk materials such as polymers have already been commercialized. Main advantages are high density of logic elements, cost reduction and higher bio-compatibility when compared to silicon.

DNA (RNA) computing is the technique in which information encoded on DNA is used to perform biomolecular processes to achieve targeted computing. Advantages are scalability, self-assembly capability and massively parallel processing capabilities. Main disadvantage is the fact that computing is slow, on the order of tens of milliseconds to minutes.

Quantum computing is based on quantum physics. In a quantum computer, each quantum bit , called qubit, can be 0, 1, or a superposition of states 0 and 1 at the same time. Since the computation performance is tremendous comparing with actual supercomputers, quantum computing can be applied to some difficult problems like cryptography, search, and number theory. Quantum computing will be discussed in detail in the last part of homework.

A special form of computing is *optical computing* which uses light as carrier for digital information. Despite his huge potential (digital levels travel with speed of light) there are some technical difficulties to build complex logic circuits due to the fact that controlling light is much more difficult. Even that making optical switches is a daunting challenge, progress has been made by developing optical interconnect between traditional silicon processors on multicore chips. Therefore, in near future, a hybrid solution (silicon and optical devices) will initially be used to enhance the overall speed of actual systems, mainly in communication between different

on-chip parts. Completely optical computing chips will require some fundamental breakthroughs, however.

Other exotic technologies used for computation are *micro*/*nanofluids* and *amoeba*. Main disadvantage is given by the low speed of the devices.

Third paper [3] presents some computing technologies or solutions that may have impact in near or far future. There are few which already are in production or development phase: parallel architectures, nanowires, and cooling techniques; and other solutions that still are in (pre)research phase: nanotubes, graphene, optical, molecular, quantum, and DNA computing.

One of the solutions to boost computing performance is to use *nanowires* for building a crossbar. Instead of fabricating transistors all in one plane, the crossbar approach has a set of parallel nanowires in one plane that crosses over a second set of wires at right angles to it. The many intersections that exist between the two sets of wires can act like switches, called *memristors*, that represent 1s and 0s like transistors do. This technique can also be used in designing reconfigurable logic to replace the present FPGA technology.

Another solution, developed by IBM, is to replace the silicon substrate by *carbon nanotubes* in CMOS technology. They even build a ring oscillator circuit on a single carbon nanotube that connects circuit elements.

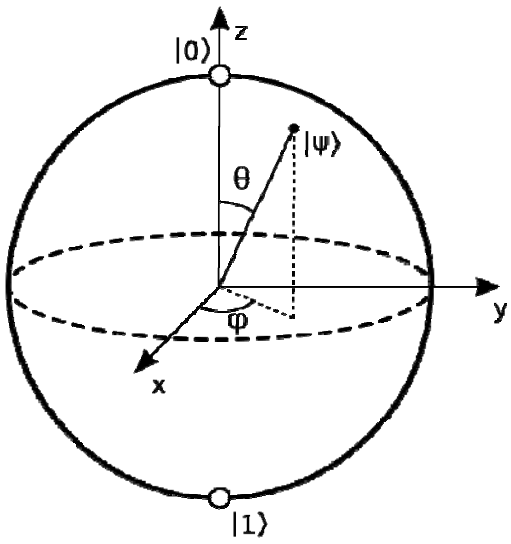
A nonsilicon material, *graphene,* is a flat sheet of repeating hexagons which conducts electrons faster than any other material at room temperature. The graphene transistors can have 10 nm across and height of one atom. In such transistor only a single electron has to move from source to drain for switching between 1 and 0. Of course, the power consumption will be very low but on the other side designing a reliable circuit will become a big challenge.

3. Quantum Computing

Logic devices made from individual atoms, photons or electrons is the ultimate goal of computing researchers (is it true??). At this dimension, laws of quantum mechanics explain the behavior of these particles. Quantum computers will have higher logic density and speed than any other imagined technology. However, building such a computer is a daunting challenge.

Atomic particles can exist in different states which can be represented by a quantum bit. Comparing with classical approach where a bit is 0 or 1, a quantum bit can have more than two

values. One approach, called spintronics, uses electrons, whose magnetic moments spin in one of two directions represents 1 or 0 states. The two states can also coexist in a single electron, however, creating a unique quantum state known as a superposition of 0 and 1 (called also "entangled"). In figure (*taken from Wikipedia*), $|\psi\rangle = \alpha|0\rangle + \beta|1\rangle$ is the state of qubit and α and β are probability amplitudes which in general both can be complex numbers.



Currently, numerous implementations are experimented: trapped ions, trapped neutral atoms, superconducting circuits, photons, and quantum dots.

Even if in the early years of quantum research quantum computation was theoretically impossible, some events in 90s changed that perception. These are: the development by Peter Shor of a quantum algorithm for efficiently factoring and computing discrete log in '94, the first experimental two-qubit gate in ion traps in '95 and the proof that quantum error correction is possible. Despite the impossibility of cloning and the continuous representation of quantum information, it was proven that quantum error-correcting codes exist and are effective in protecting quantum data from the effects of quantum noise. Instead of computing data in his primary form, quantum systems have to compute the information encoded into quantum error-correction codes. Citing from [4] "The threshold theorem states that if the rate of noise on a quantum computer is small enough, and the control over the quantum computer is precise enough, then one can simulate a quantum algorithm with a desired failure rate using an overhead that scales only polylogarithmically with the inverse of the failure rate." This means that the model of quantum computation can be analog with the model of classical computation thus, allowing to build quantum computers. Presently there are some successes in building a quantum computer like ion-trap quantum computers with up to eight qubits (qubyte) and Nuclear Magnetic Resonance (NMR) quantum computation with up to 12 qubits. Also, state-of-the- art experiments have demonstrated unconditionally secure key distribution up to a distance of approximately 100km using quantum information.

Despite these successes, my opinion is that we cannot talk about the fact that first quantum transistor was invented yet. There are still a lot of theoretical and experimental challenges to face until the first quantum gate will actually become the *building block* of a more complex quantum circuit. It took around seventy years from the first ever built transistor to a 22 nm CMOS processor, and probably, it will take more than a century from now to build a reliable and complex quantum system. To build fault-tolerant quantum computers is not an easy task. To observe, measure and control quantum particles is not presently easy; the complete state may not be measured precisely, so verification is difficult; as an analogy quantum-silicon, actual research doesn't have the tools (technology and knowledge) to measure and drive current in the first Shockley transistor.

However, building such a computer will raise other issues like developing quantum programs (quantum algorithms) which will solve problems that we barely imagine today (for example expansion of the universe, nuclear reactions at solar scale, solar system simulation, etc.).

In the near future the successful devices are going to have hybrid components like silicon-nanowires (nanotubes), silicon-optical and/or silicon-molecular. Also, we cannot say that we reached the point where all the transistors from actual chips are used in an optimal way. Therefore, it is still a lot of work to do in the actual design flow. Probably the bottlenecks in current silicon circuits will be replaced by new technologies; thus, silicon will be part of our life for at least a century.

4. References

[1] R. I. Bahar, D. Hammerstrom, J. Harlow, W. H. Joyner Jr., C. Lau, D. Marculescu, A. Orailoglu and M. Pedram, Architectures for Silicon Nanoelectronics and Beyond, Computer, vol. 40, no. 1, pp. 25-33, January 2007.

[2] T. Munakata, Beyond Silicon: New Computing Paradigms, Comm. ACM, vol. 50, no. 9, pp. 30-34, Sept. 2007.

[3] The Next 20 Years of Microchips, Scientific American, January 2010.

[4] D. Bacon and D. Leung, Toward a World with Quantum Computers, Comm. ACM, vol. 50, no. 9, pp. 55-59, Sept. 2007.