ECE 758 VLSI Design – II Homework-XV

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Due Date: Thursday, April 8, 2010

No collaboration is permitted in this homework. Your work must be your own. This rule is strictly followed. Submit a good report.

1. No complex system or circuit can be designed simply by interconnecting gates one at a time. In order to deal with such circuit complexity, a "divide and conquer" approach is used. For design, the circuit is broken up into pieces we call blocks. the blocks are interconnected to form the circuit. The functions of the blocks and the interfaces between them are carefully defined. This design approach is referred to as hierarchical design.

    (a) Write VHDL code to implement an 8-bit Ripple Carry Adder. Use three entities to build a hierarchical description. The three entities are a (i) half-adder, (ii) full adder that uses half adders, (iii) and the 8-bit adder (that utilizes the full adder). The architecture of the half-adder should consist of data-flow assignments. The architecture of the full-adder should use the half-adder as a component (i.e., structural). The architecture of the 8-bit adder should use the full-adder as a component (i.e., structural).

    (b) Report the number of gates/devices/resources utilized by the architecture from the synthesis results.

2. A serial two's complementer is to be designed. A binary integer of arbitrary length is presented to the serial two's complementer least significant bit first on input X. When a given bit is presented on input X, the corresponding output bit is to appear during the same clock cycle on output Z. To indicate that a sequence is complete and that the circuit is to be initialized to receive another sequence, input Y becomes 1 for one clock cycle. Otherwise, Y is 0.

    (a) Find the state diagram for the serial two's complementer.

    (b) Find the state table for the serial two's complementer.

    (c) Write a VHDL description (using processes) for the circuit specified. Use the D-flipflop (VHDL) as a component.

    (d) Do the synthesis of your model.

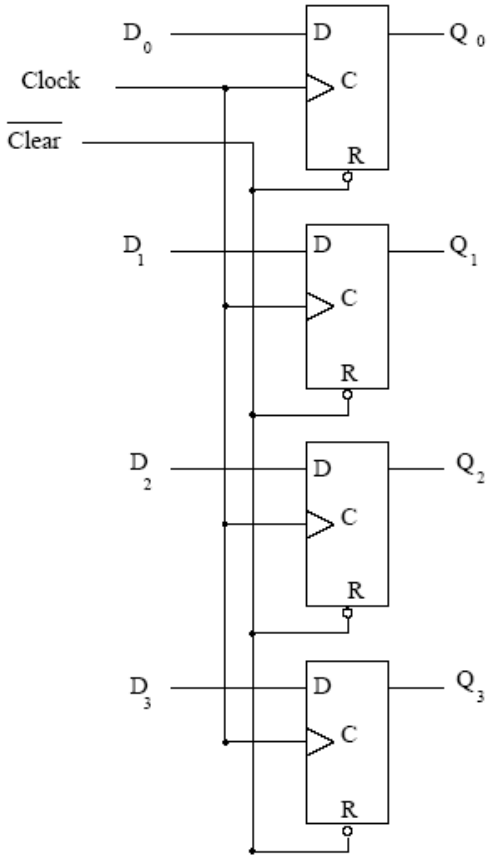


Figure 1: 4-Bit Register

3. The simplest register is a register that consists of only flip-flops without external gates. Figure 1 shows such a register constructed with four D-type flip-flops. The common Clock input triggers all flip-flops on the rising edge of each pulse, and the binary data available at the four D inputs are transferred into the 4-bit register. The four Q outputs can be sampled to obtain the binary information stored in the register. The $\overline{\text{Clear}}$ input goes to the $\overline{\text{R}}$ inputs of all four flip-flops and is useful for clearing the register to all 0's prior to its clocked operation.

   (a) Write a behavioral VHDL description for the 4-bit register. Compile and simulate your description to demonstrate correctness.
   (b) Write a structural VHDL description for the 4-bit register using D flip-flops as components. Compile and simulate your description to demonstrate correctness.

4. The algorithmic state machine (ASM) chart for a synchronous circuit with clock CLK for a washing machine is to be developed. The circuit has three external inputs **START, FULL,** and **EMPTY** (which are "1" for at most a single clock cycle and

mutually exclusive), and external outputs, HOT, COLD, DRAIN and TURN. The data-path for the control consists of a down counter which has three inputs RESET, DEC, and LOAD. This counter synchronously decrements once each minute for DEC = 1, but can be loaded or synchronously reset on any cycle of clock CLK. It has a single output ZERO which is 1 whenever the counter contains value zero and is 0 otherwise.

The circuit is to operate as follows. It goes through four distinct cycles, WASH, SPIN, RINSE, and SPIN which are detailed as follows:

WASH: Assume that the circuit is in its power up state IDLE. If START is 1 for a clock cycle, HOT become 1 and remains 1 until **FULL = 1**, filling the washer with hot water. Next, using LOAD, the down counter is loaded with a value from a panel dial which indicates how many minutes the wash cycle is to last. DEC and TURN then become 1 and the washer washes its contents. When ZERO becomes 1, the wash is complete, and TURN and DEC become 0.

SPIN: Next, DRAIN becomes 1, draining the wash water. When EMPTY becomes 1, the down counter is loaded with the value 7. DEC and TURN then becomes 1 and the remaining wash water is wrung from the contents. When ZERO becomes 1, DRAIN, DEC, and TURN return to 0.

RINSE: Next, COLD become 1 and remains 1 until FULL=1, filling the washer with cold rinse water. Next, using LOAD, the down counter is loaded with value 10. DEC and TURN then become 1 and the washer rinses its contents. When ZERO becomes 1, the rinse is complete, and TURN and DEC become 0.

SPIN: Next, DRAIN becomes 1, draining the rinse water. When EMPTY becomes 1, the down counter is loaded with 8. DEC and TURN then becomes 1 and the remaining rinse water is wrung from the contents. When ZERO becomes 1, DRAIN, DEC, and TURN return to 0 and the circuit returns to state IDLE.

(a) Find the ASM chart for the washer circuit.

(b) Implement the ASM chart by using either a “one flip-flop per state” or a “sequence register and decoder".

(c) Perform the design using VHDL instead of an ASM chart. Include the counter in the VHDL. Compile and simulate your design by running the washer through a cycle. Adjust the clock intervals if necessary to avoid long simulation times.

(d) Report the number of gates/resources utilized by the architecture from the synthesis results.

(e) Define a test bench model to test your model.