ECE 758 (SP'10) Homework-III-A Due Date: February 11, 2010

No collaboration is permitted in this homework. Your work must be your own. This rule is strictly followed.
Extra credit for showing independent work

Model a 16-bit adder circuit in two different ways i.e. (i) algorithmic and (ii) dataflow models. Synthesize the two 16-bit adder circuits with 0.18µ and 0.35µ CMOS technologies using Mentor Graphics tools. Implement the circuits two ways by synthesizing for minimum area (area optimization) and for minimum delay (delay optimization).

Find its critical path delay. You can use any tool including static timing analysis tool (it may not be in the tutorials) to estimate the timing. Compare timings using HSPICE simulation.

Tabulate number of gates, estimates of area, delay and power consumption.

Provide a summary outlining the benefits of technology scaling and optimization principles.