Steps for making the layout using Silicon Ensemble and Cadence using your verilog file generated from Ambit Buildgates

1. From your pwd go to ece658 directory (not ece758)
2. Open the cds.lib file in any word editor and add this line

DEFINE wcells /afs/cad/solaris/cadence2002/ic446/vendor_libs/tsmc/cmosp35.3.0/dfII_lib/wcells

This definition adds the path for standard library cells. Save this file. Make sure that you have exactly the same file in your cadence_tech directory also.

3. Open Silicon Ensemble by typing cadence at ece658 prompt and select the option 4.
4. Once you see the window – you have to upload the following files one-by-one.
    a. File - > Import - > LEF . Select the LEF file that you have downloaded from the website. Once importing is complete you have to check the display below saying that the database has been created successfully.
    b. Now you can see that the other options are highlighted in the Import window. Now select File -> Import -> Timing Library. Select the GCF file that you have downloaded from the website. Open the GCF file in any text edition and make sure that the path inside the timing library *.gcf is correctly given. If not, update your gcf file and save the changes.
    c. Once this complete you will have to see in the display window that the database has been updated successfully without any errors. Ignore any warnings, if there are.
    d. Once this is done import your verilog file using File - > Import -> Verilog. Once this done a screen window appears. You have to select the post-synthesised verilog file along with other required standard *.v files required for your project.
    e. Make sure that you give the name of the verilog top module as you see in your post synthesised verilog file.
    f. The compile verilog reference libraries will now show all the libraries present in the directory. Delete them all and include only the following two libraries with a space between them. wcells cds_vbin
    g. Let the compiled verilogy output library be cds_vbin.
    h. Once this done change all the displayed vdd! To VDD! And gnd! To VSS! And press OK.
    i. Make sure that the final command says the completed importing verilog.

5. Click on FLOORPLAN – INITIALISE FLOORPLAN. Change Left/Right IO to Core distance to 40.0 microns . Change Top/Bottom IO to core distance to 40.0 microns. Click on flip Every other row and Abut Rows. Click on OK.
6. Click on ROUTE – PLAN POWER – ADD RINGS. Change CORE RIGHT WIDTH for Horizontal metal1 to 0.9 microns. Change Core Ring width for Vertical metal2 to 0.9 microns. Click on OK.
7. If you get an error Cannot create rings… because of not space go to Floorplan.. Resize floorplan – horizontal 100%. Repeat this for Floorplan – Resize floorplan - Vertical 100%. This increases your layout module area.
8. Click on Place – Ios – OK to place the inputs and outputs.
9. Click Place – Cells –OK to place the required standard cells. If you get the message Impossible to Place cells without overlaps, then you need to resize the floorplan to increase the available area.
10. Click on Route – Route Power –Follow pins changing the primary Metal1 width in the form to 0.9 Click OK.
11. Click on Route – Wroute – OK to finish the final detailed routing.
12. Once this done export them as DEF file and save it in the same ece658 directory. In the option form give the file name for the .def file.
13. Exit the tool from the File menu.

14. Now open the DEF file in any text editor and replace the text VIAGEN21 by M2_M1 and save them.
15. Open your cadence Virtuoso and create a new cell library. Once you make a new cell library make a new cell view of the file and view name as autorouted and the select Virtuoso as your tool.Make sure that the cell name matches your DEF filename.
16. Go to your icfb window and select File - >Import -> DEF . A window appears and give the library name and cell view name as you have created earlier. Do not select Reference libraries and press OK.
17. Once this done go back to your icfb window and open your cell view under autorouted.
18. You can see the design with the standard instances of the cells. At the same time you can see a different set of tools on your left side. Now go to the main menu and select Tools -> layout and you get your LSW window virtuoso layout tools.
19. In the Edit -> Search menu, change the search for blank to inst in current cellView. Click on Add Criteria and change the first blank to view name = = abstract. Change the bottom line to Replace View name - > layout. Click on Apply and Replace all. You should now have a layout cell with your standard cell logic, such that you can place this cell in a manually-created design. Use Hierarchy - > Flatten cells option to see the layout cells drawn for you !!.
20. Follow the rest of the steps as you normally do for your cadence.