By Jing Kong

COMPUTATION WITH CARBON NANOTUBE DEVICES

The remarkable properties of carbon nanotubes make them very promising candidates for future computing elements—both as a successor for silicon-based technology and beyond.

A single-walled carbon nanotube (SWNT) can be viewed as a sheet of graphite (a hexagonal lattice of carbon) rolled into a cylinder that is typically a few nanometers in diameter and many micrometers in length. Depending on the roll-up direction (their geometric configurations), SWNTs can have different electronic properties. Each geometric structure can be described by a circumferential vector of two integer components (n, m) (see Figure 1). A nanotube can change from a metal or semimetal to a semiconductor with n or m changes only by 1: The tubes are metallic for $n = m$; semimetallic for $n - m = 3j$ where j is a non-zero integer; and semiconducting for all others with $n - m = 3j \pm 1$ where j is an integer. As a result, one-third of the SWNTs are metallic or semimetallic and two-thirds are semiconducting with a direct bandgap of approximately one electron volt.

There have been two main approaches for using carbon nanotubes to perform logic functions. The first one is to use semiconducting SWNTs to replace the silicon (Si) channel of metal-oxide-semiconductor field-effect transistor (MOSFET) devices. SWNTs have many advantages in this regard: they have less electron scattering, higher thermal conductivity, and more robust, chemically inert structures. The earliest SWNT FETs were built in 1998 [7, 9]. In the following years, performance improvements have continuously been made. At present, individual SWNT transistors demonstrate one to two orders of magnitude higher mobilities than state-of-the-art Si MOSFETs [5, 6] and faster switching

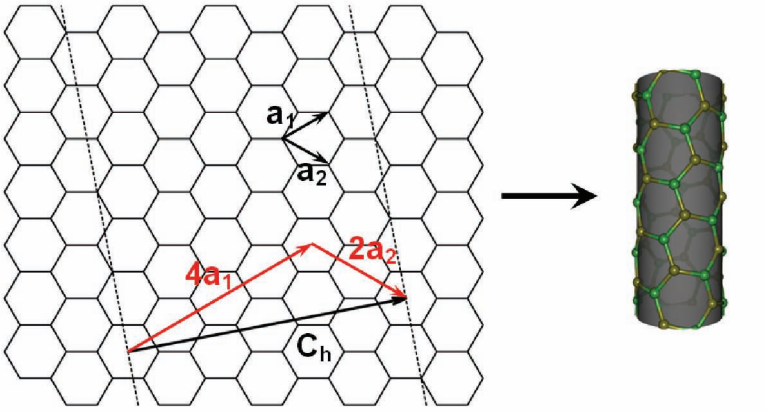


Figure 1. The construction of a SWNT by rolling up a strip of graphite layer. In this example an (*n*, *m*) = (4, 2) nanotube is generated and the resulting tube is shown on the right.

speed (lower subthreshold swing) [1, 2]. Both p-type and n-type transistors have been demonstrated, which is desirable for CMOS technology. This approach does not take advantage of their small sizes, and the channel lengths of the SWNT FETs are still limited by lithography. It is expected, however, that SWNTs will provide superior performance at about the same length as their scaled silicon counterparts.

The biggest challenge of this approach lies in the large-scale fabrication of SWNT devices. This will require having identical SWNTs at desired locations and with determined orientations on the substrates, which has been one of the most difficult problems in nanotube research. As a result, until now only primitive logic circuits with nanotube FETs were constructed, including NOT, NOR, OR, NAND, AND gates and memory cells. More recently, a five-stage ring oscillator fabricated on a single nanotube was demonstrated [3]. Oscillation frequency of up to ~70MHz was achieved, which is five to six orders of magnitude greater frequency response than ring oscillators built by off-chip external wiring of the individual devices. As SWNTs can now be synthesized up to centimeter length on Si substrates [10], constructing more complicated circuits on a single SWNT can be expected in the near future. The ultimate realization of carbon nanotube computer circuits will rely on technology breakthroughs in nanotube synthesis and integration.

The second approach proposes to build nanoelectromechanical switches using carbon nanotubes to perform logic functions. An example concept is illustrated in Figure 2 [8]. These reversible, bi-stable device elements could be used to construct nonvolatile random access memory and logic function tables. Since this approach can fully exploit the advantage of the small sizes of nanotubes, depending on the design, a device density of up to 10^{12} per square centimeter can be anticipated. The switching speeds of these devices are determined by mechanical bending, thus operation frequencies can be higher than 100GHz. In addition, the small sizes are likely to give rise to small device capacitances (depending on

the design), the dynamic power consumption can be lower than the conventional CMOS circuits.

Following this idea, individual switches employing multi-walled carbon nanotubes (concentric tubes of multiple graphite layers) have been demonstrated [4]. Similar to the first approach, large-scale fabrication has been the biggest challenge. A simpler approach has been implemented by Nantero, Inc., using thin films of SWNTs to develop memory devices, where a "mat" of suspended SWNTs can be switched "up" and "down" by electrostatic forces. These memory devices are termed nanotube-based/nonvolatile random access memory (NRAM). The NRAM is intended to be a universal memory chip that can replace DRAM, SRAM, flash memory, and ultimately hard disk storage. To date, arrays of 10 billion suspended nanotube junctions on a single silicon wafer have been demonstrated with switching lifetimes over 50 million cycles. The current operating voltages are below 5V and the switching times are below 3ns. Nantero is also developing nanoelectromechanical switches that can function as logic devices for fast, radiation-tolerant logic circuits that are scalable to 65nm and below. If successful, this will become the most immediate application of SWNTs for computation.

Metallic SWNTs have been considered as the replacement for the copper interconnects in integrated circuits. As interconnect feature sizes shrink, copper resistivity increases due to surface and grain boundary scatterings. The superior electrical conduction in SWNTs provides a natural solution. In addition, the current carrying capability of a SWNT is more than three orders of magnitude larger than that of copper (10^9 A/cm^2 vs. 10^6 A/cm^2). These excellent mechanical properties also allow nanotubes as a much sturdy interconnect material, which can easily handle the electro-migration that plagues copper interconnects. Research efforts are currently very active in this field.

The scope that SWNTs contribute to computation, however, is not just limited to the aforementioned areas. Quantum computation has been proposed to solve a series of problems that cannot be addressed even by today's fastest supercomputers. Carbon nanotubes represent one of the model solid-state systems to realize an elementary quantum computer. The spin of a single electron confined in a nanotube quantum dot is used as a quantum bit (qbit), which is the building block of a quantum computer. Compared with other solid-state systems for quantum computation, the spin relaxation time in a carbon nanotube quantum dot could be much longer due to the least spin-orbit coupling in carbon system, which is very advantageous. Currently, spin relaxation and interactions of spin in multiple nanotube quantum dots are areas awaiting further investigation.

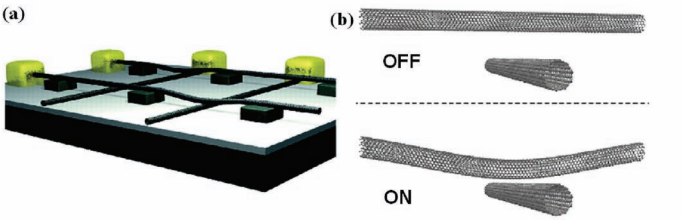


Figure 2. Concept of Nantero's nonvolatile memory device (adapted with permission from [8]).

In this article, a brief overview of the various aspects of nanotube devices for future computation is provided. Some prototypes are being commercialized whereas the rest are still under intensive research development. A key issue involves large-scale integration and the ability to synthesize nanotubes of a uniform type (semiconducting vs. metallic). These are very challenging issues, however, given that a tremendous amount of efforts are being devoted to nanotube research currently, it is probably a matter of time before nanotube circuits and interconnects are integrated into future computer chips. C

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