Extraction of Parasitic Capacitance and Resistances for HSPICE Simulation

Make the layout window active and select Calibre > Run PEX from the top menu bar to start a Parasitic EXtraction. You will need to fill in a few screens to properly initialize Calibre. The Calibre setup information can be saved so you only need to enter it once. The Calibre extraction tool reads in your layout file and creates a Spice netlist suitable for simulation.

Calibre PEX window should pop up along with Load Runset File window.

	Calibre Interactive - PEX	
Eile Transcript Setup		Help
Bules PEX Rules Jnputs Indes Qutputs PEX Run D Transcript .	File	View Load
Run <u>P</u> EX Start RVE	Load Runset File Runset File Path Recent Runsets Path OK	

Calibre saves all the information of the extraction in a runset file. As we have never saved any runset files before, click cancel.

Rules

Click on the Rules tab in the left, and then on the button with the '...' to choose the rules for the extraction. Browse and choose the file /afs/cad.njit.edu/solaris/mentor.2007/adk3_1/technology/ic/process/tsmc035.ca libre.rules.

	Calibre Interactive - PEX	- 66
Elle Iranscript	: <u>S</u> etup	<u>H</u> elp
Rules	PEX Rules File	
Inputs	//////////////////////////////////////	Load
Outputs		
Run <u>C</u> ontrol	PEX Run Directory	
Tr <u>a</u> nscript	/afs/cad.njit.edu/u/s/a/sam45/ECE658/HW5	
Run <u>P</u> EX Start R⊻F		

Choose a PEX Run Directory as Working Directory. Calibre files created during the extraction is stored in this directory.

Inputs

Click the red Inputs button

Your screen should now look like that shown below:

	Calibre interactive - PEX	000			
Eile Transcript	Elle Transcript Setup Help				
Bules Jipputs Outputs	Layout Netlist H-Cells Blocks Probes File: [atch2layout.gdsi]				
Run <u>C</u> ontrol Tr <u>a</u> nscript	Format: GDSI -	Export from layout viewer			
Run <u>P</u> EX	Top Cell: latch2				
Start R⊻E					

Outputs

Click on the Outputs tab on the left to set the output file.

- Extraction Type: Select Transistor Level, R + C + CC, No Inductance
- Under the **Netlist** tab
 - File: latch2.pex.netlist
 - This option is already be filled in by the tool, leave it as is
 - Format: HSPICE
 - Use Names From: LAYOUT
 - o select "View netlist after PEX finishes"

	Calibre Interactive - PEX	
Eile Transcript	Setup	Help
Elle Transcript Bules Jnputs Qutputs Run Control Transcript Run EEX Start RVE	Extraction Type: Transistor Level R + C + CC No Inductance Netlist Nets Reports SVDB Format: HSPIDE Use Names From: LWOUT File: latch2.pex.netlist View netlist after PEX finishes	

- Under the Nets tab
 - Extract parasitics for: Select "All Nets"
- Under the **Reports** tab
 - PEX Report File: NAND2.pex.report
 - This option is already be filled in by the tool, leave it as is
 - Select "Generate PEX Report" and "View Report after PEX finishes"
- Under the **SVDB** tab
 - SVDB Directory: svdb_nand2
 - Select "Generate cross-reference data for RVE" and "Start RVE after PEX"

Select Setup > PEX Options from the top menu bar. In the Netlist tab, click the Ground node name: check box and enter GND as shown.

Calibre Interactive - PEX					
Eile Transcript Set	h	Help			
Bules Jnputs Qutputs PEX Options Run Control Transcript	Netlist LVS Options Connect Misc Include LEFDEF Inductance Database Library Ground node name: GRD Ground layer name: Hierarchy separator: / Gutput intentional device locations Gutput intentional device locations				
Run <u>P</u> EX Start R <u>V</u> E	Output parasitic resistor I locations widths I layers Enable TICER reduction below:	Hz			
	Enable CC reduction: Absolute Ratio Scale I Extract metal fill: EXTRACT = Ground coupling capacitors: All Less than: Size multiplier for length units (in metars): Formatter map file:	View			

In the LVS Options tab, set the Recognize gates: check box to All. Also, make sure that VDD is one of the Power nets: and GND is one of the Ground nets:

Calibre Interactive - PEX						
Eile Transcript	<u>S</u> etu	P			Help	
Bules	1	vetlist LV	V5 Opti	ons Connect Misc Include LEFDEF Inductance Database Library)	
<u>O</u> utputs		Power n	ets:			
PEX Options		Ground a	nete:		- 11	
Rup Control						
Tr <u>a</u> nscript		LVS Report Options: None				
					=11	
Run <u>P</u> EX		Recogni	ze gate	s: 🔶 All 🔿 Simple 🔿 None		
		🔲 🗆 Mix s	subtype	s during gate recognition		
Start R⊻E						
		Filter Unused Device Options:				
		LS	Opt	Filter Description	-14-	
			AB	MOS devices with source, drain, and gate pins tied together.		
			AC	MOS devices with floating gate pin, and source and drain pins connected to a single power net.		
			AD	MOS devices with floating gate pin, and source and drain pins connected to a single ground net.		
			AE	MOS devices with source, drain, and gate pins all floating.		
			AF	MOS devices with source and drain pins field together.		
			AG	MOS devices with all pins tied together, including bulk and optional pins.		
			B	MOS devices if the gate is floating or has no path to any pad, and either the source or drain is floating.		
			C	MOS devices with gate fied to power or ground and either the source or drain floating.		
			D	MOS devices if the gate is floating, either source or drain have a path to power, and neither source nor drain have paths to ne	01	
			E	MOS devices if the gate is floating, either source or drain have a path to ground, and neither source nor drain have paths to r	IC	
			F	MN and LDDN devices with the gate tied to ground.		
			FY	MN and LDDN devices with gates fied to ground.		
			G	MP and LODP devices with the gate fied to power.		
			GY	MP and LDDP devices with the gate field to power. Connects source and drain nets if not connected to different pads.		
			н	MUS devices with both source and drain fied to power, and series MOS devices with both ends of the series field to power.		
			1	MOS devices with both source and drain lied to ground, and series MOS devices with both ends of the series lied to ground.		
			IH	MOS devices with one of the source/drain pins tied to ground and the other tied to power, and series MOS devices with one of	16	
		2			3	

Then click the "Run PEX" button. If PEX runs successfully, with out any error, then you will be able to view PEX Report File - NAND2.pex.report and also PEX Netlist File - NAND2.pex.netlist, which is the extracted netlist from the layout along with parasitic capacitances and resistances

Click on the "Transcript" tab in Calibre Interactive - PEX to see the log file.

Now let us understand the NAND2.pex.netlist File

The main hspice netlist "NAND2.pex.netlist" contains only the intentionally designed devices.

Filenames with the extensions ".pex" and ".pxi" files are included in the "latch2.pex.netlist"

- The .pex file (actually called "NANd2.pex.netlist.pex") contains one subckt per net: each subckt containing the RC tree structure modeling the net.
- The **.pxi** file (actually called "NAND2.pex.netlist.latch2.pxi") contains the connections between the parasitic networks i.e. containing the instance calls to the

net model subckts along with the coupling capacitors connecting between these net model instances.

The NAND2.pex.netlist is as shown below

```
* File: NAND2.pex.netlist
* Program "Calibre xRC"
* Version "v2006.1_19.20"
.include "NAND2.pex.netlist.pex"
.subckt NAND2 GND! Z VDD! A B
* В
      В
* A
       Α
* VDD! VDD!
* Z
       Z
* GND! GND!
MM1 X N_A_MM1_g N_GND!_MM1_s N_GND!_MM1_b NMOS_VTL L=5e-08 W=9e-08
MMO N_Z_MMO_d N_B_MMO_g X N_GND!_MM1_b NMOS_VTL L=5e-08 W=9e-08
MM2 N_Z_MM2_d N_A_MM2_g N_VDD!_MM2_s N_VDD!_MM2_b PMOS_VTL L=5e-08
W=9e-08
MM3 N_Z_MM2_d N_B_MM3_g N_VDD!_MM3_s N_VDD!_MM2_b PMOS_VTL L=5e-08
W=9e-08
.include "NAND2.pex.netlist.NAND2.pxi"
.ends
```

Extract with Parasitic Capacitances Only

Looking through the **.pex** and **.pxi** files, you should see that even this very simple circuit has resulted in hundreds of capacitors and resistors. This level of detail is necessary to achieve the highest degree of accuracy, but for larger circuits, it can slow an HSPICE simulation to a crawl. While the resistances are necessary to accurately understand the *delay* of a circuit, the *power* dissipation can be predicted very well using capacitances only. We often call this a "lumped-C model" for a net, as opposed to an "RC-tree model".

To extract a lumped-C model, make the following change in the *Calibre Interactive - PEX* window:

Outputs

• Extraction Type: Change from "R + C + CC" to "C + CC"

Re-run PEX, and you should find that you have capacitances only. Not only that, but the number of capacitances has reduced by a factor of 10.

PEX.Netist.File - Jatch2.pex.netlist	
Elle Edit Options Windows	
<pre></pre>	

Close the netlist window. Close Calibre PEX and save the runset if you wish. Exit IC Station.

Helpful website:

http://www.eda.ncsu.edu/wiki/Tutorial:Layout_Tutorial2