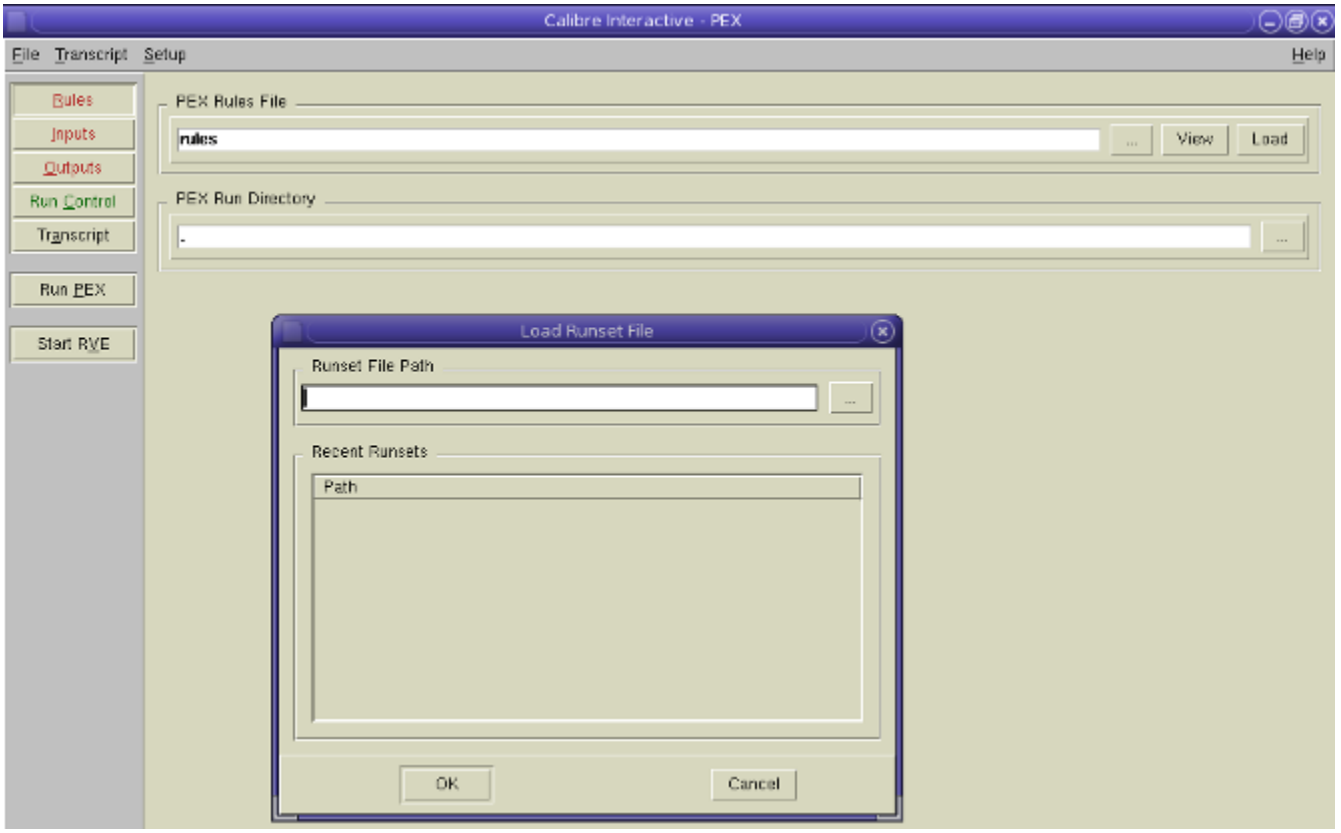
Extraction of Parasitic Capacitance and Resistances for HSPICE Simulation

Make the layout window active and select Calibre > Run PEX from the top menu bar to start a Parasitic EXtraction. You will need to fill in a few screens to properly initialize Calibre. The Calibre setup information can be saved so you only need to enter it once. The Calibre extraction tool reads in your layout file and creates a Spice netlist suitable for simulation.

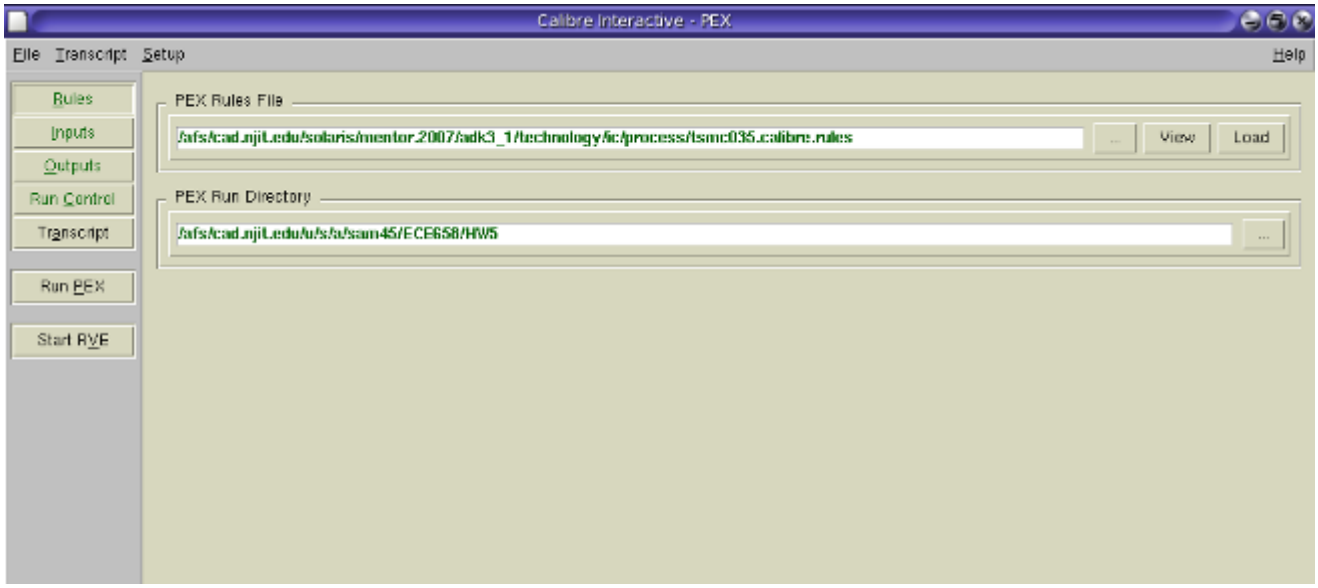
Calibre PEX window should pop up along with Load Runset File window.



Calibre saves all the information of the extraction in a runset file. As we have never saved any runset files before, click cancel.

Rules

Click on the Rules tab in the left, and then on the button with the '...' to choose the rules for the extraction. Browse and choose the file /afs/cad.njit.edu/solaris/mentor.2007/adk3_1/technology/ic/process/tsmc035.calibre.rules.

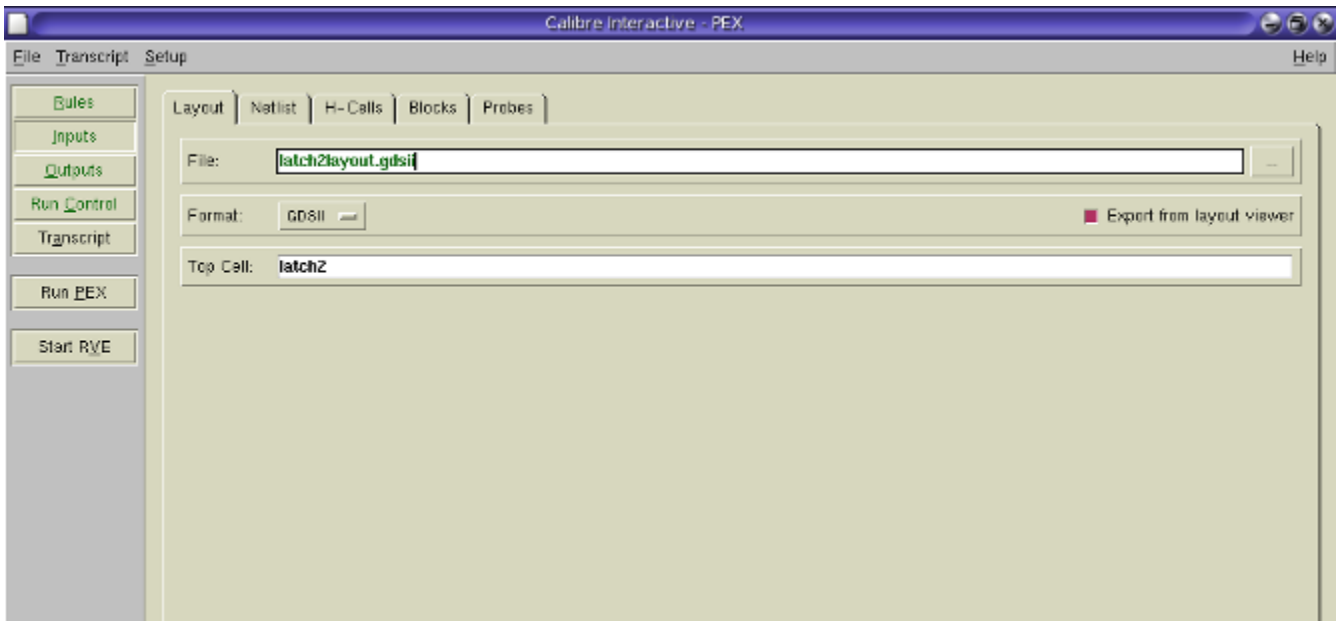


Choose a PEX Run Directory as Working Directory. Calibre files created during the extraction is stored in this directory.

Inputs

Click the red Inputs button

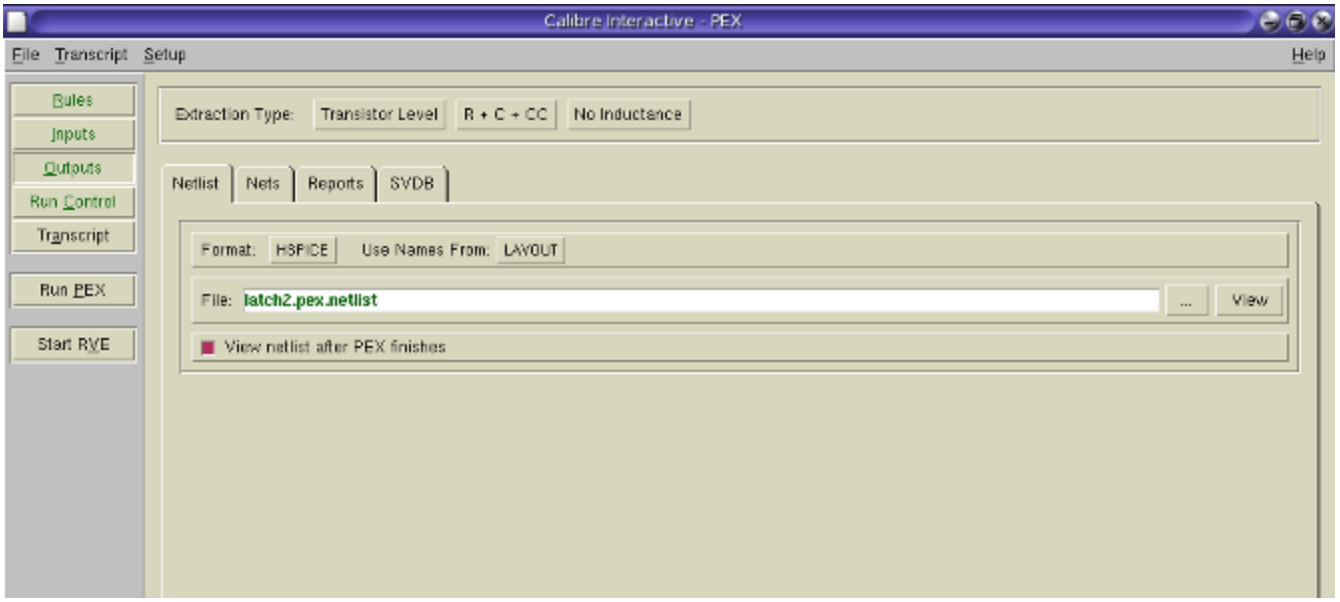
Your screen should now look like that shown below:



Outputs

Click on the Outputs tab on the left to set the output file.

- Extraction Type: Select Transistor Level, R + C + CC, No Inductance
- Under the **Netlist** tab
    - File: latch2.pex.netlist
    - This option is already be filled in by the tool, leave it as is
    - Format: HSPICE
    - Use Names From: LAYOUT
    - select "View netlist after PEX finishes"

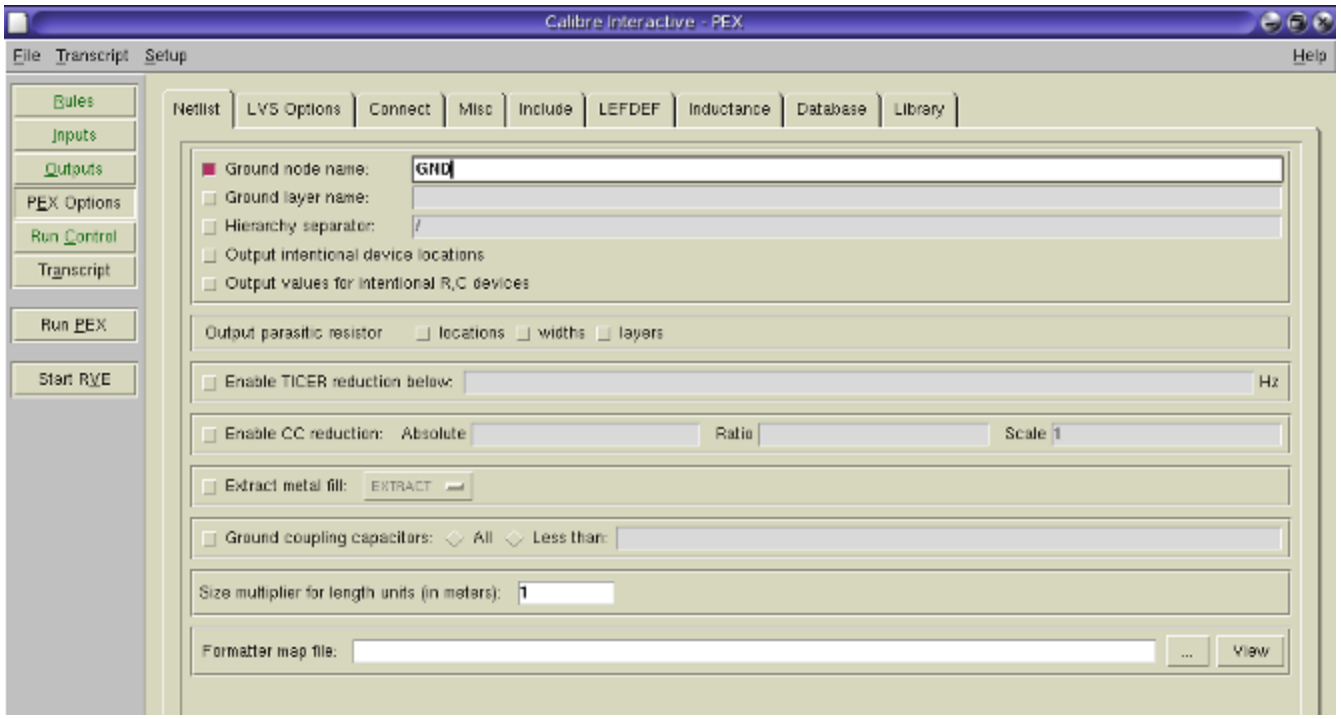


- Under the **Nets** tab
    - Extract parasitics for: Select "All Nets"

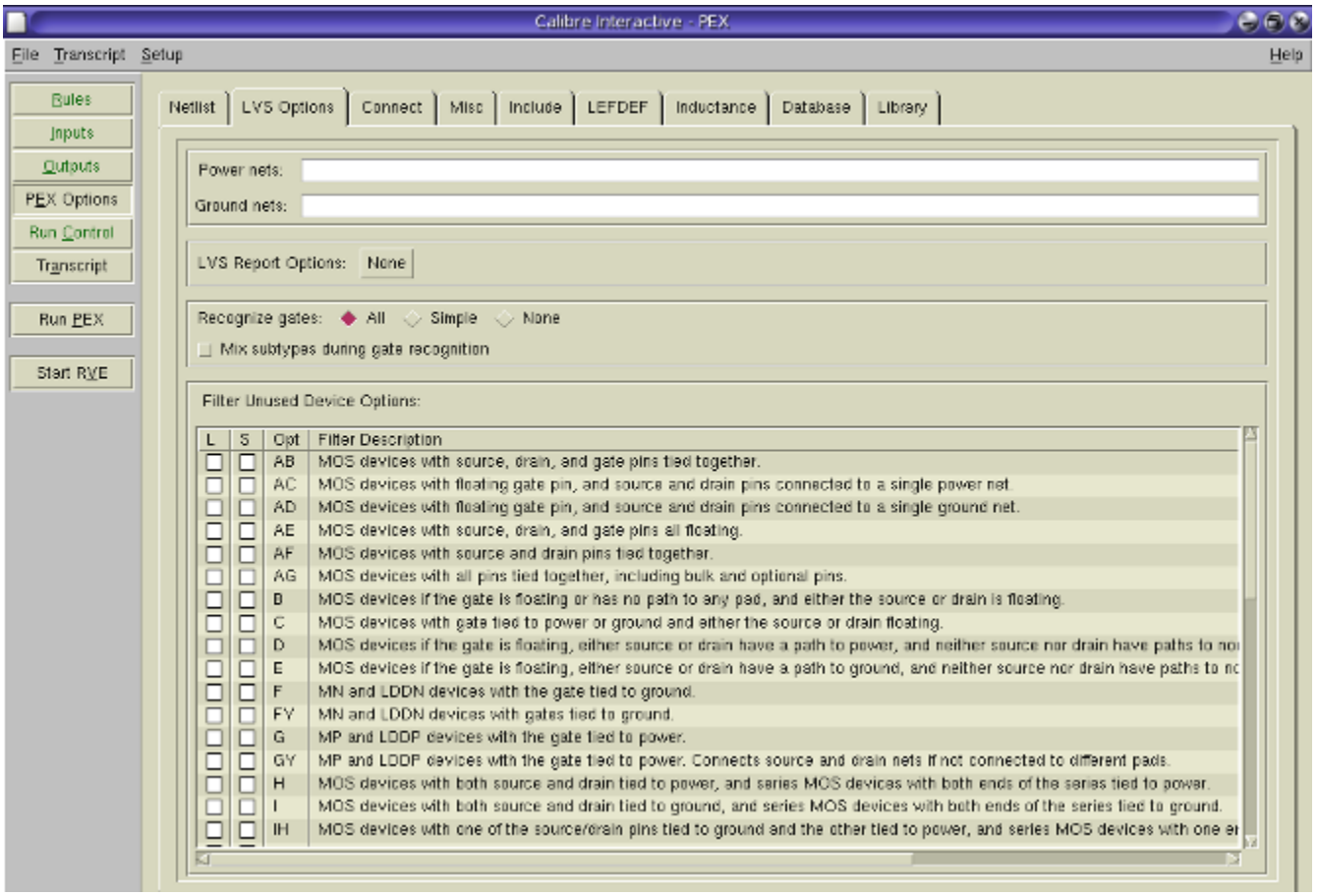
- Under the **Reports** tab
    - PEX Report File: NAND2.pex.report
    - This option is already be filled in by the tool, leave it as is
    - Select "Generate PEX Report" and "View Report after PEX finishes"

- Under the **SVDB** tab
    - SVDB Directory: svdb_nand2
    - Select "Generate cross-reference data for RVE" and "Start RVE after PEX"

Select Setup > PEX Options from the top menu bar. In the Netlist tab, click the Ground node name: check box and enter GND as shown.



In the LVS Options tab, set the Recognize gates: check box to All. Also, make sure that VDD is one of the Power nets: and GND is one of the Ground nets:



Then click the “Run PEX” button. If PEX runs sucessfully, with out any error, then you will be able to view PEX Report File - NAND2.pex.report and also PEX Netlist File - NAND2.pex.netlist, which is the extracted netlist from the layout along with parasitic capacitances and resistances
.

Click on the "Transcript" tab in Calibre Interactive - PEX to see the log file.

Now let us understand the NAND2.pex.netlist File

The main hspice netlist "NAND2.pex.netlist" contains only the intentionally designed devices.
Filenames with the extensions ".pex" and ".pxi" files are included in the "latch2.pex.netlist"

- The **.pex** file (actually called "NANd2.pex.netlist.pex") contains one subckt per net: each subckt containing the RC tree structure modeling the net.
- The **.pxi** file (actually called "NAND2.pex.netlist.latch2.pxi") contains the connections between the parasitic networks i.e. containing the instance calls to the

net model subckts along with the coupling capacitors connecting between these net model instances.

The NAND2.pex.netlist is as shown below

```
* File: NAND2.pex.netlist
* Program "Calibre xRC"
* Version "v2006.1_19.20"
*
.include "NAND2.pex.netlist.pex"
.subckt NAND2  GND! Z VDD! A B
*
* B     B
* A     A
* VDD!  VDD!
* Z     Z
* GND!  GND!
MM1 X N_A_MM1_g N_GND!_MM1_s N_GND!_MM1_b NMOS_VTL L=5e-08 W=9e-08
MM0 N_Z_MM0_d N_B_MM0_g X N_GND!_MM1_b NMOS_VTL L=5e-08 W=9e-08
MM2 N_Z_MM2_d N_A_MM2_g N_VDD!_MM2_s N_VDD!_MM2_b PMOS_VTL L=5e-08
W=9e-08
MM3 N_Z_MM2_d N_B_MM3_g N_VDD!_MM3_s N_VDD!_MM2_b PMOS_VTL L=5e-08
W=9e-08
*
.include "NAND2.pex.netlist.NAND2.pxi"
*
.ends
*
```

Extract with Parasitic Capacitances Only

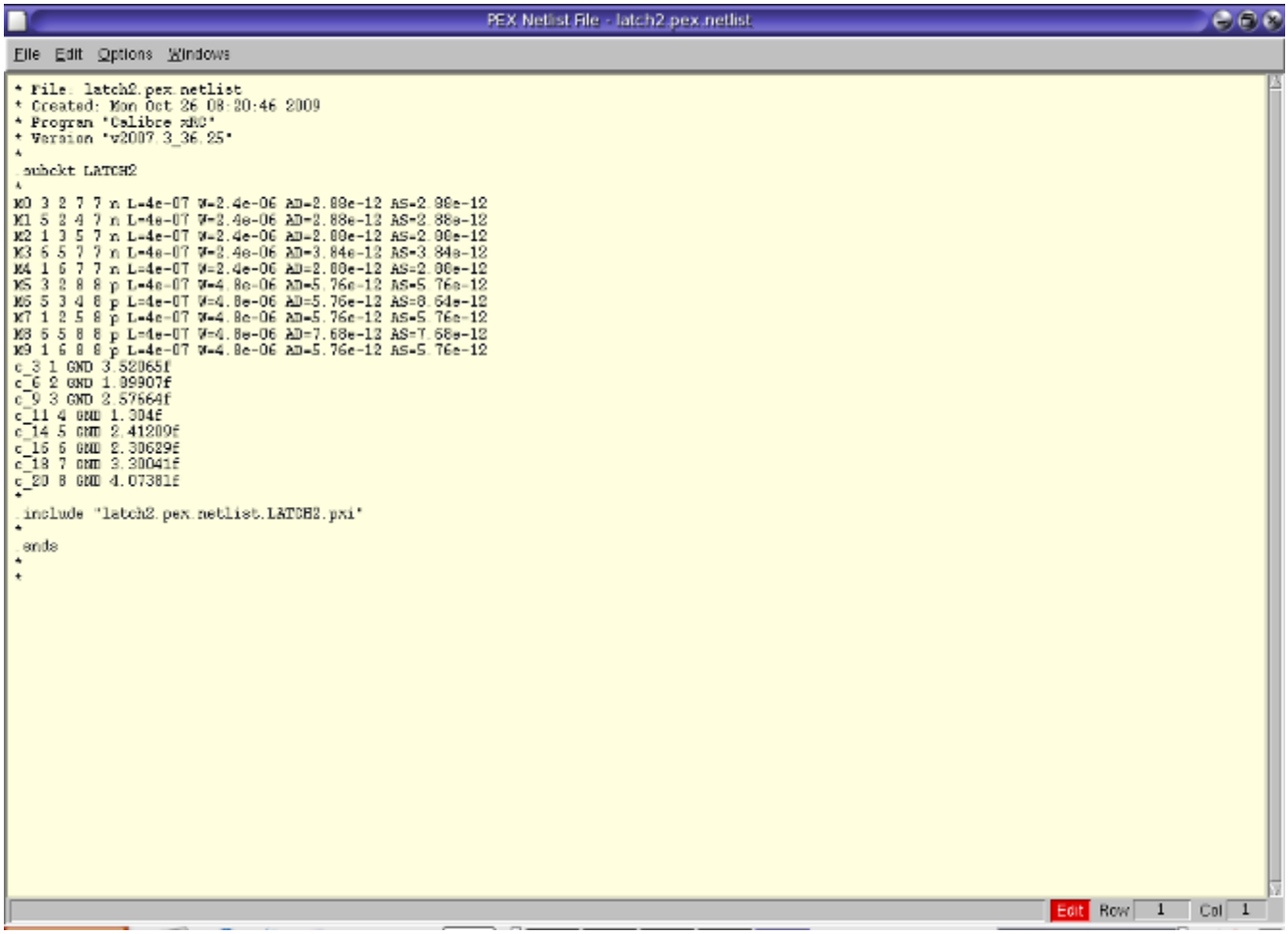
Looking through the **.pex** and **.pxi** files, you should see that even this very simple circuit has resulted in hundreds of capacitors and resistors. This level of detail is necessary to achieve the highest degree of accuracy, but for larger circuits, it can slow an HSPICE simulation to a crawl. While the resistances are necessary to accurately understand the *delay* of a circuit, the *power* dissipation can be predicted very well using capacitances only. We often call this a "lumped-C model" for a net, as opposed to an "RC-tree model".

To extract a lumped-C model, make the following change in the *Calibre Interactive - PEX* window:

Outputs

- Extraction Type: Change from "R + C + CC" to "C + CC"

Re-run PEX, and you should find that you have capacitances only. Not only that, but the number of capacitances has reduced by a factor of 10.



Close the netlist window. Close Calibre PEX and save the runset if you wish. Exit IC Station.

Helpful website:

http://www.eda.ncsu.edu/wiki/Tutorial:Layout_Tutorial2