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# Interface Hardening with Deuterium Implantation

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Incorporation of deuterium to passivate silicon-dangling bonds at the Si-$SiO_2$ interface through ion implantation before the growth of the gate oxide is the focus of this work. Polycrystalline silicon gate n-channel metal-oxide-semiconductor diodes with 4 nm gate oxide grown on deuterium-implanted p-type silicon ⟨100⟩ substrate were investigated. Deuterium implanted at a light dose of $1 \times 10^{14}/cm^2$ at 25 keV reduced oxide leakage current due to reduction in oxide charge and interface traps. Out-diffusion of deuterium during oxidation was observed for lower energy implant. Higher energy implant, on the other hand, causes enhanced substrate damage and prevents deuterium from reaching the Si-$SiO_2$ interface. Formation of Si—D bonds at the interface as well as in bulk oxide seems to reduce bulk electron traps as noticed in constant current stress measurements. Interface state density $N_{it}$ as obtained from the conductance measurements suggests that implanted deuterium passivates the silicon dangling bonds, thereby reducing the interface charge. The $N_{it}$ distribution in silicon bandgap shows that there is significant reduction in $N_{it}$ for deuterium-implanted samples at an energy position about 0.2 eV above midgap, which corresponds well with $P_{b0}$ center 0/− transition level of $E_v + 0.85$ eV.
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In metal oxide semiconductor (MOS) devices the Si/$SiO_2$ interface is most widely studied, but reliability of the interface remains a major concern today. Low-temperature postmetal anneals (350-450°C) in forming gas (10% $H_2$) have been successfully used in MOS fabrication technologies to passivate silicon dangling bonds and consequently, to reduce Si/$SiO_2$ interface trap charge density.[1] This treatment is imperative since silicon-dangling bonds at the Si/$SiO_2$ interface are electrically active and lead to the reduction of channel conductance and also result in deviations from the ideal capacitance-voltage (C-V) characteristics. Electron spin resonance (ESR) measurements[2] performed in conjunction with deep-level transient spectroscopy (DLTS) and C-V measurements have elucidated the role of hydrogen in this passivation process,[3,4] which is described as $P_b + H_2 \rightarrow P_bH + H$, where $P_bH$ is the passivated dangling bond. These measurements indicate that for the oxides grown on Si(111), the density of the interface trap states in the middle of the forbidden gap decreases from $10^{11}$-$10^{12}$ $cm^{-2}$ $eV^{-1}$ to about $10^{10}$ $cm^{-2}$ $eV^{-1}$ after the postmetal anneal process step. The Si(100)/$SiO_2$ material system, which is technologically more significant, exhibits the same qualitative behavior. Therefore, the n-MOS threshold voltage and transconductance distributions on a wafer annealed in forming gas (10% $H_2$) show significant improvement compared with an untreated wafer. The high mean value and variation of the threshold voltage and reduced channel mobility across the untreated wafer is a clear indication of the unacceptable levels of interface trap density for complementary MOS (CMOS) circuit operation and stability.

The importance of hydrogen in the electrical degradation process for the Si/$SiO_2$ system was demonstrated by Nicollian *et al.*[5] by using a series of experiments performed on MOS capacitors. Nicollian *et al.* showed that there was a one-to-one correspondence between the hydrogen lost (*i.e.*, reduced activity) and negative charge produced in a hydrated $SiO_2$ layer in the presence of electron currents. In the channel hot carrier aging investigation, the Si/$SiO_2$ interface degrades by hot carriers that are traversing the device from source to drain. This hot carrier degradation in MOS transistors manifests itself in the form of threshold voltage instability, transconductance degradation, and increase in the subthreshold slope over time. It has been suggested that the generation of the interface trap states is due to hot carrier stimulated hydrogen desorption and depassivation of the silicon dangling bonds. The existence of degradation, at low voltages, points to the multiple vibrational excitation mechanism of H desorption at the Si/$SiO_2$ interface and hints at a dependence of desorption mechanism on both voltage (electric field) and current density. Obviously, hot carrier induced transistor degradation will continue to be a major constraint for the design of high-performance sub-0.18 μm CMOS devices. However, under bias condition the MOS transistor performance can degrade as a result of desorption of the hydrogen that is passivating the dangling bonds at the Si/$SiO_2$ interface or bonds at the $SiO_2$/polysilicon interface due to channel hot carriers (electrons and holes). Hot carrier reliability concerns are further exacerbated by ever-ongoing miniaturization (scaling) efforts and complexity in device processing. Replacing hydrogen with deuterium does have the same chemical impact but is technologically advantageous.

Lyding, Hess, and Kizilyalli[6,7] recently reported significant improvement in hot carrier lifetime when the interface was passivated by deuterium rather than hydrogen. Since the chemistry of deuterium and hydrogen is virtually identical, either atom is equally suitable for passivating the dangling bonds at interfaces. This development inspired a new wave of interest in deuterium in the Si-$SiO_2$ system.[8-11] Mogul *et al.*[8] showed that deuterium-sintered submicrometer devices are less prone to degradation due to electrical stress than forming gas annealed devices. Similarly, Devine *et al.*[9] confirmed that the degradation in channel transconductance is mainly due to creation of interface states, and a significant reduction in interface states was noticed for deuterium-annealed devices. The observed improvement in the degradation rates (hot carrier lifetimes) in the transistors is a result of the large difference in the desorption rates of the two isotopes with the loss of hydrogen being significantly greater than deuterium.[7] Studies also indicate that transistors annealed in deuterium are much more resilient against plasma process induced damage (as quantified by Si/$SiO_2$ interface trap generation and gate oxide leakage).[12] In a complementary study, the characteristics of deuterium as a function of thermal annealing were examined in thin $SiO_2$ films[10] and in CMOS devices.[11]

Significant challenges still remain in integrating deuterium annealing into mainstream semiconductor manufacturing. The improvement in hot carrier lifetime in deuterium-annealed samples could be unstable and relaxed when the samples are subjected to further processing.[13] When CMOS technologies incorporate multiple metal and dielectric layers, the improvement due to deuterium sintering was reduced further.[14] In addition, undoped polycrystalline silicon[11] and $Si_xN_y$, used as a sidewall spacer, serve as a diffusion barrier for deuterium,[14] which could limit the transportation of deuterium to the Si-$SiO_2$ interface during annealing. Furthermore, a nonuniform deuterium distribution at the interface might be possible

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due to these barriers. These limitations can be overcome by extended time and temperature anneals at higher deuterium concentration,[15] but cycle time associated with extended anneals and detrimental effects of higher temperatures on the long-term metal properties require exploring possible alternatives for deuterium incorporation at the Si-$SiO_2$ interface. In CMOS processing middle-of-line and back-end-of-line deuterium anneals were suggested.[16] In an alternative approach,[17] when gate oxide was grown in $D_2O$ ambient, the interface state density not only reduced the process but also suppressed charge trapping in the oxide.[17] Recently, it was observed that the improvement of interface properties depends on the method whereby deuterium is incorporated into the Si-$SiO_2$ interface after deuterium was incorporated by deuterium pyrogenic oxidation.[18] The behavior of deuterium in the Si-$SiO_2$ system, therefore, is not very well understood, and there is no study to understand desorption of deuterium from the Si/$SiO_2$ interface, even though there is a fundamental difference in surface and interface desorption.

In this work we have introduced deuterium by implantation into silicon substrate before the thin gate oxide is grown to incorporate deuterium at the Si/$SiO_2$ interface in the MOS device. Deuterium implantation provides a spatially uniform distribution of deuterium, whereas deuterium diffusion can have a localized effect, such as higher concentration at the drain and source end of the channel due to the presence of sidewall spacers. Even though this approach will streamline process integration and reduce cycle time, two questions still remain. Will the benefit of deuterium incorporation still exist after the many process steps required to complete the device, and what will be the impact of implantation on gate oxide? Earlier studies by Park and Helms[19] on implantation of deuterium in bare silicon and silicon oxide systems show that the release of deuterium from bare silicon is possible at 600°C, whereas deuterium might diffuse out completely from a Si/$SiO_2$ system at 900°C. The distribution of implanted deuterium, when subjected to annealing, therefore, depends on the presence of oxide film. This work investigates oxide/interface quality when the oxide was grown on deuterium-implanted silicon substrate.

Ion implantation conditions can cause irreparable substrate damage and thereby deteriorate oxide integrity. In a separate study we have demonstrated that a low-energy nitrogen implant before gate oxide growth could be used to incorporate nitrogen at the Si/$SiO_2$ interface.[20,21] After successful incorporation of nitrogen by using ion implantation it is possible to implant deuterium before oxide growth to improve oxide reliability. However, extreme caution can be used to select implantation energy and dose. We have used different implantation energies to optimize the process. Implantation energy of 25 keV with a dose of $1 \times 10^{14}/cm^2$ was found to be most appropriate for device applications. Oxides grown without any deuterium implantation and without any annealing were used as a reference device (control).

## Experimental

At room temperature (300 K), deuterium was implanted into p-type Si(100) substrates with a resistivity of 1.25-2.0 Ω cm. Three different implantation energies of 15, 25, and 35 keV were used with a constant dose of $1 \times 10^{14}/cm^2$ through a 200 Å sacrificial oxide. The sacrificial oxide was used to avoid any irreparable surface damage. SRIM simulation for the above-mentioned implantation energies shows peaks at 0.38, 0.6, and 0.75 μm, respectively. The gate oxide was then grown in dry $O_2$ at 800°C for 20 min after the sacrificial oxide was removed. The oxide thickness was 4 nm for all the splits. The gate oxide thickness was measured by ellipsometry at 16 sites on each wafer to obtain an averaged value. No apparent thickness variation was noticed due to deuterium implantation. Some of the wafers were annealed at 850°C for 20 min in $N_2O$ ambient. A 3000 Å polycrystalline silicon layer was then deposited at 600°C and a blanket implantation of phosphorus was given at 30 keV with a dose of $10^{16}/cm^2$ given to dope the polysilicon layer. A furnace anneal for 30 min at 800°C was given to all samples for

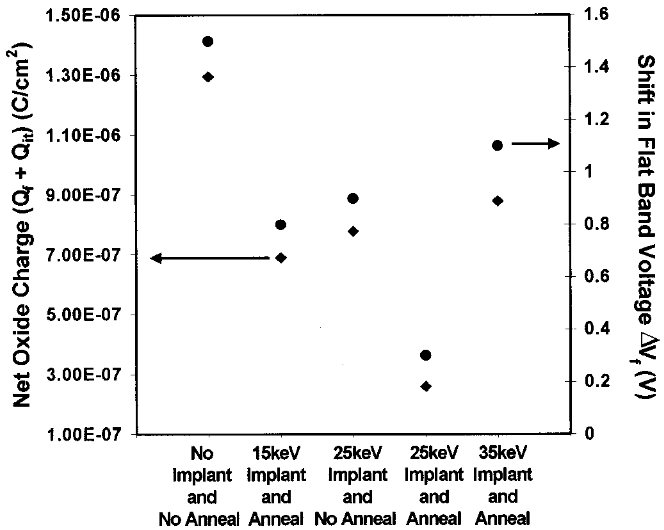


**Figure 1.** (●) The flatband voltage shifts and (♦) net oxide charge extracted from high-frequency C-V measurements for various deuterium-implanted samples.

dopant activation in polysilicon. The doping in polysilicon would be approximately $10^{19}$ cm$^{-3}$, which keeps the Fermi level close to conduction band in polysilicon gate. The surface was then patterned using reactive ion etching to form MOS capacitors with 50 μm diam. High-frequency C-V measurement was used to characterize the oxide. A constant current stress of 200 mA/cm$^2$ in gate injection mode was applied to evaluate the bulk oxide traps. The conductance method at 1 MHz was employed by using an HP 4156B parameter analyzer to estimate interface state density ($N_{it}$).

## Results and Discussion

*Oxide charge and trapping characteristics.*—The observed flatband shifts and the net oxide charge from high-frequency C-V measurements reveal that the control devices induce a negative voltage shift, indicating a net positive charge in the oxide and/or at interface. Figure 1 shows implanted deuterium partially neutralizes the oxide/interface charge. The net oxide charge is rather high for no implant and no anneal sample. Note that no forming gas anneal was given to any of the samples. C-V measurements are affected by the capacitive response of fast interface states and fixed oxide charge. A sharp reduction in net oxide charge indicates that deuterium implanted at 25 keV devices incurred increased interface passivation of the dangling bonds at the Si-$SiO_2$ interface compared to devices without any deuterium implant. For 25 keV deuterium-implanted and annealed sample, a significantly reduced interface state and fixed oxide charge was observed. Wafers implanted at 25 keV (no anneal) have comparable flatband shift and net oxide charge with that of 15 keV implanted and annealed devices. It is known that postoxidation annealing reduces oxide charge. We believe the effect of annealing reduced the fixed oxide charge of 15 keV implanted and annealed devices, but the observed characteristic is possibly due to out-diffusion of deuterium from the interface for the 15 keV implanted (annealed) wafer compared to that of the 25 keV implanted (unannealed) wafer. The 15 keV implantation is comparatively shallow (0.38 μm) and during oxide growth out-diffusion of deuterium is possible. The reduction of oxide charge in the 25 keV implanted sample after annealing clearly shows an enhanced deuterium presence. Retention of deuterium in the 25 keV implanted sample after growth of the 4 nm of gate oxide was observed when investigated by secondary ion mass spectroscopy (SIMS) and reported elsewhere.[22] Since no forming gas anneal was used in this experiment, the presence of deuterium therefore retards the charged defect sites at the interface. The observed oxide charge and flatband shift for the 35

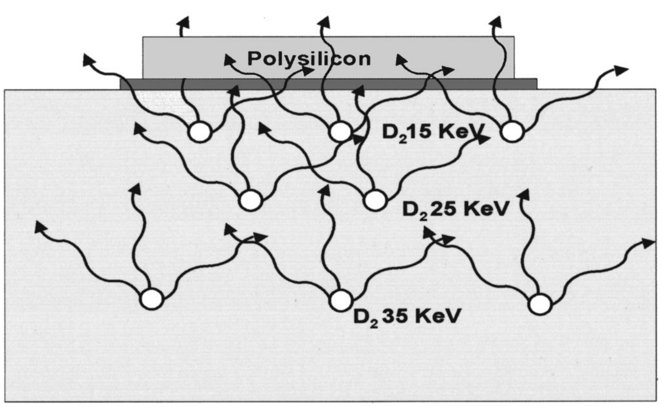


**Figure 2.** Schematic representation of possible deuterium diffusion in silicon for various implantation conditions shows that deuterium might have out-diffused for 15 keV implantation and never reached the interface for 35 keV implantation during gate oxide growth.

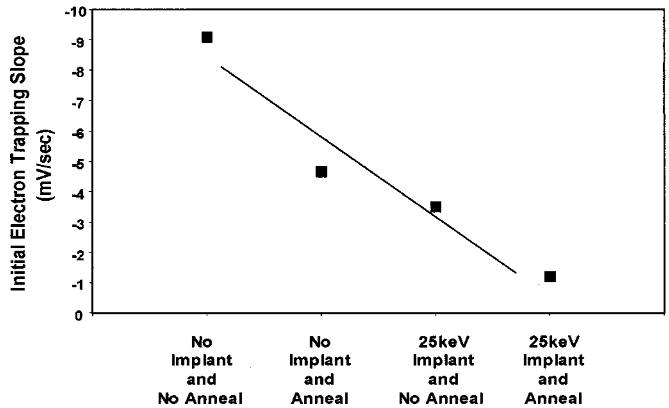


**Figure 3.** The average values of the initial electron trapping slope for the 25 keV deuterium-implanted samples when compared to control device. Initial oxide trap creation was suppressed for deuterium-implanted sample.

keV implantation and annealed sample, on the other hand, is not much better than the control wafer, suggesting irreparable crystal damage occurred as the implantation energy was increased. In addition, since the implantation depth for 35 keV implantation is rather deep (approximately 0.75 μm), during oxidation deuterium might have diffused into vacancies rather than diffusing toward the interface. The interface passivation thus depends on the implantation condition (Fig. 2) as the oxide growth temperature and polysilicon dopant activation annealing is 800°C for all cases.

To investigate the impact of deuterium implantation on trap creation in bulk oxide only 25 keV implanted devices were subjected to a constant current stress of 200 $mA/cm^2$ in gate injection mode and compared with that of the control sample. The voltage required the current be recorded as a function of time when the current is injected into the gate oxide of a MOS capacitor. This voltage variation relates directly to the net charges trapped under the current stress. The slope of the initial portion of the voltage curve during injection represents the net electron-trapping rate.[23] This trapping process is initially dominated by the filling of pre-existing empty electron traps per injected electron under a particular stress condition. The initial slope can be obtained by approximating the earliest (or the steepest) part of the voltage-time curve with a straight line. During this period the hole trapping rate should be saturated and remain constant and the electron trap creation rate should be approximately constant. Different initial electron trapping slopes (IETS) thus provide an estimate of the rates of filling existing electron traps, and therefore are related to initial bulk oxide charge. The average values of the IETs for 25 keV implanted devices are shown in Fig. 3. There is about an order of magnitude suppression of trap creation over the control wafer with deuterium implantation and annealing. Even without any annealing wafers with deuterium implantation show improvement over the control sample. The suppression of trap creation can also be explained by thermal desorption characteristics of implanted deuterium as described previously. Deuterium atoms incorporated by 25 keV implantation not only diffuse into the $Si/SiO_2$ interface, react with interface dangling bonds, and form Si—D bonds, but also form the Si—D bonds in bulk $SiO_2$.[18] For high-density constant current stress condition at lower voltages, deuterated devices show lower desorption rates due to the resonance between the Si—D bond bending mode and transverse optical phonon of bulk silicon.[24] The presence of deuterium at the interface and in the bulk oxide, therefore, suppresses the hole-induced increase in the density of electron traps at the near interface region during electron stress for 25 keV implanted devices.

*Interface state density*.—Next, interface state density $N_{it}$ for different implantation conditions needs to be investigated. The conductance method was employed to measure $N_{it}$. Figure 4a shows measured conductance at 1 MHz as a function of gate voltage. The magnitude of the conductance peak is much smaller for the 25 keV implanted oxide compared to no-implant oxide. The comparable conductance peak for 15 keV deuterium implantation shows some improvements over the control device but much higher than that of the 25 keV implanted devices. The conductance peak for 35 keV deuterium implantation is larger than the peak of the control device (not shown in Fig. 4a). Conductance measured at 10 kHz and 1 MHz for 25 keV implanted oxide is shown in Fig. 4b. The increase in peak magnitude at higher frequency is due the series combination of oxide capacitance with that of the impedance of interface states. The conductance peak shifts to a gate bias closer to flatband condition with increase in frequency due to the dependence of carrier time constant of the interface states on band bending.[25]

Figure 5 shows the peak $N_{it}$ values for various deuterium-implanted devices. The initial density of interface states (no implant and no anneal) is rather high, with a peak value around $10^{13}$ $cm^{-2}$ $eV^{-1}$. However, as can be seen in Fig. 5, $N_{it}$ decreases initially with increase in implantation energy (15-25 keV) but increases again once the implantation energy is increased further (25-35 keV). The line in Fig. 5 serves as a visual guide. The 25 keV deuterium-implanted and annealed sample shows the lowest density of interface states. Even though annealing reduces $N_{it}$, note that $N_{it}$ for 15 keV implanted and annealed sample is higher than that of the unannealed 25 keV implanted device. For 35 keV implantation $N_{it}$ increases sharply, indicating strong effect of implantation-induced substrate damage. This agrees well with our findings from the C-V measurement that some of the deuterium atoms are lost during oxide growth due to out-diffusion for shallower implantations (Fig. 2). It seems that if the implantation dose is appropriate, deuterium tends to remain at the interface during oxide growth. However, if the implantation dose is high (~35 keV implant) the thermal budget may not be able to remove the implantation damage. In addition, the improvement in $N_{it}$ for 25 keV implanted and annealed sample indicates a completely different behavior of deuterium if oxide is grown on the implanted substrate compared to annealing in an inert ambient.[19] It is known that the stability of the Si—H bond increases when silicon atoms bond with larger electronegative oxygen atoms.[26] Therefore, it is believed that the strength of the Si—D bond that forms during oxidation is stronger than that of the Si—D bond that passivates the interface dangling bonds by deuterium annealing. Mitani *et al.*,[18] using thermal desorption spectroscopy, observed a 7% difference in activation energy of desorption between pyrogenic oxide (deuterium incorporated during oxidation) and deuterium-annealed oxide. We believe that stable Si—D bonds that are formed when deuterium is incorporated by ion implantation can sustain a

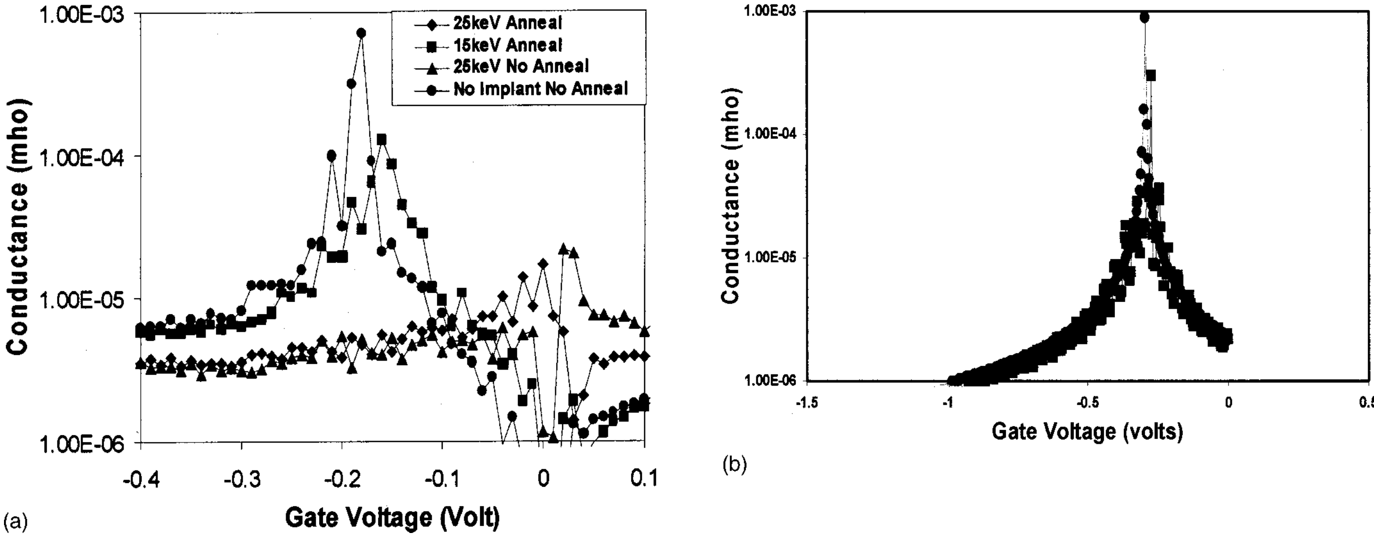


**Figure 4.** (a, left) Measured conductance at 1 MHz as a function of gate voltage for various samples and (b, right) conductance peak for 25 keV implanted sample at two different frequencies.

higher thermal budget of oxidation if the implantation dose and energy are appropriate.

Implanted deuterium likely results in formation of Si—D bonding,[2,27] which plays an important role in the change of distribution of deuterium in silicon and at the Si-$SiO_2$ interface during oxide growth and subsequent annealing. During oxidation deuterium diffuses either to the bulk or to the surface. Since the oxidation temperature (800°C) is the same for all cases, contribution of deuterium to passivate the interface depends on the implantation condition. Once the oxide is formed the thermal energy to break the bond to silicon at the interface is higher than that of bare silicon surface.[19] In addition, since deuterium is tied up with the silicon dangling bonds in large numbers at the interface, the kinetics of breaking the Si—D bond at the interface is quite different from that of bulk silicon. Park and Helms[19] found that the release of deuterium from implantation-induced Si-D or Si-OD configuration in the Si-$SiO_2$ system occurs at around 900°C. We believe, for the 25 keV implanted sample the implantation depth and thermal budget retain most of the deuterium at the Si-$SiO_2$ interface.

*Nature of interface passivation.*—Silicon dangling bonds account for a large portion of the intrinsic electrically active states at the Si-$SiO_2$ interface. There are two types of these dangling bond defects, namely, $P_{b0}$ and $P_{b1}$ on the [100] interface. $P_{b0}$ is identified as a silicon atom bonded to three other silicon atoms with a fourth available bonding orbital left dangling, designated •Si≡Si.[2] Although these states are distinguishable spectroscopically, $P_{b1}$ is insignificant as an electrical interface state[4] whereas all $P_{b0}$'s are electrically active interface states. The variation of interface state densities *vs.* energy with respect to midgap estimated from the conductance method is shown in Fig. 6 for deuterium-implanted samples. The trap energy $E_T$ is with respect to intrinsic Fermi level $E_I$. We only compared the 25 keV deuterium-implanted (annealed and unannealed) with that of no implant and no anneal sample to investigate the nature of interface states. The interface states were sensitive to ~1 μs and the slower states were not investigated in this experiment. The conductance method was applied by Uren *et al.*[28] to investigate interface states in n-type Si(100) where they have grown 19 nm oxide at 900°C. The interface state density profiles observed in Ref. 28 were inconsistent with the profiles in Fig. 6. It is because the 4 nm deuterium-implanted oxide was grown on p-type substrate at 800°C. Interface states above the midgap are clearly passivated for unannealed deuterium-implanted samples. It is inter-

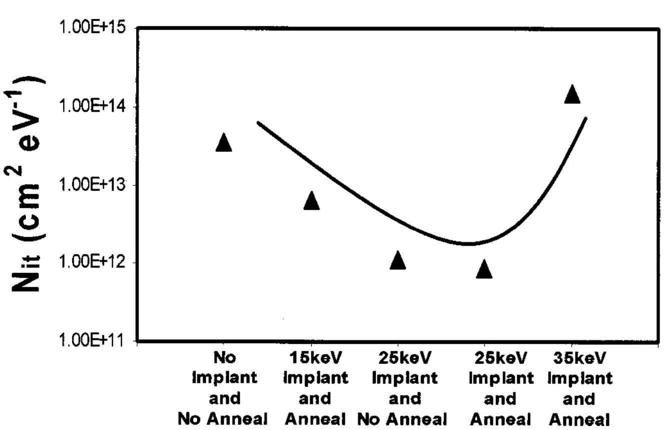


**Figure 5.** Peak $N_{it}$ values for different deuterium implantation conditions indicate that $N_{it}$ went through a minimum value (for 25 keV implantation) as a function of implantation energy.

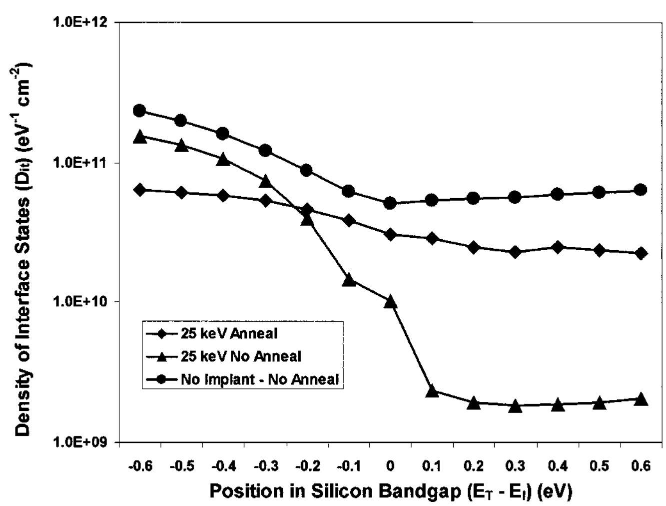


**Figure 6.** Density of interface traps $D_{it}$ as obtained from the conductance measurements. The trap energy $E_T$ is with respect to intrinsic Fermi level $E_I$.

esting to note that the interface state density above the midgap has increased for the deuterium-implanted and 850°C annealed samples. However, it has the lowest $N_{it}$ below midgap and above the valence bandedge.

Since $P_{b0}$ states account for the vast majority of electrically active traps, the results of the present investigation of ion implantation of deuterium to passivate silicon dangling bonds indicate that the interface state density $N_{it}$ is in accordance with the predicted behavior of $P_{b0}$ centers.[29] In the (100) Si-$SiO_2$ interface, contribution of $P_{b0}$ centers to $N_{it}$ is through the significant +/0 and 0/− levels at approximately $E_v + 0.2$ eV and $E_v + 0.85$ eV. The $N_{it}$ distribution in Fig. 6 for the unannealed deuterium-implanted sample with the energy position about 0.2 eV above midgap shows significant reduction in $N_{it}$ and corresponds well with EPR measurement for $P_{b0}$ center 0/− transition level of $E_v + 0.85$ eV. Devine *et al.*[9] also found a peak around 0.2 eV above midgap for deuterium-annealed interfaces. They have observed an asymmetry similar to that of deuterium-implanted devices. We believe it could be due to the difference in stoichiometry at the interface in our case. The possible structural configuration of $P_{b0}$ centers by deuterium passivation can explain the reduction in interface states in the deuterium-implanted devices. A deuterium-passivated $P_{b0}$ center eliminates the dangling orbital contribution to $N_{it}$, therefore suggesting that deuterium implantation contributes to the passivation of the $P_{b0}$ centers.

As discussed earlier, during oxidation, deuterium would diffuse through silicon to the interface and react with the $P_{b0}$ centers to passivate the dandling bonds. Since the activation energy for diffusion of deuterium in $SiO_2$ is higher than that of silicon,[19] deuterium (D) is possibly trapped at the interface before diffusing into oxide. The passivation reaction would be $D + P_{b0} \rightarrow DP_{b0}$.[24,30] For a 25 keV deuterium-implanted and annealed device it might be possible that a fraction of deuterium has diffused into the oxide through a depassivation process, whereas most of the deuterium remained at the interface for 25 keV deuterium-implanted and unannealed samples.

## Conclusions

In conclusion it can be said that the incorporation of deuterium at the silicon-silicon dioxide interface using ion implantation before gate oxide growth is an effective means to improve the oxide quality by hardening the interface. This process could be a viable alternative to many hours of annealing through a middle-of-line or back-end process for reliable incorporation of deuterium. The reduction in oxide charge indicates that deuterium implantation brings about a clear enhancement in gate oxide quality. Reduction in preexisting bulk electron trap density has also been observed. A reduction in density of interface traps $N_{it}$ as obtained from the conductance measurements for the deuterium-implanted devices suggests that deuterium implantation contributes to the passivation of the $P_{b0}$ centers. Finally, the selection of appropriate implantation energy, implantation doses, and annealing conditions are important for the optimization of thin oxide quality and reliability in sub-0.13 μm CMOS technologies. Many more experiments are required to understand this process and to estimate the appropriate concentration of deuterium required to passivate the interface. Many systems where hydrogen is used for passivation will benefit from the proposed research, and the transport mechanism of deuterium in silicon will be better understood.

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