EE 658-102 VLSI I Project

2-bit [3x3]x[3x3]
Matrix Multiplier

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<u>OVERVIEW</u>

- The Design
- The Steps of the Project
- The Project Results
- The Future
- The Learning Experience

<u>Design</u>

- Design a chip that will complete the task of multiplying a [3x3] matrix by a [3x3] matrix.
- Meet establish design factors
- Use HSpice for the simulation
- Use IC Graphics for the layout

Design Factors

- Limited to 40-pins
- At least 25 MHz
- Limit Complexity
- Low Noise Margin
- Minimal Clock Skew
- 2000um x 2000um
- Asynchronous Reset

Design Decisions

- Input Pulse 30ns
- Clock 30ns
 - Initial Delay 5ns
 - Rise & Fall Time 5ns
- 3 Multiplier Cells
 - Single Chip 2-bit [3x3] x [3x1] operation
 - Three Chips 2-bit [3x3] x [3x3] operation

Steps to the Design

- Design Logic Diagram
 - Box Level
 - Gate Level
- Develop Semiconductor B_p/B_n Ratio
- Design Transistor Logic
- HSpice Simulation

- IC Graphics Layout
 - Gate Subcells
 - Cells [DFF, Full Adder, Half Adder, Multiplier]
- Extract Capacitance File
- HSpice Simulation
- Check Results
- Adjust Layout if necessary
- Graph Results in Awaves

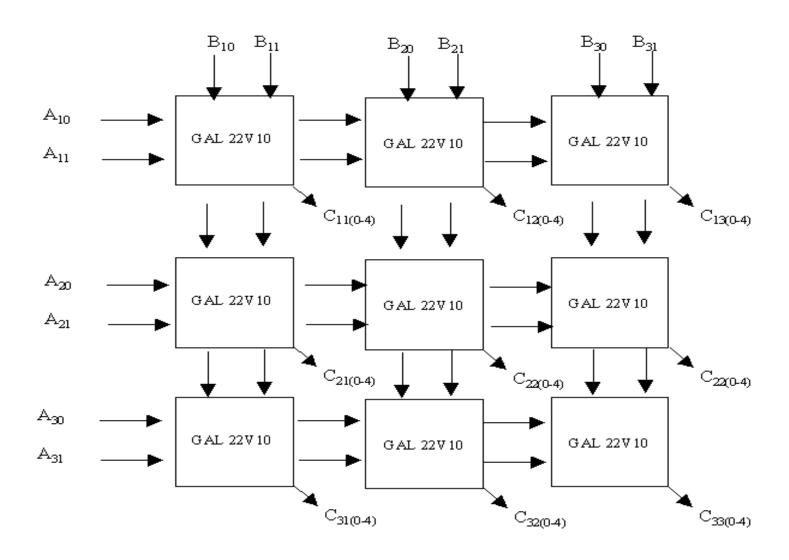
LOGIC DIAGRAMS

MATRIX MULTIPLICATION

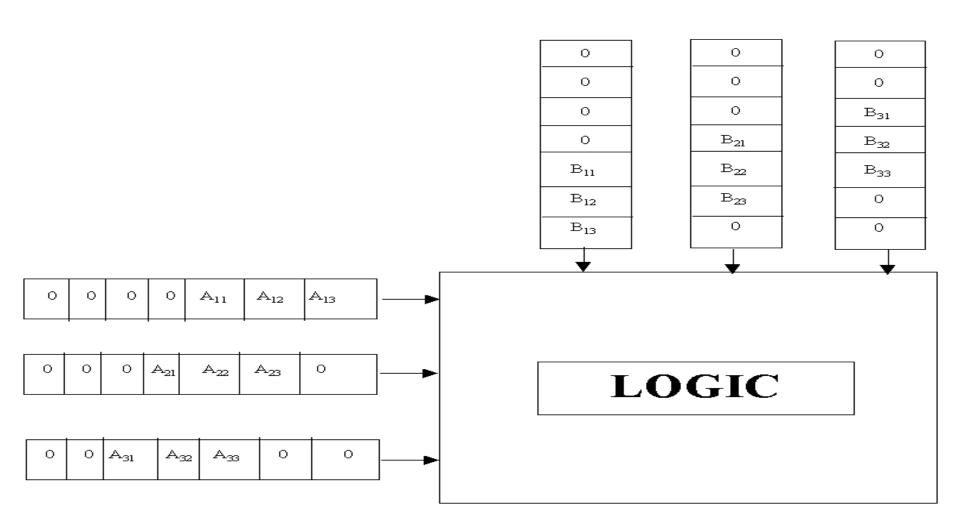
i				Ī								
	A11	A12	A13		В11	B12	B13		C11	C12	C13	
	A21	A22	A23	x	B21	B22	B23	=	C21	C22	C23	
	A31	A32	A33		B31	B32	В33		C31	C32	С33	
				l					L			_

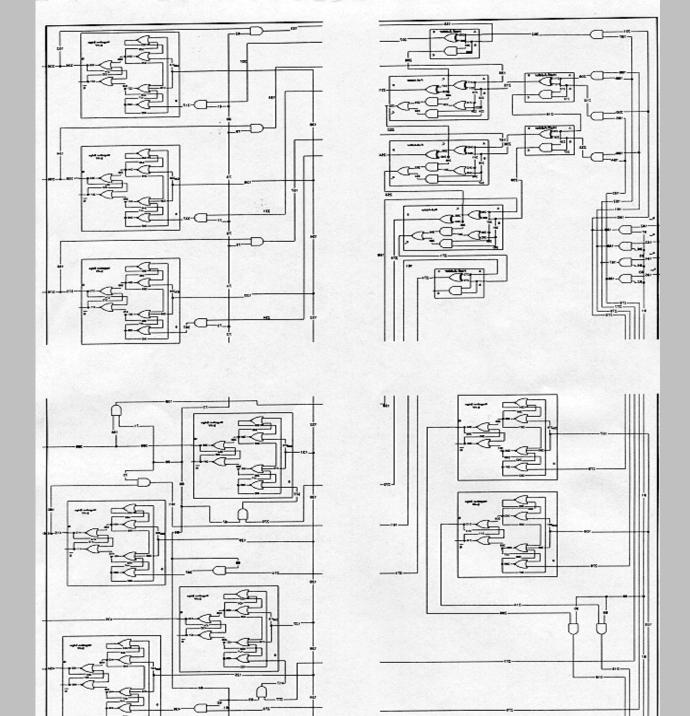
$$\begin{array}{lll} \text{C11} &=& (\text{A11})(\text{B11}) + (\text{A12})(\text{B21}) + (\text{A13})(\text{B31}) \\ \text{C12} &=& (\text{A21})(\text{B11}) + (\text{A22})(\text{B21}) + (\text{A23})(\text{B31}) \\ \text{C13} &=& (\text{A31})(\text{B11}) + (\text{A32})(\text{B21}) + (\text{A33})(\text{B31}) \\ \\ \text{C21} &=& (\text{A11})(\text{B12}) + (\text{A12})(\text{B22}) + (\text{A13})(\text{B32}) \\ \text{C22} &=& (\text{A21})(\text{B12}) + (\text{A22})(\text{B22}) + (\text{A23})(\text{B32}) \\ \\ \text{C23} &=& (\text{A31})(\text{B12}) + (\text{A32})(\text{B22}) + (\text{A33})(\text{B32}) \\ \\ \text{C31} &=& (\text{A11})(\text{B13}) + (\text{A12})(\text{B23}) + (\text{A13})(\text{B33}) \\ \\ \text{C32} &=& (\text{A21})(\text{B13}) + (\text{A22})(\text{B23}) + (\text{A23})(\text{B33}) \\ \\ \text{C33} &=& (\text{A31})(\text{B13}) + (\text{A32})(\text{B23}) + (\text{A33})(\text{B33}) \\ \\ \end{array}$$

2-Bit [3X3] X [3X3] MATRIX MULTIPLIER



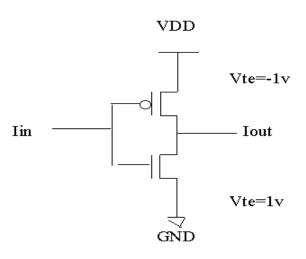
SHIFT REGISTER FEED WITH DELAY





Bp/Bn RATIO

Bp/Bn ASPECT RATIO



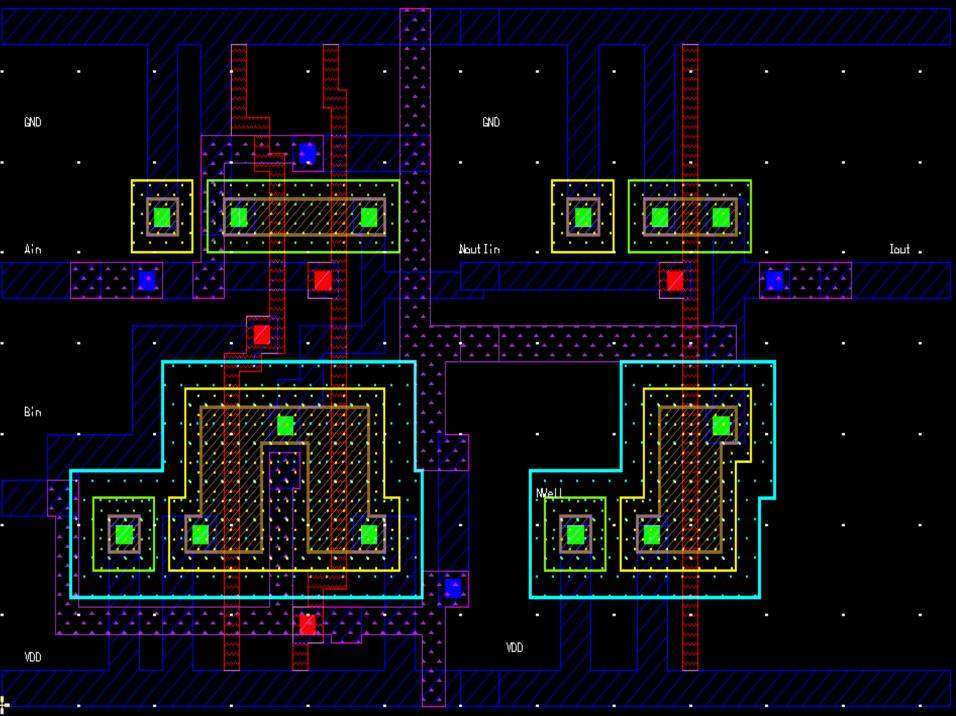
```
Vin
                      Vout =
                                            0.4VDD
Vin
                      2v
           =
Vout
                      2v
Pch
           in
                      Saturation
Nch
           in
                      Saturation
                    \frac{1}{2} u_p \cos^{w}/_1 (Vgs - Vt)^2
Idsp
                    \frac{1}{2} u_n \operatorname{Cox}^{w} / (\operatorname{Vgs-Vt})^2
Idsn
Idsp/Idsn
                                [\frac{1}{2} u_p \text{ Cox } \frac{w}{1} (4)] / [\frac{1}{2} u_n \text{ Cox } \frac{w}{1} (1)]
(w/l)p
                                 4
(w/l)n
                                 1
                      =
```

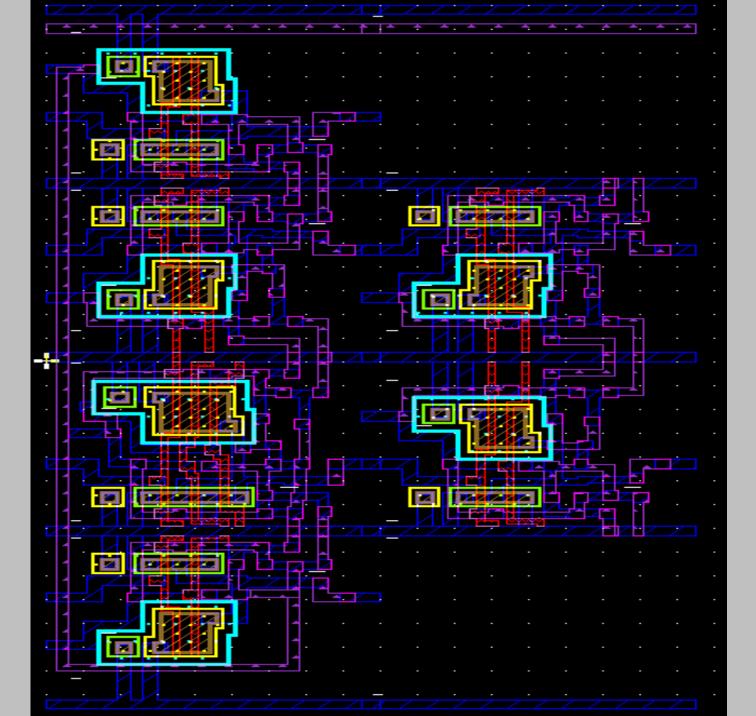
TRANSISTOR LOGIC

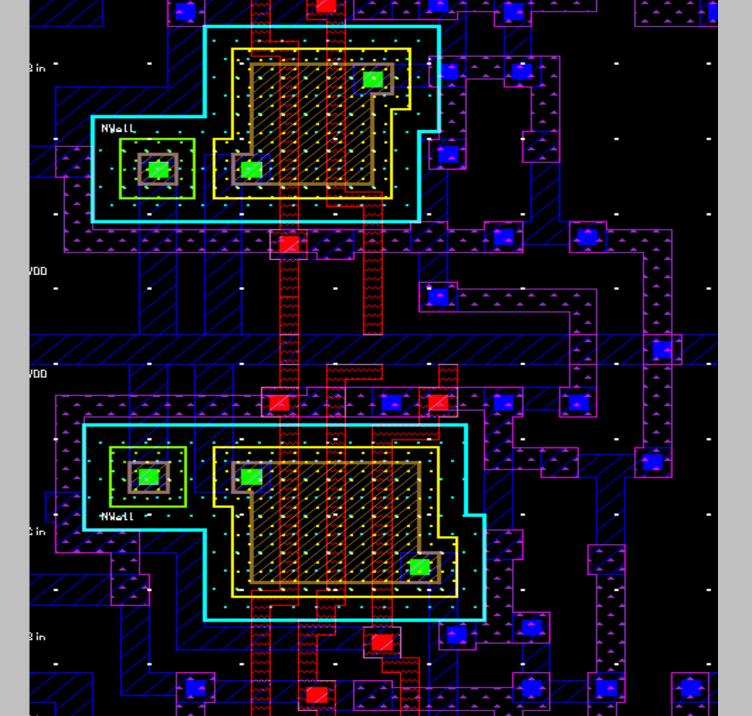
TRANSISTOR LOGIC

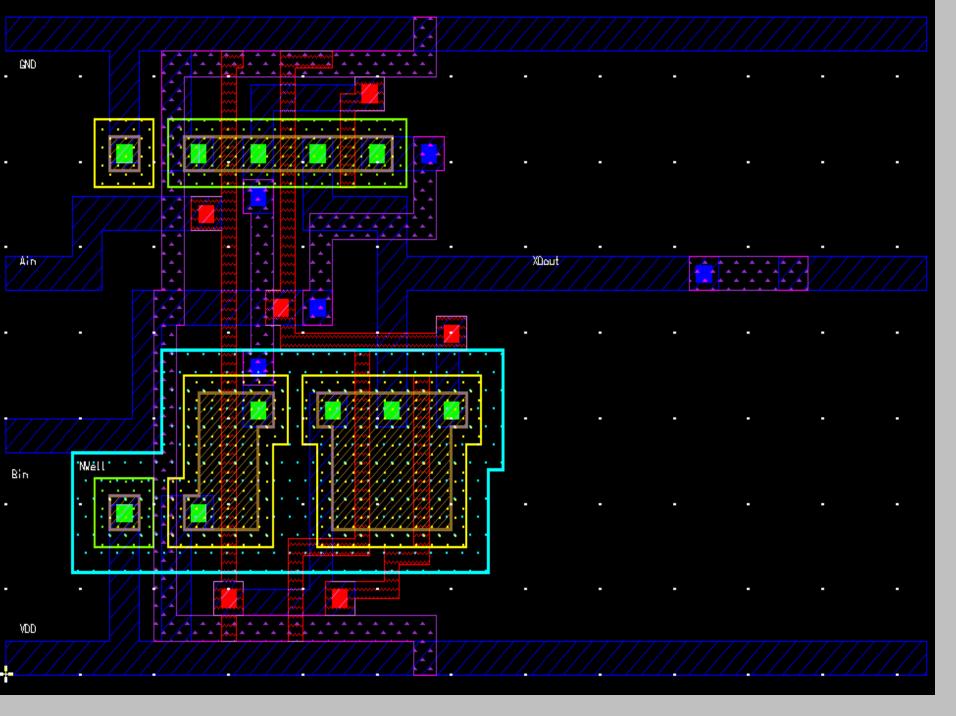
	kt Inv1	GND	VDD	Iin	Iout	1-2.4	···-1 2		
m0 m1	Iout Iout	Iin Iin	GND VDD	GND VDD	N P	1=2.4 1=9.6	w=1.2 w=1.2		
ends.		1111	VDD	VDD	Г	1-5.0	vv—1.2		
· chas									
.subc	kt NANI	D2	GND	VDD	Ain	Bin	Nout		
m0	MIS	Ain	GND	GND	N				
m 1	Nout	Bin	MIS	GND	\mathbf{N}				
m 2	Nout	Ain	VDD	VDD	P				
m3	Nout	Bin	VDD	VDD	P				
.ends NAND2									
.subckt NOR2 GND VDD Ain Bin Nrout									
m0	Nrout		GND	GND	N	141041			
m1	Nrout		GND	GND	N				
m2	Nrout		MPS	VDD	P				
m3	MPS	Ain	VDD	VDD	P				
ends.	NOR2								
	kt AND?		VCC	Ain	Bin	Aout			
x1	0	VCC	Ain	Bin	Iin	NAND	02		
x2	0	VCC	Iin	Aout		Inv1			
enas.	AND2								
.subc	kt OR2	GND	VCC	Ain	Bin	Aout			
x1	0	VCC	Ain	Bin	Iin	NOR2			
x2	0	VCC	Iin	Aout		Inv1			
.ends	OR2								
					- ·	a.	3.77		
	kt NOR3		VDD	Ain	Bin	Cin	NRout		
m0	Nrout		GND	GND	N				
m1 m2	Nrout Nrout		GND GND	GND GND	N N				
m3	Nrout		MPS1		P				
m4	MPS1		MPS2		P				
m4	MPS2		VDD	VDD	P				
	NOR3				_				
.subcl	kt XOR2		VDD	Ain	Bin	About			
$\mathbf{m0}$	AM1	Ain	GND	GND	\mathbf{N}				
m 1	AM1	Ain	VDD	VDD	P				
m 2	About		Ain	VDD	P				
m3	About	Bin	AM1	GND	N				

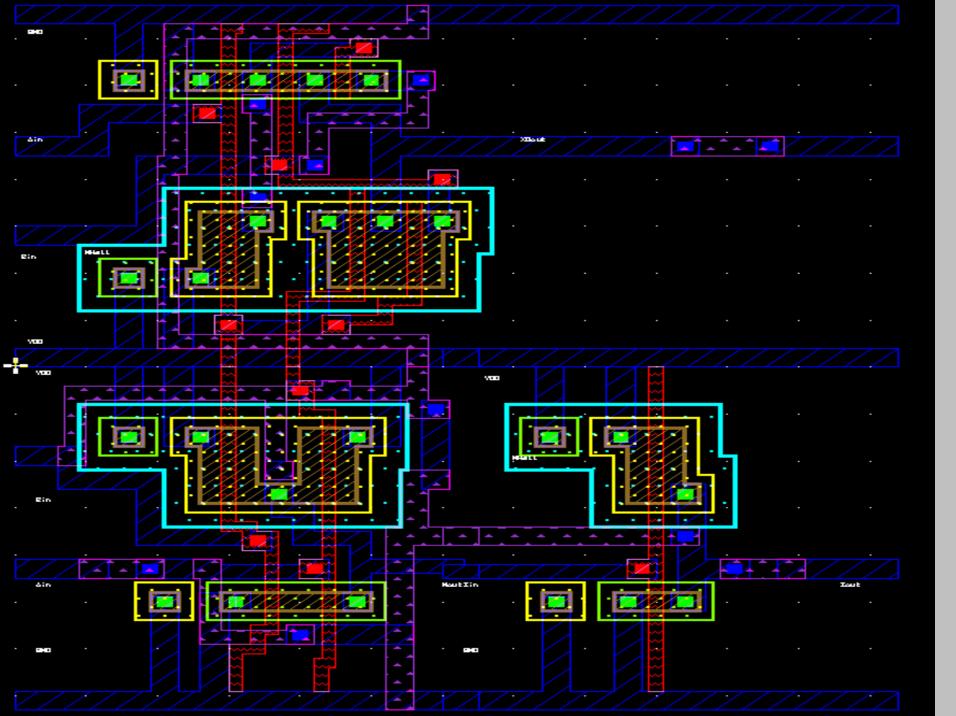
CELLS & SUBCELLS

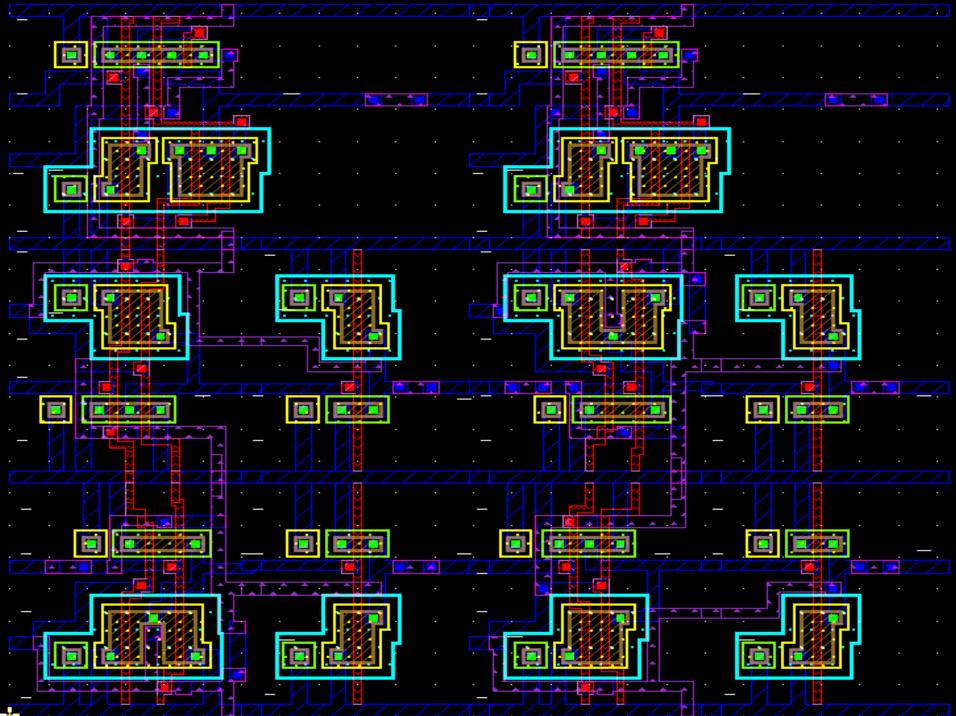


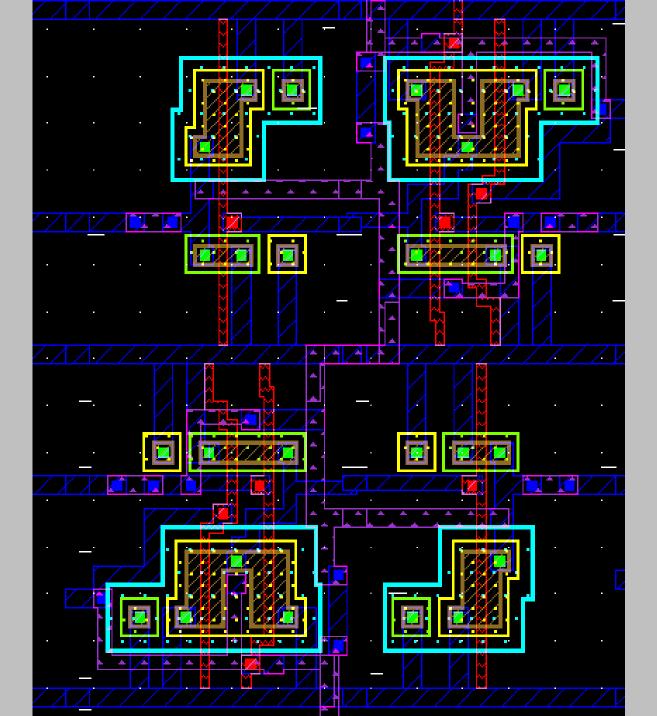


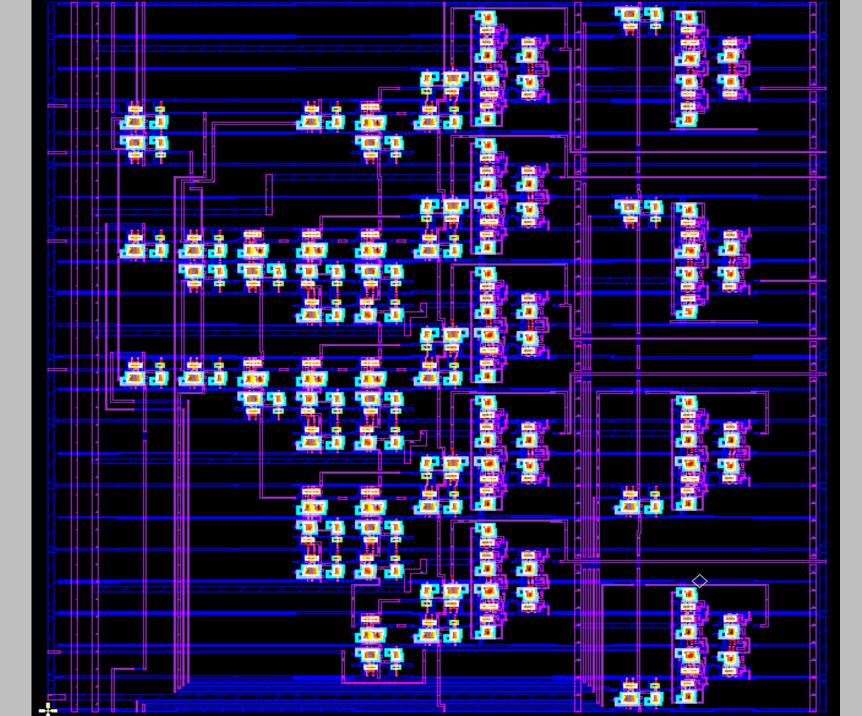


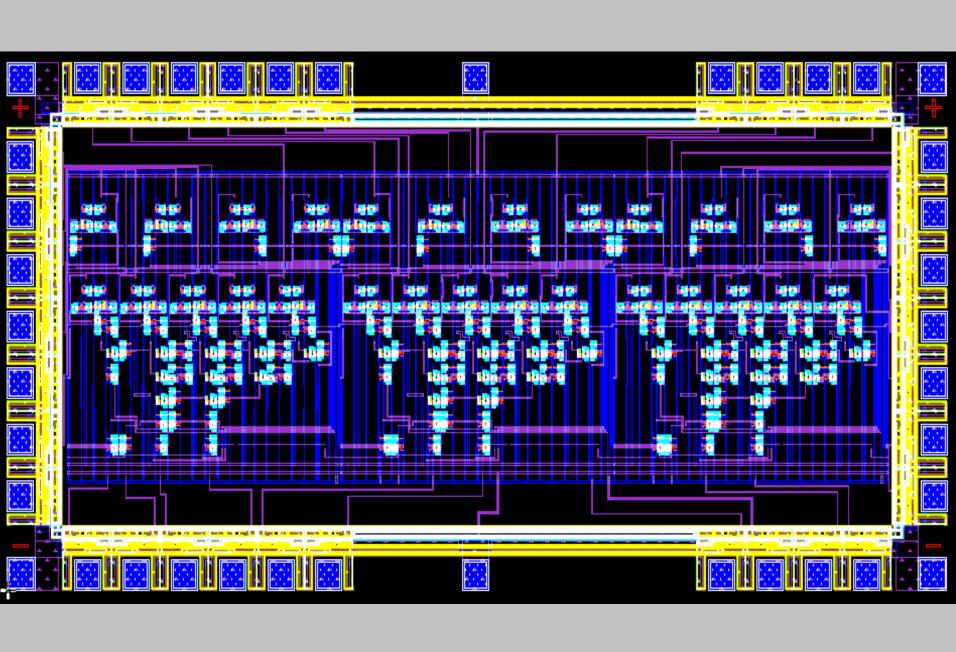


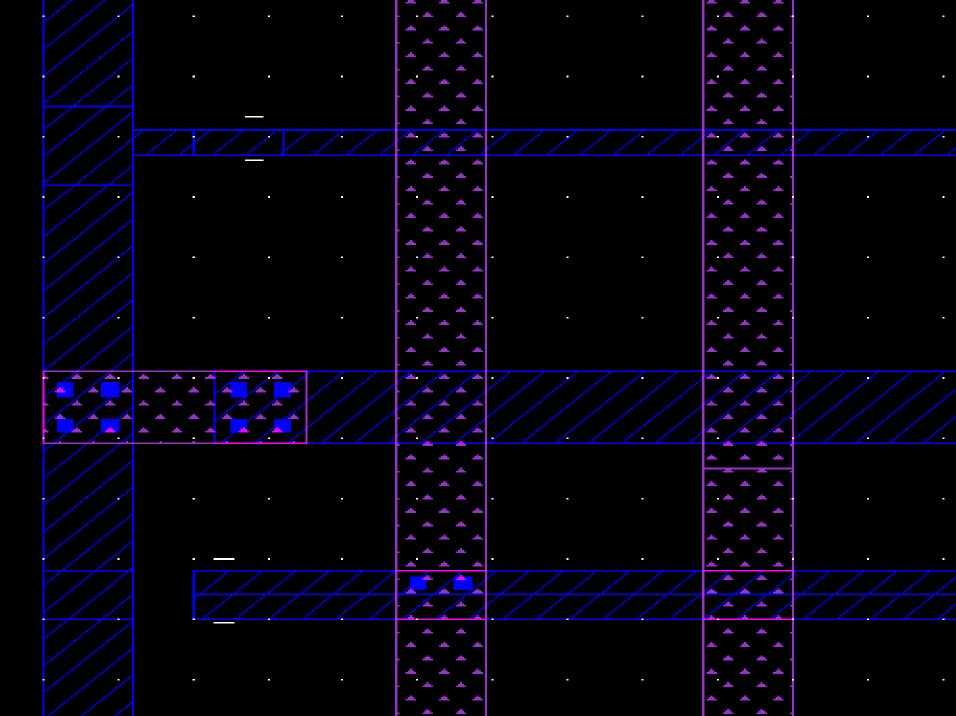












RESULTS

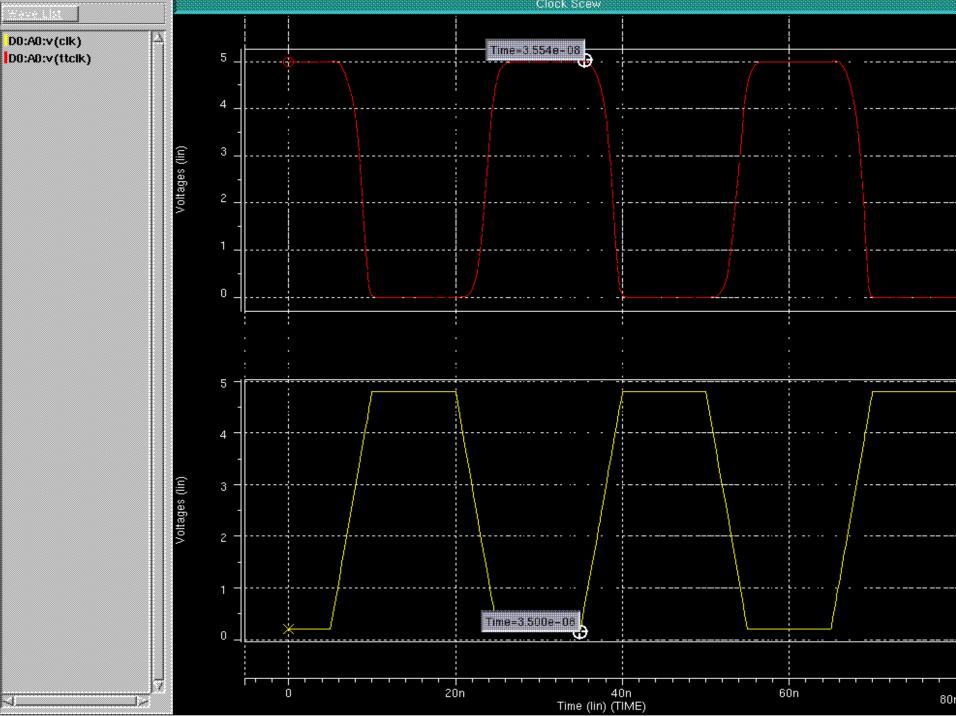
Final Specs:

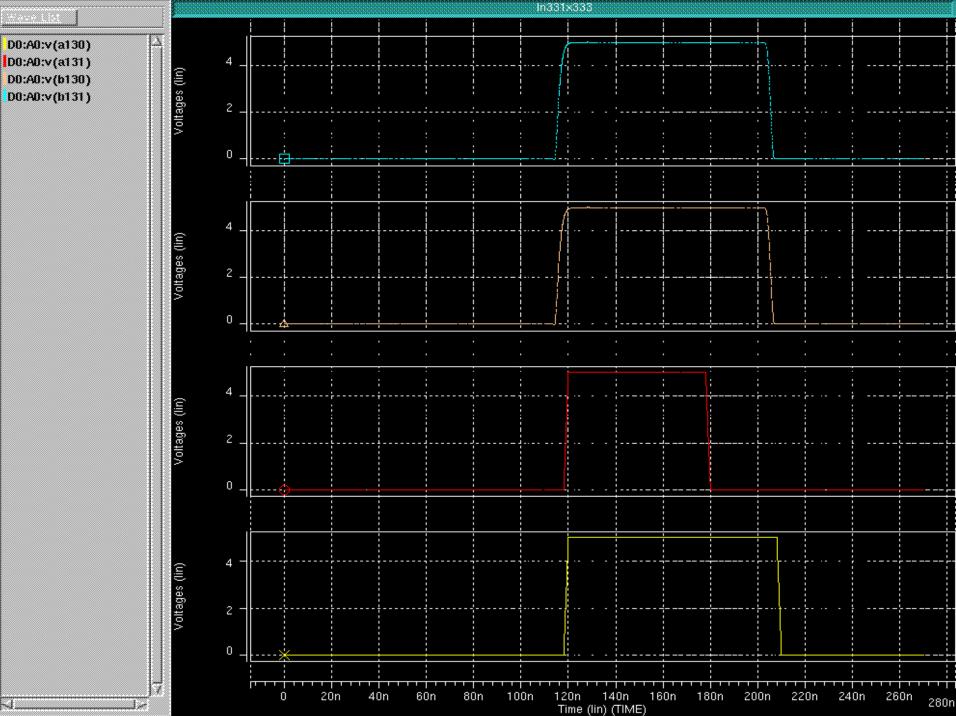
- Clock
 - 5ns Start delay 5ns Rise 5ns Fall 10ns pulse 30ns period
 - skew of 0.54ns
- Transistors 1565
- Capacitors 2292
- Size 1.305mm x 2.872mm

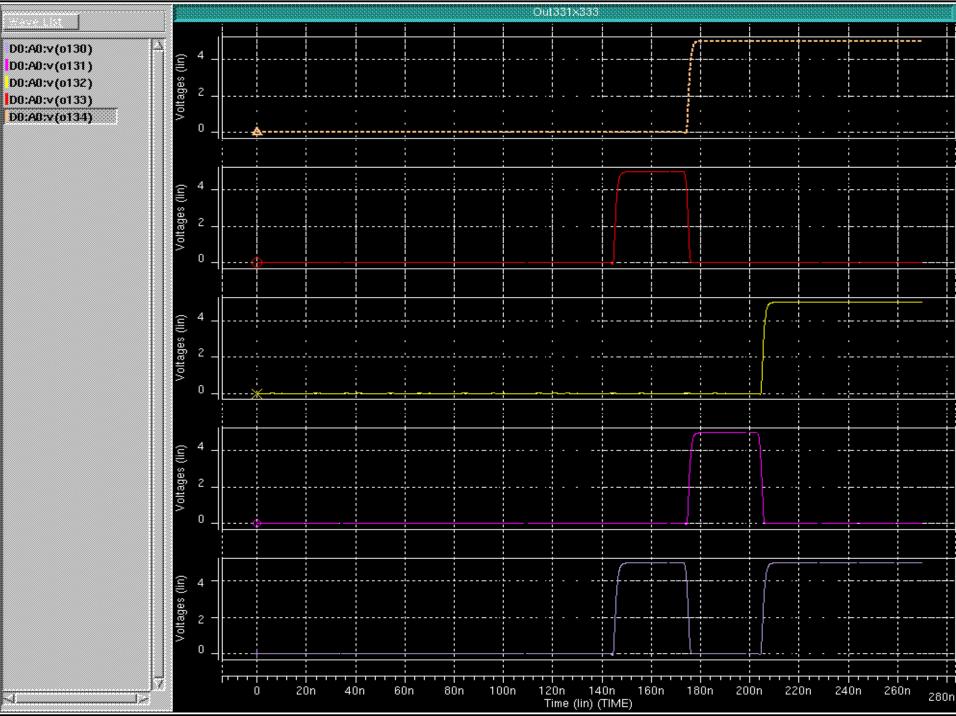
[without pads]

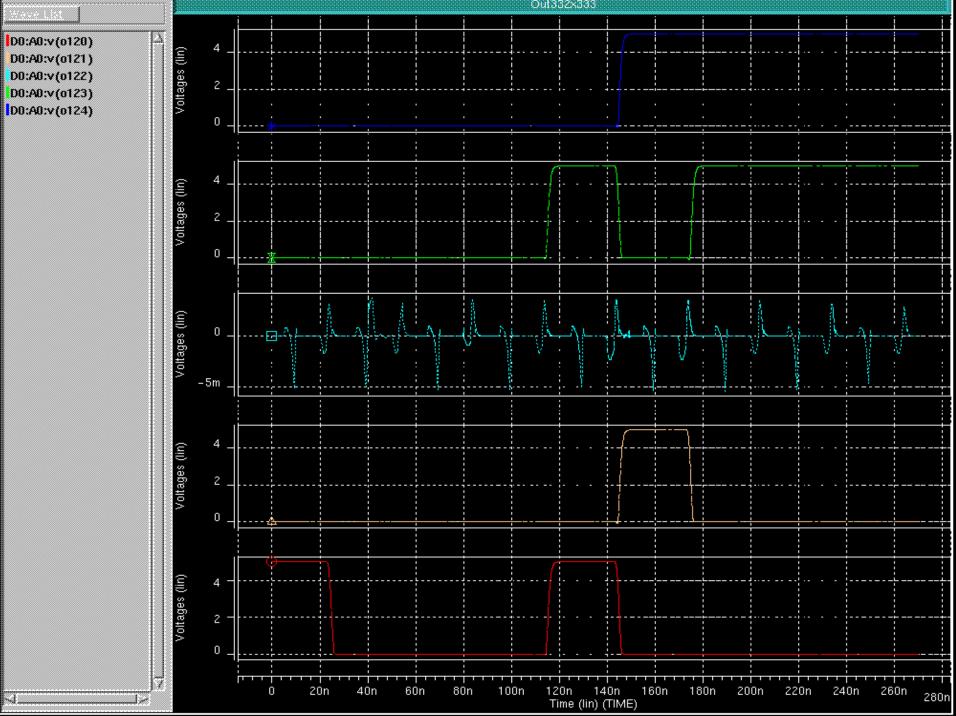
1.850mm x 3.300mm [with pads]

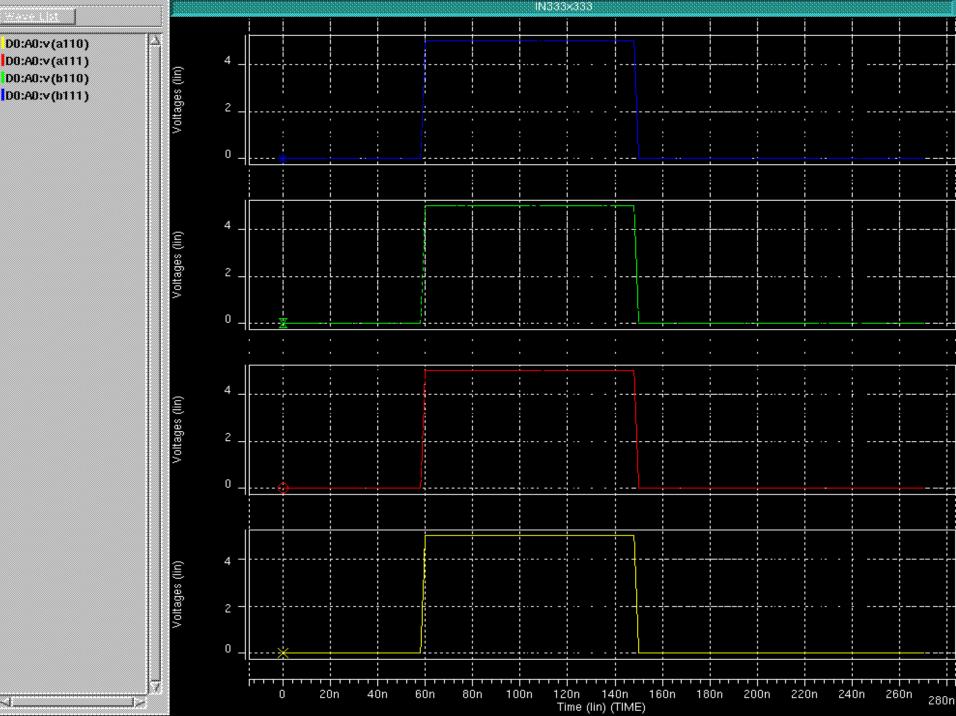
Critical Path Delay - 13ns

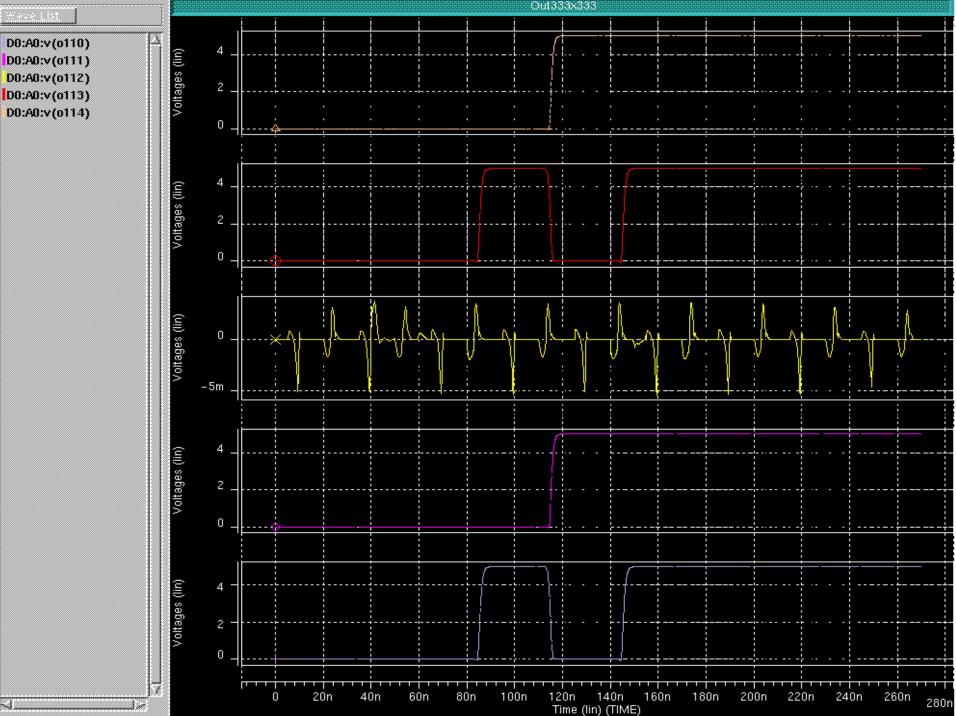


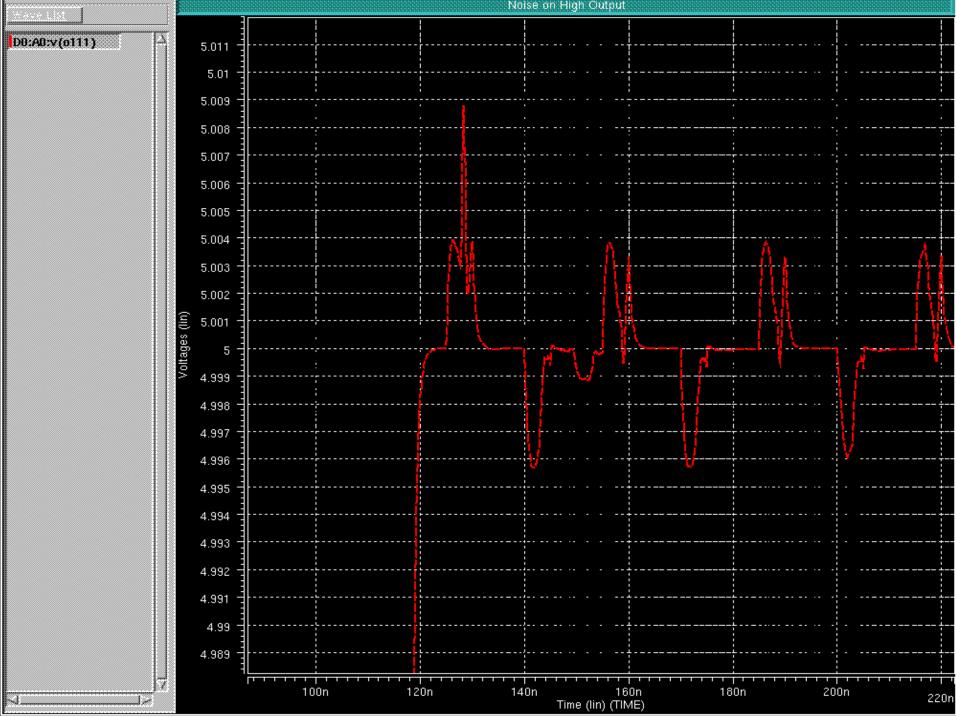


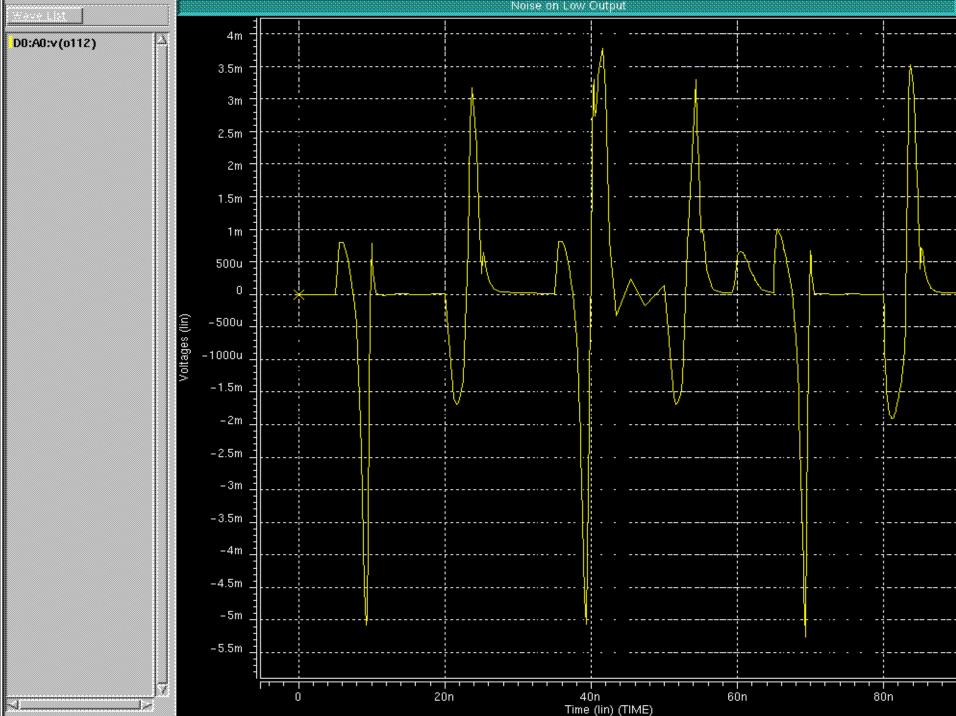












The Future

- Minor modifications for different size matrixes
- Test the chip using Design and Testability algorithms
- Possible use in COE Labs for student testing

The Learning Experience

- How to use IC Graphics
- How to use HSpice
- Tricks to solve problems with both
 - .include subckt_filename
 - Awaves' stack/overlay
- VLSI Chip Design
 - Transistor Characteristics
 - Layout Problem Solving