EE 658-102
VLSI I
Project

2-bit [3x3]x[3x3] Matrix Multiplier

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OVERVIEW

- The Design
- The Steps of the Project
- The Project Results
- The Future
- The Learning Experience
Design

- Design a chip that will complete the task of multiplying a [3x3] matrix by a [3x3] matrix.
- Meet establish design factors
- Use HSpice for the simulation
- Use IC Graphics for the layout
Design Factors

- Limited to 40-pins
- At least 25 MHz
- Limit Complexity
- Low Noise Margin
- Minimal Clock Skew
- 2000um x 2000um
- Asynchronous Reset
Design Decisions

- Input Pulse - 30ns
- Clock - 30ns
  - Initial Delay - 5ns
  - Rise & Fall Time - 5ns
- 3 Multiplier Cells
  - Single Chip - 2-bit $[3\times3] \times [3\times1]$ operation
  - Three Chips - 2-bit $[3\times3] \times [3\times3]$ operation
Steps to the Design

• Design Logic Diagram
  – Box Level
  – Gate Level
• Develop Semiconductor $B_p/B_n$ Ratio
• Design Transistor Logic
• HSpice Simulation
• IC Graphics Layout
  – Gate Subcells
  – Cells [DFF, Full Adder, Half Adder, Multiplier]

• Extract Capacitance File
• HSpice Simulation
• Check Results
• Adjust Layout if necessary
• Graph Results in Awaves
LOGIC

DIAGRAMS
**MATRIX MULTIPLICATION**

\[
\begin{bmatrix}
A_{11} & A_{12} & A_{13} \\
A_{21} & A_{22} & A_{23} \\
A_{31} & A_{32} & A_{33}
\end{bmatrix}
\times
\begin{bmatrix}
B_{11} & B_{12} & B_{13} \\
B_{21} & B_{22} & B_{23} \\
B_{31} & B_{32} & B_{33}
\end{bmatrix}
= 
\begin{bmatrix}
C_{11} & C_{12} & C_{13} \\
C_{21} & C_{22} & C_{23} \\
C_{31} & C_{32} & C_{33}
\end{bmatrix}
\]

\[
C_{11} = (A_{11})(B_{11}) + (A_{12})(B_{21}) + (A_{13})(B_{31})
\]
\[
C_{12} = (A_{21})(B_{11}) + (A_{22})(B_{21}) + (A_{23})(B_{31})
\]
\[
C_{13} = (A_{31})(B_{11}) + (A_{32})(B_{21}) + (A_{33})(B_{31})
\]
\[
C_{21} = (A_{11})(B_{12}) + (A_{12})(B_{22}) + (A_{13})(B_{32})
\]
\[
C_{22} = (A_{21})(B_{12}) + (A_{22})(B_{22}) + (A_{23})(B_{32})
\]
\[
C_{23} = (A_{31})(B_{12}) + (A_{32})(B_{22}) + (A_{33})(B_{32})
\]
\[
C_{31} = (A_{11})(B_{13}) + (A_{12})(B_{23}) + (A_{13})(B_{33})
\]
\[
C_{32} = (A_{21})(B_{13}) + (A_{22})(B_{23}) + (A_{23})(B_{33})
\]
\[
C_{33} = (A_{31})(B_{13}) + (A_{32})(B_{23}) + (A_{33})(B_{33})
\]
2-Bit [3X3] X [3X3] MATRIX MULTIPLIER
SHIFT REGISTER FEED WITH DELAY

LOGIC
Bp/Bn
RATIO
$V_{in} = V_{out} = 0.4V_{DD}$

$V_{in} = 2\nu$

$V_{out} = 2\nu$

$Pch$ in Saturation

$Nch$ in Saturation

$Idsp = \frac{1}{2} u_p C_{ox}^{\gamma/1} (V_{gs} - V_t)^2$

$Idsn = \frac{1}{2} u_n C_{ox}^{\gamma/1} (V_{gs} - V_t)^2$

$Idsp/Idsn = \left[ \frac{1}{2} u_p C_{ox}^{\gamma/1} (4) \right] / \left[ \frac{1}{2} u_n C_{ox}^{\gamma/1} (1) \right]$

$(w/l)p = 4$

$(w/l)n = 1$
TRANSISTOR LOGIC
TRANSISTOR LOGIC

.subckt Inv1 GND VDD Iin Iout
m0 Iout Iin GND GND GND N l=2.4 w=1.2
m1 Iout Iin VDD VDD VDD P l=9.6 w=1.2
.ends Inv1

.subckt NAND2 GND VDD Ain Bin Nout
m0 Mis Ain GND GND GND N
m1 Nout Bin Mis GND GND N
m2 Nout Ain VDD VDD VDD P
m3 Nout Bin VDD VDD VDD P
.ends NAND2

.subckt NOR2 GND VDD Ain Bin Nrout
m0 Nrout Ain GND GND GND N
m1 Nrout Bin GND GND GND N
m2 Nrout Bin MPS VDD VDD P
m3 MPS Ain VDD VDD VDD P
.ends NOR2

.subckt AND2 GND VCC Ain Bin Aout
x1 0 VCC Ain Bin Iin NAND2
x2 0 VCC Iin Aout Inv1
.ends AND2

.subckt OR2 GND VCC Ain Bin Aout
x1 0 VCC Ain Bin Iin NOR2
x2 0 VCC Iin Aout Inv1
.ends OR2

.subckt NOR3 GND VDD Ain Bin Cin NRout
m0 Nrout Ain GND GND GND N
m1 Nrout Bin GND GND GND N
m2 Nrout Cin GND GND GND N
m3 Nrout Cin MPS1 VDD P
m4 MPS1 Bin MPS2 VDD P
m4 MPS2 Ain VDD VDD VDD P
.ends NOR3

.subckt XOR2 GND VDD Ain Bin About
m0 AM1 Ain GND GND GND N
m1 AM1 Ain VDD VDD P
m2 About Bin Ain VDD P
m3 About Bin AM1 GND N
CELLS & SUBCELLS
RESULTS
Final Specs:

- **Clock**
  - 5ns Start delay 5ns Rise 5ns Fall 10ns pulse 30ns period
  - skew of 0.54ns
- **Transistors** - 1565
- **Capacitors** - 2292
- **Size** - 1.305mm x 2.872mm [without pads]
  - 1.850mm x 3.300mm [with pads]
- **Critical Path Delay** - 13ns
The Future

- Minor modifications for different size matrixes
- Test the chip using Design and Testability algorithms
- Possible use in COE Labs for student testing
The Learning Experience

- How to use IC Graphics
- How to use HSpice
- Tricks to solve problems with both
  - .include subckt_filename
  - Awaves’ stack/overlay
- VLSI Chip Design
  - Transistor Characteristics
  - Layout Problem Solving