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Ge MOS Capacitors with Thermally Evaporated HfO_2 as Gate Dielectric

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We have investigated the characteristics of thermally evaporated hafnium oxide (HfO_2) films on germanium substrates. Surface roughness of the HfO_2 film was studied by scanning electron microscopy. The presence of crystalline GeO_2 was evident from X-ray diffraction results on as-deposited films. Capacitance–voltage (C-V) and current–voltage (I-V) measurements of the as-deposited metal-oxide semiconductor (MOS) capacitors demonstrated a hysteresis of 2.3 V and leakage current density of 10 A/cm^2 at 1 V, respectively. Annealing of these films at two different temperatures of 500 and 550°C in N_2 ambience reduced the hysteresis to 0.9 V and the leakage current density by five orders of magnitude. Observed increment of equivalent oxide thickness (EOT) after annealing indicates growth of an interfacial layer. The composition of film evaluated by X-ray photoelectron spectroscopy for annealed devices further confirms the increase of interfacial layer. Interface state density, estimated using the conductance method after 550°C annealing, was 5.1×10^{12} cm^{-2} eV^{-1}.
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Recently deposition of high-*k* dielectrics on Ge substrate has gained considerable research interest in complementary metal-oxide-semiconductor (CMOS) technology. Originally transistors were fabricated on Ge substrate, but lack of stable Ge native oxide has been an obstacle in CMOS device realization in Ge. Therefore, for decades silicon has been used in CMOS technology due to better qualities of its native oxide such as low leakage current, low interface state density, and good thermal stability.

But with device dimensions scaling down to nanometer range and subsequent gate oxide scaling, the leakage current density in SiO_2 is much higher than 2 mA/cm^2, which is the maximum permissible limit for low-power application.[1] Therefore, high-dielectric-constant materials with higher physical thickness are being used to limit the leakage current while maintaining the capacitance values of the scaled devices. HfO_2 seems to be the most promising candidate to replace silicon dioxide because of its high dielectric constant (~20), relatively large bandgap (5.68 eV), and thermodynamic stability with Si interface and poly-Si gate. However, severe surface carrier mobility degradation has been observed in metal oxide semiconductor (MOS) devices using HfO_2 as the gate dielectric.[2]

Changing the substrate from silicon to germanium could be a possible solution to surface carrier mobility degradation as Ge has higher carrier mobility in comparison to Si. Devices using high-*k* gate dielectrics deposited directly on Ge substrate have shown some promise.[3] Chui et al. reported Ge MOS devices with atomic layer deposited (ALD) HfO_2.[4] Ge MOS capacitors using CVD HfO_2 were reported by Bai et al.[5] Germanium-on-insulator devices with Al_2O_3 gate dielectrics have also been demonstrated.[6] In this work we explored the deposition of HfO_2 film on Ge by thermal evaporation as the HfO_2 films deposited by the same process on Si substrate has produced excellent devices.[7] The MOS capacitors formed with thermally evaporated HfO_2 on germanium substrate demonstrated similar characteristics compared to other deposition techniques.

Experimental

Thin films of HfO_2 of physical thickness 5 and 10 nm were deposited on 2-in. n-type germanium substrates with doping concentration of 1.5×10^{15} cm^{-3} by thermal evaporation. Oxygen was added at constant partial pressure during the deposition to form HfO_2. During the deposition substrate was kept at room temperature. Prior to deposition germanium substrate was dipped into HF solution to remove the native oxide. Thickness of the films was measured by quartz crystal microbalance. After HfO_2 deposition samples were annealed at 500 and 550°C in N_2 environment for 20 min. The annealing temperature was kept below 600°C as diffusion of germanium in the HfO_2 has been observed above 600°C annealing.[8] Various sizes of Al gate electrode were formed by photolithography. Back-side contact by depositing Al on the wafer ensured a reduction in contact resistance. Samples were subjected to 350°C forming gas anneal (FGA: N_2/H_2 5%) after the aluminum deposition.

The devices were physically characterized using X-ray diffraction (XRD), scanning electron microscopy (SEM), and X-ray photoelectron spectroscopy. Capacitance–voltage (C-V) and current–voltage (I-V) characterizations were performed with a Boonton Capacitance meter and an HP 4156B semiconductor parameter analyzer.

Results and Discussion

Physical characterization.— Figure 1a shows the SEM image of as-deposited HfO_2 film on the Ge substrate. The surface of the HfO_2 film shows island-like morphology. The film seems to have a rough surface and a nonuniform deposition. A similar type of surface structure has been reported for as-deposited HfO_2 film on germanium substrates by Wu et al.[9] using atomic force microscopy (AFM), where surface roughness was attributed to the presence of GeO_2 interfacial layer. After 500°C anneal in N_2 environment the film seems to be smooth without any significant surface roughness, as shown in Fig. 1b. This suggests that the film went through structural transformation during annealing.

The as-deposited HfO_2 film was analyzed by XRD for structural analysis. Figure 2 shows the XRD spectra of as-deposited HfO_2 film. A peak was observed at an angle of 66.7° corresponding to GeO_2. No other peaks were detected, indicating the desired amorphous nature of the dielectric film. The presence of crystalline GeO_2 has also been detected at the interface[10] by other deposition techniques, as GeO_2 induced by gaseous O_2 is found to be polycrystalline.[11] Therefore, it is possible that during thermal evaporation, GeO_2 formation took place when oxygen came in contact with the Ge substrate. Due to the nonuniformity of GeO_2 induced by the oxidation of Ge,[11] hafnium oxide films deposited on top of this nonuniform interfacial layer also exhibited nonuniform characteristics, as seen in the SEM image (Fig. 1a).

As the SEM images after the 500°C annealing show significant

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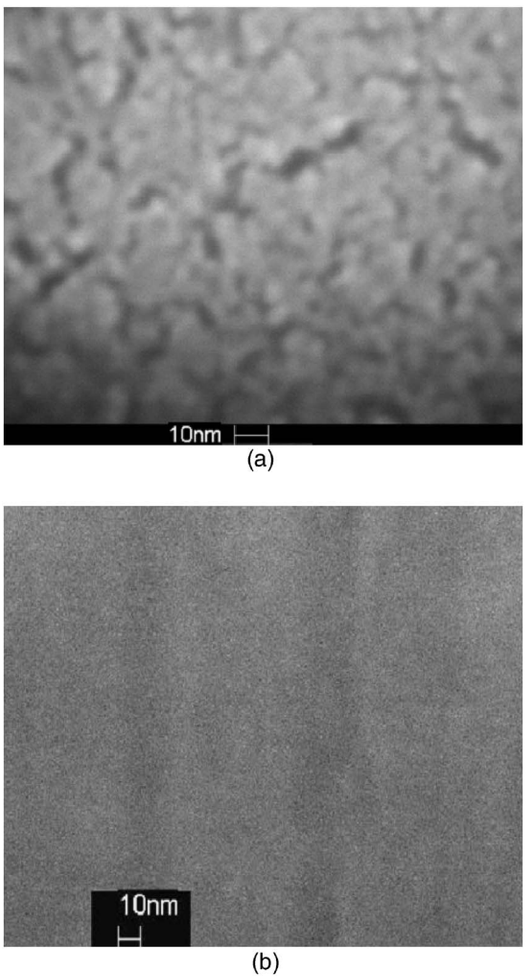

Figure 1. Top down SEM image of the thermally evaporated HfO_2 (a) as deposited and (b) after 500°C annealing on top of Ge substrate.

improvement on the uniformity of the dielectric film, X-ray photoelectron spectroscopy (XPS) was done to study the effect of annealing on the composition of gate dielectric. Figure 3a shows the XPS spectrum of the Hf 4f peak for HfO_2. Also, Ge 2p3 peaks were detected at 1220.9 eV and identified for GeO_2, which shows the incorporation of Ge in HfO_2. No signal was observed for Ge or

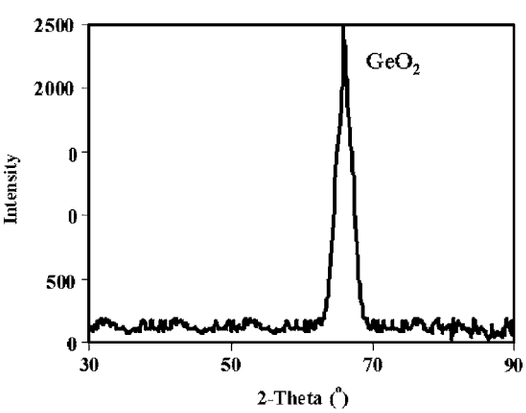

Figure 2. XRD spectra of the as-deposited films. The peak indicates the presence of crystalline GeO_2.

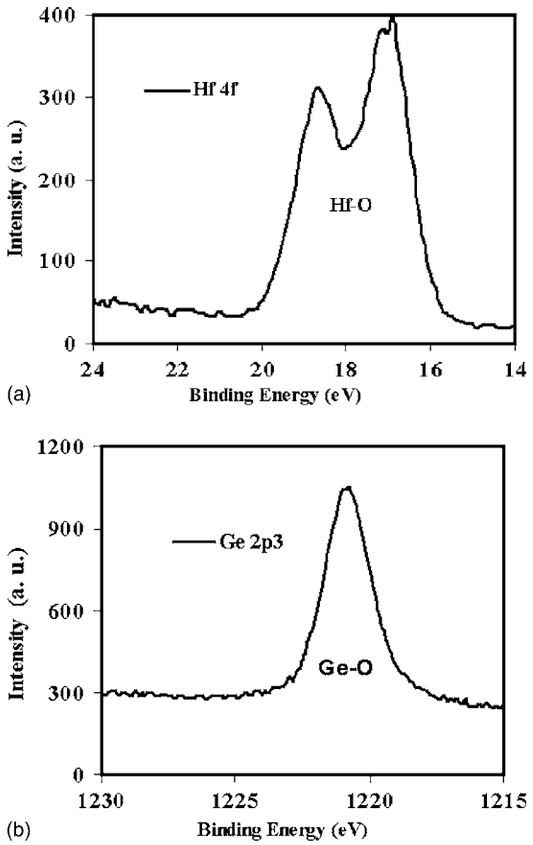

Figure 3. XPS spectra of (a) Hf 4f and (b) Ge 2p3 for HfO_2 films after 500°C annealing.

Ge–Hf bond, indicating that the dielectric film is composed of both GeO_2 and HfO_2. Similar film composition has been observed for the HfO_2 films deposited by other techniques[10] on Ge substrate without any surface treatment.

Electrical characterization.— C-V characteristics of the devices with as-deposited 5-nm HfO_2 films did not demonstrate typical MOS capacitor behavior. A linear dependence was observed for $1/C^2$ vs applied gate voltage (V), as shown in Fig. 4. This suggests

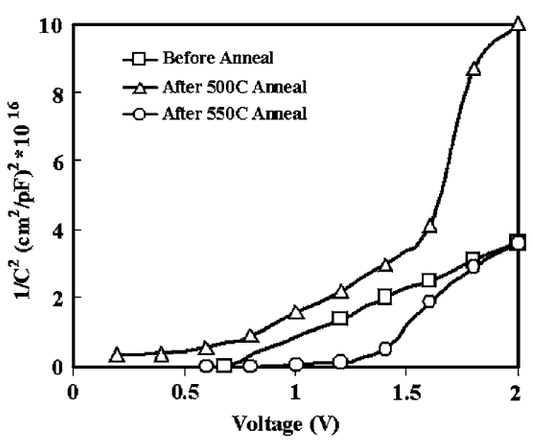

Figure 4. $1/C^2$ vs applied gate voltage for MOS capacitors with 5-nm HfO_2 films before anneal and after anneal. Barrier height, calculated from the intercept on the voltage axis, is in the range of 0.38–0.68 V.

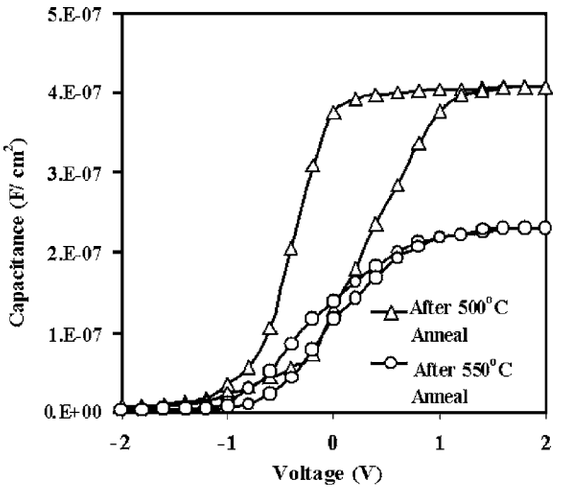

Figure 5. C-V characteristics of devices with 5-nm HfO_2 films after annealing at 500 and 550°C in N_2 environment. Hysteresis reduced to 0.2 V while EOT and V_{FB} increased to 10.5 nm and 1.23 V, respectively, after 550°C annealing.

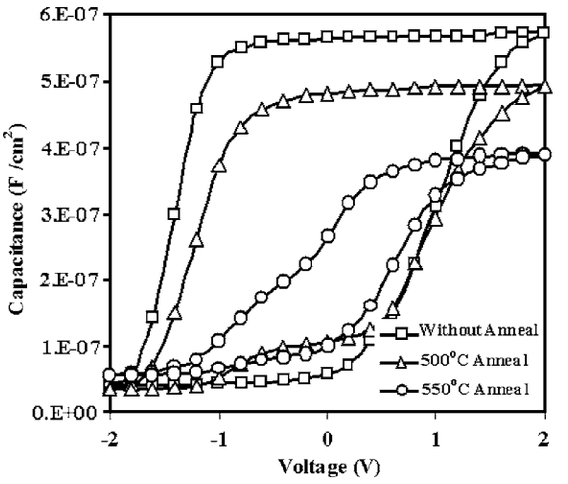

Figure 6. C-V characteristics of devices with 10-nm HfO_2 films. Hysteresis reduced to 0.9 V while EOT and V_{FB} increased to 9.3 nm and 0.73 V, respectively, after 550°C annealing.

a rectifying behavior for as-deposited devices, implying that the as-deposited films were either hafnium-rich at the Ge/HfO_2 interface or they were rather nonuniform. The barrier height calculated from a $1/C^2$-V plot of devices with as-deposited HfO_2 film was in the range of 0.38–0.68 V. After annealing these films at 500 and 550°C in N_2 ambience transformation of gate dielectric could be observed, as nonlinear dependence was seen for $1/C^2$ on the applied gate voltage (V) (Fig. 4), possibly due to stiochiometric changes occurring in the films during the annealing.

After 500°C annealing, 0.7 V of hysteresis is observed which reduced to 0.2 V for films annealed at 550°C, shown in Fig. 5. This is comparable to the hysteresis obtained in HfO_2 films deposited by other techniques such as ALD[4] and reactive atomic beam deposition[12] with no surface treatment. This significant reduction in hysteresis in our case shows an improvement in gate dielectric, but at the same time a reduction in accumulation capacitance is also observed at 550°C annealing as compared to 500°C annealing. Because GeO_2 had been detected by XRD analysis, it is possible that during high-temperature annealing GeO_2 interacted with HfO_2 and formed an interfacial layer of hafnium germinate.[10] XPS results also show that dielectric film is a combination of HfO_2 and GeO_2. The dielectric constant of good GeO_2 is ~3, implying that a significant interfacial layer of GeO_2 has a much lower capacitance in comparison to HfO_2 film. This low capacitance in series with high capacitance of HfO_2 film would bring down effective accumulation capacitance of the gate stack. As the EOT was calculated from the accumulation capacitance of the total gate stack, it resulted in a higher EOT. EOT further increased to 10.5 nm with 550°C annealing, confirming interaction of the interfacial layer with the gate dielectric. After 500°C annealing, the flatband voltage (V_{FB}) shift observed in these devices was 0.36 V, which further shifted to 1.23 V after 550°C annealing. This positive shift in V_{FB} indicates the induction of negative charge in the film at high-temperature annealing.

C-V curves for devices with 10-nm as-deposited HfO_2 films showed a rather large hysteresis of 2.3 V and an EOT of 6.6 nm, as shown in Fig. 6. After annealing the films at 500°C, a small decrease in hysteresis (2.1 V) was observed but EOT was increased to 7.5 nm. Annealing at 550°C reduced the hysteresis significantly to 0.9 V but increased the EOT further to 9.3 nm. This reduction in hysteresis indicates improvement in gate dielectric characteristics, but increase in EOT indicates formation of a thicker interfacial layer with increase in annealing temperature. Chen et al.[12] observed the identical behavior where EOT was increased and hysteresis was decreased with 550°C annealing. Also, 5-nm devices exhibited similar behavior due to possible interaction of interfacial GeO_2 with the HfO_2 film at higher temperature annealing, which is confirmed by the XPS results shown in Fig. 3a and b. Flatband voltage shifted (ΔV_{FB}) from −0.77 V before annealing to −0.35 V after 500°C annealing indicates that the positive charge present in as-deposited HfO_2 films is being compensated during the annealing, hence pushing the V_{FB} toward ideal value. After 550°C annealing, ΔV_{FB} further increased to 0.73 V, indicating the generation of more negative charge in the gate dielectric.

The leakage current density in devices with 5-nm HfO_2 films is shown in Fig. 7. The leakage current density of devices with as-deposited HfO_2 film is 10 A/cm^2, which is slightly higher than the reported leakage current[10,12] for as-deposited HfO_2. This high leakage current indicates the presence of a large density of oxide traps in the film, which resulted in trap-assisted tunneling.[13] After the annealing of these HfO_2 films at 500°C, leakage current reduced to 1 A/cm^2 at 1 V, but annealing at 550°C resulted in further reduction of leakage current by 5 orders of magnitude, which is lower than the leakage current obtained in HfO_2 films deposited on Ge substrate by other techniques such as metallorganic chemical vapor

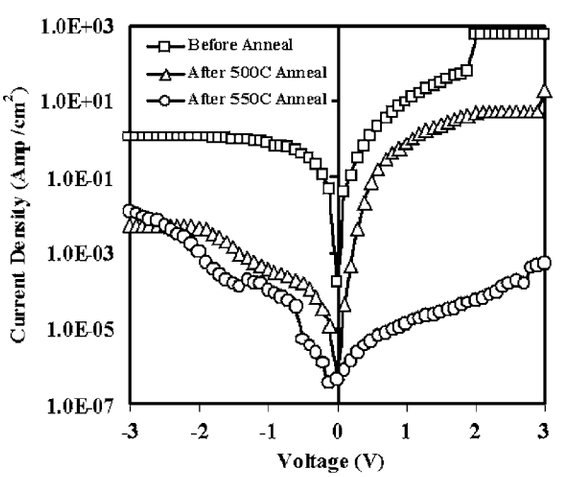

Figure 7. Leakage current density of the MOS capacitors with 5-nm HfO_2 films. After 550°C annealing leakage current reduced to ~10^{-5} A/cm^2.

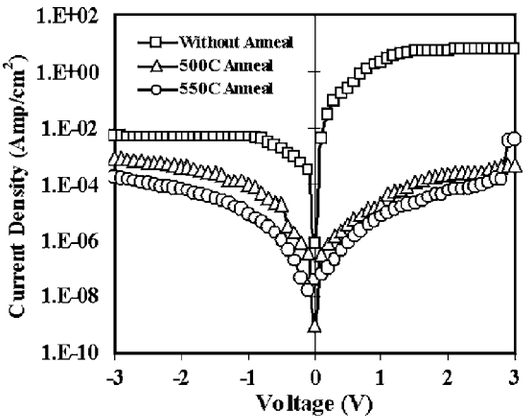

Figure 8. Leakage current density of the MOS capacitors with 10-nm HfO_2 films. After 550°C annealing leakage current reduced to $\sim 10^{-5}$ A/cm^2.

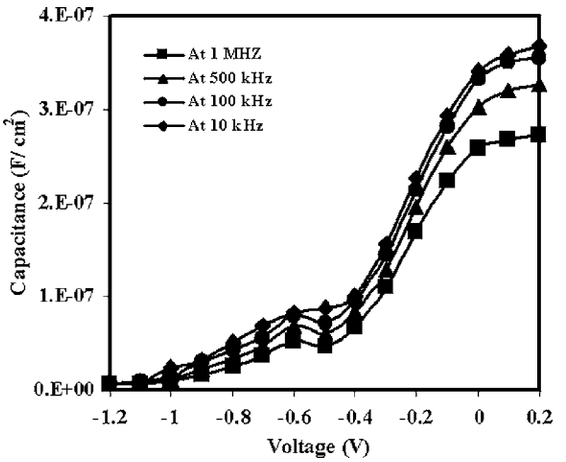

Figure 9. C-V characteristics of Ge/HfO_2 (5 nm)/Al MOS capacitors at different frequencies after 550°C annealing.

deposition (MOCVD), reactive atomic beam deposition, etc.[10,12] As higher temperature (>600°C) annealing makes the HfO_2 films crystalline, 550°C anneal seems to be a good annealing temperature to bring the oxide trap density to its lowest possible inherent level for 5-nm devices, but an increase in EOT due to the interaction of interfacial layer as observed from C-V characteristics remains a problem.

Figure 8 shows the leakage current density of MOS capacitors with 10-nm HfO_2 films. The leakage current obtained for as-deposited HfO_2 films was lower by 2 orders of magnitude as compared to the 5-nm HfO_2 films, which is expected due to higher thickness of the gate dielectric. After annealing these films at 500 and 550°C in N_2 environment, leakage current reduced significantly to $\sim 10^{-5}$ A/cm^2 for both annealing conditions. Even though significant improvement can be noticed between 500 and 550°C annealing for 5-nm devices (Fig. 7), not much improvement was observed for the two annealing temperatures used for 10-nm devices (Fig. 8). Almost identical leakage current was obtained for both 5- and 10 -nm HfO_2 films after 550°C annealing, implying the higher concentration of oxide traps in 10-nm HfO_2 films.

An increase in EOT was observed for both 5- and 10-nm HfO_2 films after the annealing, but for 5-nm films EOT was found to be thicker than physical thickness while in the case of 10 nm it was lower than the actual thickness of the film. Assuming that the thickness of the interfacial layer grown during the deposition was the same for both films, the fraction of this interfacial layer in EOT would be greater in 5-nm film as compared to 10-nm film. With further growth of the interfacial layer during the annealing, its fraction in total gate dielectric thickness also increases in 5-nm films than 10-nm films, consequently reducing the fraction of HfO_2. This reduction in HfO_2 thickness could be the possible reason for the positive shift observed in V_{FB} for both films. Also, as similar leakage current was observed for both 5-nm and 10-nm films after 550°C annealing, it could be because of the improvement in oxide quality of 5-nm HfO_2 film.

We have investigated the effect of HfO_2/GeO_2 interface on device performance using conductance measurements. C-V characteristics of MOS capacitors with 5-nm HfO_2 film were taken at different frequencies, as shown in Fig. 9. The dispersion observed in the accumulation region is due to the substrate series resistance, R_s, which mainly affects the high-frequency C-V curve. Kinks seen in the inversion region at high frequency imply the existence of fast surface states near the valence band E_v. The difference between 10- and 100-kHz C-V curves in the same region indicates the presence of slow interface states as well.[3]

In contrast to C-V characteristics of 5-nm HfO_2 films, significant dispersion can be observed in the flatband regime for 10-nm HfO_2 films, shown in Fig. 10. Combined with hysteresis (Fig. 6) and leakage current (Fig. 8) observed in these films, this dispersion suggests that more bulk oxide traps are present in these films. With the reduction in frequency, kinks start appearing in the inversion region, indicating the presence of slow interface states near the valence band.[3] Peaks observed in G-V plots in these films (Fig. 11) are broader compared to 5-nm HfO_2 films (Fig. 12), indicating a large distribution of the energy levels of interface states in the germanium bandgap.[14]

Interface state densities (D_{it}) extracted from the peak of Gp/ω vs frequency plot (Fig. 13) are 3.1×10^{13} cm^{-2} eV^{-1} and 5.1×10^{12} cm^{-2} eV^{-1} for 5- and 10-nm HfO_2 films, respectively, comparable to the D_{it} values obtained in HfO_2 films deposited by other techniques[12,15] on Ge. The interface state density is higher with a reduced bulk oxide trap concentration in 5-nm HfO_2 film, indicating that the quality of gate dielectric film has improved after 550°C annealing in N_2 environment, whereas the GeO_2/HfO_2 interface degraded. This suggests that the GeO_2-type interfacial layer has increased further.

Different groups have reported similar characteristics of HfO_2 films deposited on Ge substrate. Films deposited directly on Ge

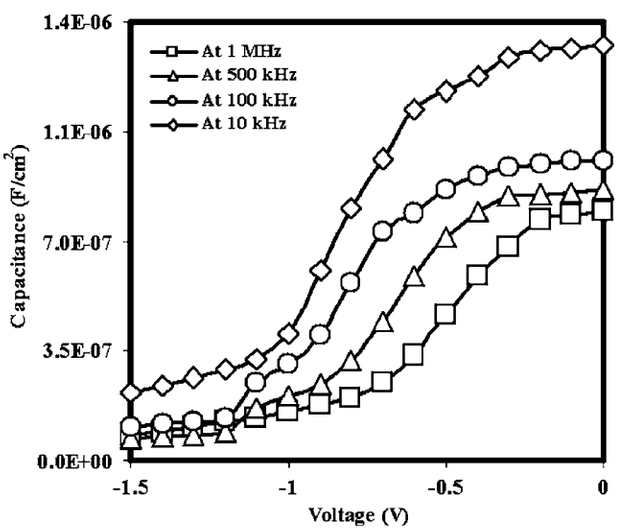

Figure 10. C-V characteristics of Ge/HfO_2 (10 nm)/Al MOS capacitors at different frequencies after 550°C annealing.

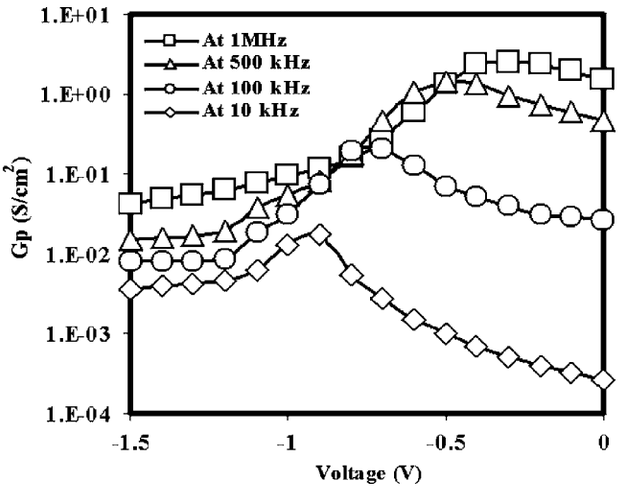

Figure 11. G-V characteristics of Ge/HfO_2 (10 nm)/Al MOS capacitors at different frequencies after 550°C annealing.

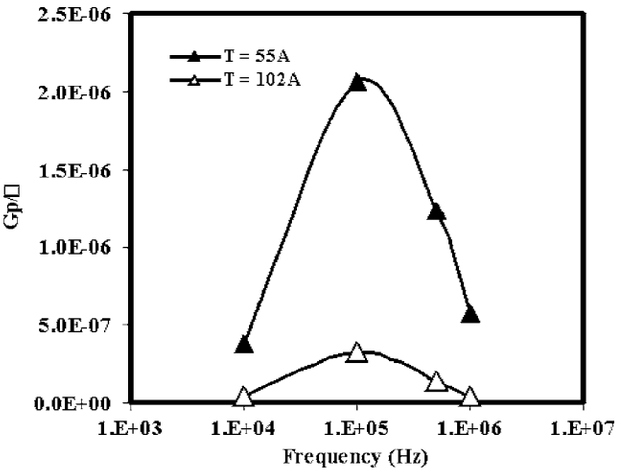

Figure 13. Gp/ω vs ω for both 5-nm and 10-nm HfO_2 films after 550°C annealing. Interface state densities (D_{it}) calculated from the peak of Gp/ω are 3.1×10^{13} and 5.1×10^{12} cm^{-2} eV^{-1} for 5- and 10-nm HfO_2 films, respectively.

without any surface preparation show large hysteresis along with high leakage current[12] after postdeposition anneal. EOT also increased after annealing of films due to growth of the interfacial layer. Surface nitridation prior to HfO_2 deposition is being suggested to reduce interface layer thickness. References 10 and 12 reported a thinner interfacial layer with a nitrided Ge surface, but a negative shift in flatband voltage indicates the presence of more positive oxide charge. Significant frequency dispersion was observed in the inversion region for thinner films in comparison to thicker films[15] after surface nitridation, indicating the higher interface states being present in thinner oxides.

Because we have deposited HfO_2 directly on the Ge substrate without any surface treatment, interfacial layer formation was possible for both 5-nm and 10-nm HfO_2 films. Reduced hysteresis and leakage current in 5-nm HfO_2 film and lower interface state density and EOT in 10-nm film further confirms that impact of the interfacial layer is higher for 5-nm film. In addition, an increase in interfacial layer thickness improves oxide quality but at the same time degrades the interface quality.

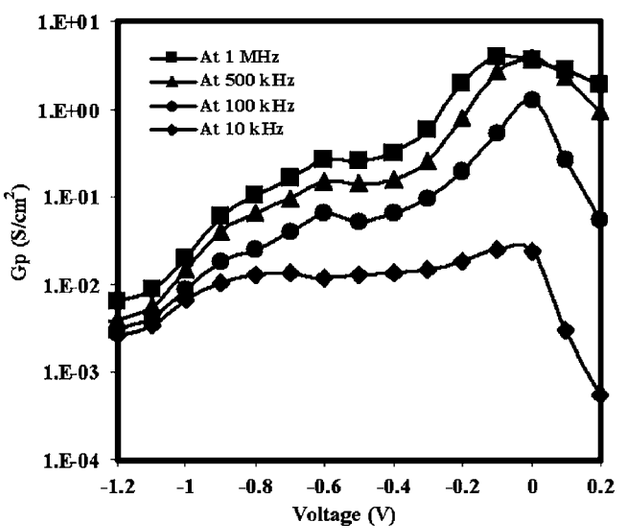

Figure 12. G-V characteristics of Ge/HfO_2 (5 nm)/Al MOS capacitors at different frequencies after 550°C annealing.

Conclusion

The physical and electrical properties of Ge MOS capacitors using thermally evaporated HfO_2 have been studied. SEM analysis showed the nonuniformity and island-like morphology of as-deposited HfO_2 films on the Ge substrate, but after 500°C annealing the films show a smooth and uniform surface. XRD analysis showed the presence of crystalline GeO_2. Electrical characterization showed the large hysteresis of 2.3 V and high leakage current of 10 A/cm^2 at 1 V in 10-nm as-deposited films. Hysteresis was significantly reduced to 0.9 V and leakage current also reduced by 6 orders of magnitude after annealing of these films at 550°C in N_2 ambience. 5-nm HfO_2 films showed the reduced hysteresis of 0.2 V and leakage current of $\sim 10^{-5}$ A/cm^2 after 550°C annealing. An increase in EOT was observed in both films at different annealing temperatures, which indicates possible the interaction of the interfacial layer with the gate dielectric. XPS results also confirm the interaction of GeO_2 with HfO_2 after 500°C annealing. Interface trap density was found to be in the range of 10^{12}–10^{13} cm^{-2} eV^{-1} after 550°C annealing.

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