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Charge Trapping at Deep States in Hf–Silicate Based High-κ Gate Dielectrics

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We have observed charge trapping during constant voltage stress in Hf-based high-κ dielectrics at deep traps as well as at the shallow traps. ΔV_{FB} and leakage current dependence on these deep traps further suggest that trapping at deep levels inhibits fast ΔV_T recovery. The earlier findings where charge trapping seemed to be very transient due to the presence of a large number of shallow traps and trapped charge could be eliminated by applying a reverse direction electric field may no longer be valid. The experimentally observed trap energy levels from low-temperature measurements establish a relationship between the origin of the deep traps and their dependence on O vacancy formation in Hf–silicate-based films. Substrate hot electron injection gives rise to significant electron trapping and slow post-stress recovery under negative bias conditions, which confirms that O-vacancy-induced deep defects determine the transient behavior in Hf–silicate-based high-κ gate dielectrics. It is further shown that *negative-U* transition to deep defects is responsible for trap-assisted tunneling under substrate injection. A fraction of the injected electrons remains trapped at the deep defects and gives rise to significant ΔV_{FB}. This has the potential to be the ultimate limiting factor for the long-term reliability of Hf-based high-κ gate dielectrics.
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Transistor scaling has so far achieved remarkable success in optimizing the diverse objectives like operational speed and lower power consumption. However, further downscaling of metal oxide semiconductor field effect transistor (MOSFET) sizes, specifically oxide thickness (t_{ox}) below 1.6 nm, increases transistor leakage current to levels unacceptable for low-power applications.[1] An attractive solution is to replace SiO_2 with high-κ dielectric materials (mostly Hf-, Zr-, and Al-based) while retaining the standard MOSFET design. Stringent application of the physical and electrical criteria like permittivity, band structure offset, thermodynamic stability, interface quality, gate-electrode compatibility, process compatibility, reliability, etc., shows Hf-based oxides as the most potential candidates out of many alternatives available.[2] In particular, Hf-silicates and their nitrided alloys are more likely to be the first generation of implementable high-κ. They have a moderately high dielectric constant (~8 to 15), depending on Hf content. But, it is compensated by higher thermal stability, better leakage characteristics, improved threshold instability, and lower mobility degradation compared to HfO_2.[3,4] In addition, silicates form better interfaces than metal oxides. However, long-term reliability remains the most critical factor to hold back its successful incorporation into the mainstream commercial integrated circuits (ICs).

For high-κ gate stacks, trapping within bulk dielectric is widely reported to be the most critical reliability issue.[1,2,5,6] First, significant hysteresis due to very fast charging and discharging of the trapped carriers causes transient threshold voltage instability, ΔV_T. This hampers high-frequency switching operations. Second, ΔV_T due to comparatively stable trapping is a serious concern for the long-term operational performance of MOS devices. Third, trapping has the most detrimental effect on the degradation of the channel-carrier mobility in high-κ MOSFETS. Fourth, bulk trapping distorts the internal electric field and modifies V_T and leakage characteristics. Fifth, defects responsible for trapping also assist in tunneling, which gives rise to the high gate current and inversely affects the advantages of high-κ oxides. Sixth, charging at trap levels, specifically near the metal gate electrode/high-κ interface, modifies the gate Fermi level. This gives rise to gate Fermi level pinning, which results in higher V_T. Therefore, it is obvious that studying the charge-trapping-induced degradation of the high-κ gate stacks is a key to understanding its reliability as it is the ultimate limiting factor for its long-term performance.

Charge-trapping characteristics can be investigated by hot carrier stress (HCS), positive/negative bias temperature instability (PBTI/NBTI), charge-to-breakdown (QBD), stress-induced leakage current (SILC), etc.[7] As far as high-κ gate stacks are concerned, this can be achieved by understanding the atomic structure and electronic properties of the defects within the high-κ dielectrics, electronic structure of the gate stacks, and carrier transport and kinetics under different oxide electric field conditions in conjunction with the critical analysis of the results observed from the electrical experiments. It is, therefore, imperative that high-κ reliability studies be carried out on a case-by-case basis. In this work, charge-trapping behavior of $Si/HfSi_xO_y/TiN$ gate stacks were studied by constant voltage stress (CVS) and substrate HCS. From low-temperature characteristics in the range of 275–78 K we try to establish a relationship between the energy levels of observed deep traps to that of the energy levels of O vacancy defects in Hf–silicate-based films. The conduction mechanisms through the dielectric due to the presence of deep states are also outlined.

Charge Trapping in High-κ

High-κ dielectrics have a much larger preexisting intrinsic trap density compared to silicon dioxide.[2,8] The high amount of heat required for the formation of SiO_2 makes the off-stoichiometry defects like O vacancies energetically costly. Moreover, SiO_2 has polar covalent bonds with a low coordination. This makes SiO_2 an excellent glass former, so that it remains amorphous. In addition, bonding in amorphous SiO_2 can relax locally to minimize defect concentration. The more prevalent bonds are the dangling bonds, specifically at the Si/SiO_2 interface. Passivation by hydrogen or deuterium can effectively remove them. Unlike SiO_2, high-κ oxides (e.g., HfO_2, ZrO_2, etc.) have higher atomic coordination numbers and greater ionic nature in their bonding due to the large difference in electronegativity of the metal and O atoms. Hence, high-κ oxides are poor glass formers, which is also evident from experimental observations as they cease to remain amorphous when subjected to high-temperature processing. This is why HfO_2 is preferred to ZrO_2, silicates to pure oxides, and nitrogen is added to inhibit crystallization.

The electrically active defect levels, responsible for electron/hole trapping, can be classified into three groups according to their locations within the bulk high-κ bandgap in the context of the MOS energy-band diagram,[1] specifically with respect to Si band edges, as shown in Fig. 1. Group A: Defect levels above the Si conduction

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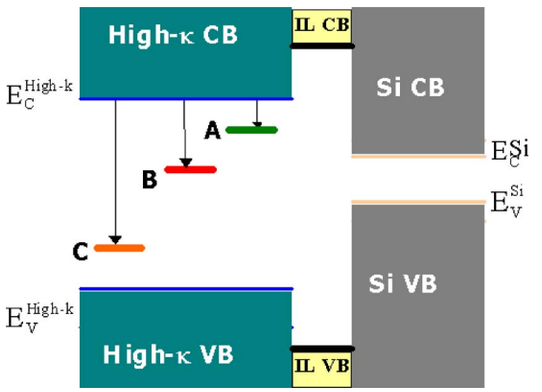


Figure 1. (Color online) Defect levels within the bulk high-κ in the context of MOS energy-band diagram.

edge, E_C^{Si} remain empty under "zero bias," i.e., zero electric field and thermal equilibrium conditions. However, under "nonzero" gate bias, i.e., substrate/gate injection conditions, such states are available for the resonant tunneling of electrons from E_C^{Si}/gate. Thus, they serve as electron traps. Trapping near the substrate is mostly responsible for ΔV_T. Once the bias is removed, very fast detrapping to substrate/gate, in the order of μs for gate stacks with thin interfacial layers, occurs from these states. Hence, these shallow levels give rise to fast transient trapping of electrons, which is mostly responsible for hysteresis and mobility degradation. Group B: Defect levels lie within the Si bandgap range. Electron/hole trapping in them can occur due to substrate/gate injection. Under zero bias condition, carriers trapped in these deep states detrap slowly to the substrate, depending on the physical distance from the substrate, and the activation energy with respect to E_C^{Si} ($E_a = E_T - E_C^{Si}$), which gives rise to slow transient trapping. ΔV_T due to trapping at these deep levels is the most critical reliability factor for the high-κ MOS devices. Transient trapping is described in more detail in the following sections. Group C: Electrons trapped at levels below E_V^{Si} give rise to fixed oxide charges. However, shallow hole trap levels, resonant with E_V^{Si}, are responsible for fast transient trapping under nonzero bias conditions.

Calculation-based models show that charged and neutral O vacancies $V^{2+}/V^{+}/V^{0}/V^{-}/V^{2-}$ are the potential electron traps in the bulk HfO_2.[1,2,7-15] V^{2+}, resonant with the Si conduction band at positive gate bias (substrate injection) due to its shallow level, relaxes to deep V^{+} level after trapping an electron ($V^{2+} + e \rightarrow V^{+}$). After trapping another electron V^{+} further relaxes to even deeper V^{0} level ($V^{+} + e \rightarrow V^{0}$). V^{0} level lies within the Si bandgap in the context of the MOS band diagram. Thus, negative-*U* behavior of V^{2+}, due to strong electron–lattice interaction, is responsible for deep electron trapping, which gives rise to slow transient trapping. V^{-}/V^{2-}, lying near the dielectric conduction band edge, shows no such electron-trapping-induced relaxation ($V^{-} + e \rightarrow V^{2-}$). Thus, V^{-} acts as a shallow trap and induces fast transient trapping.

Table II. Calculated formation energies of defects responsible for transient trapping.

Ref.	$V^{2+}/V^{+}/V^{0}$ (eV)	Hf–V^{2+} – Si/ Hf–V^{0}–Si
Gavartin et al.[9]	7	4 eV
Foster et al.[10]	9	—

O interstitials in the bulk HfO_2 are responsible for hole trapping. O^{2-} and O^{-} have energy levels below the Si valence band and after capturing holes ($O^{2-} + h \rightarrow O^{-}$; $O^{-} + h \rightarrow O^{0}$), O^{0} level, resonant with Si valence band, moves to its vicinity due to the negative-*U* behavior of O^{2-}/O^{-}. Calculations further suggest that another potential hole-trapping center is O "arm" vacancy, i.e., Si–V^{0}–Hf, which induces energy levels below E_V^{Si}.[9] This vacancy is located at the interfacial layer (IL)/high-κ interface. After capturing holes, Si–V^{2+}–Hf induces energy levels above E_V^{Si}, but within Si bandgap range.

In Tables I and II, defect levels and formation energies found by the different groups are stated. It is obvious that each group used a different set of parameters as far as the oxide bandgap and offset in Si/HfO_2 conduction edges are concerned. This, along with the number of atoms used in unit supercell formation and the level of optimization used in their calculations, gave rise to variation in the values.[1,2,9,11,12] However, the general trend as far as trapping-induced relaxation is concerned is obvious.

The major contributor to ΔV_T is the change in flatband voltage (ΔV_{FB}) due to charge trapping in the dielectric. The magnitude of ΔV_{FB}, therefore, depends on the concentration of O vacancies and their distribution within the bulk oxide. ΔV_{FB} can be induced in oxidizing ambient without incurring interfacial regrowth, due to O diffusion toward substrate and subsequent oxidation, if low-temperature and low O_2 partial pressures are used.[14] A constant capacitance at the accumulation regime in a capacitance–voltage (C–V) measurement suggests that interfacial layer growth has not occurred. O vacancy removal at low-temperature anneal was experimentally observed to decrease the dipole-induced reduction in the effective work-function difference.[14] Additionally, the V_{FB} shift after O_2 anneal can be reversed if forming gas anneal (FGA) is applied afterward. Reducing ambient of FGA increases O vacancies and thus increases V_{FB}. These experimental observations clearly show the presence of O vacancies in Hf-based oxides.

Stress/relaxation cycles are normally applied on Hf–silicate based-gate stacks to evaluate dynamic charge trapping.[15] Electron trapping dominates during the stress cycle and with only ~25% recovery of ΔV_T could be achieved during relaxation induced detrapping at the no bias condition. If trapping occurs at the shallow levels under substrate injection, partial detrapping takes place when the bias condition is reversed. During stress, electrons injected from the Si conduction band fill the shallow levels under the given band-bending condition. Accumulation of the trapped charge in the localized states quickly modifies the internal electric field. This gives rise to the subsequent redistribution of the trapped charge to deep levels, and the movement of the charge centroid toward the gate then takes

Table I. Calculated defect levels within HfO_2 bandgap responsible for transient trapping.

Ref.	V^{2+} (eV)	V^{+} (eV)	V^{0} (eV)	V^{-}/V^{--} (eV)	O^{-}/O^{--}	O^{0}	Hf–V^{2+}–Si	Hf–V^{0}–Si	$E_c^{HfO_2}-E_V^{HfO_2}$ (eV)	$E_c^{HfO_2}-E_C^{Si}$ (eV)
Torii et al.[12]	9	9	1.6	—	Below E_V^{Si}	Below E_V^{Si}	—	—	5.6	1.5
Gavartin et al.[9]	7	3.4	3.1	0.4	—	—	Above E_V^{Si}	Below E_V^{Si}	6.1	2
Robertson et al.[13]	9	1.3	2	0.7	5.5	5.5	—	—	5.8	1.5
Foster et al.[11]	9	2.8	2.8	—	4.8	—	—	—	5.7	1.5

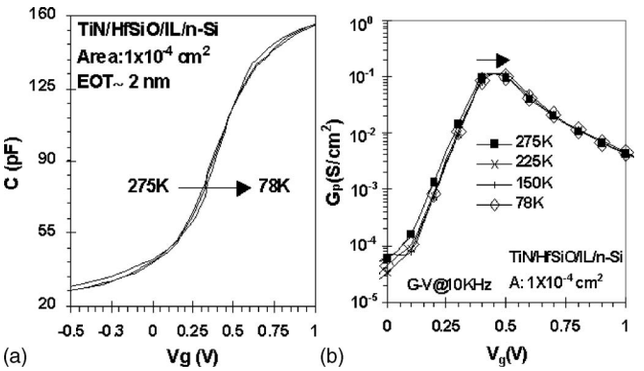


Figure 2. (a) 1 MHz C–V plots and (b) 10 kHz G–V plot in 275–78 K temperature range for pMOS-C.

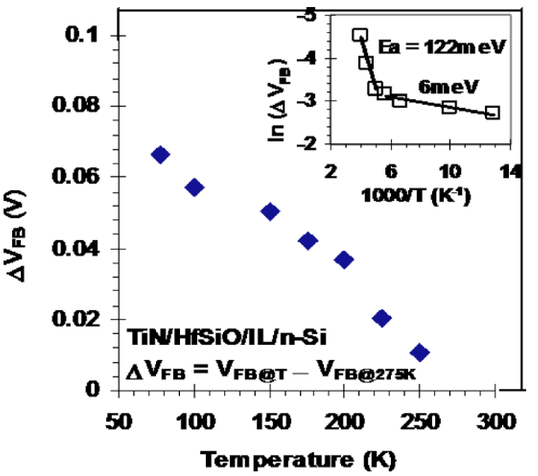


Figure 3. Flatband voltage shift (ΔV_{FB}) vs temperature for pMOS-C. (Inset) Arrhenius plot of ΔV_{FB}.

place. This explains the initial sharp rise of ΔV_T followed by its slow change as stress time is increased. During relaxation at the no bias condition, internal field, built during stress, gives rise to the release and subsequent redistribution of the trapped charges.[15] Thus, the relaxation-induced slow detrapping dominates.

Trapping within the bulk high-κ oxides is, therefore, due to the electrically active ionic defects.[2] It is also reported that it is possible to quickly (~10 ms) charge and discharge the traps under positive and negative gate-bias conditions, respectively, for Hf-based gate stacks with a thin IL (<2 nm), provided they are located near the substrate.[16,17] The defects in the deep levels, especially lying within Si bandgap range, are characterized in this paper. It is possible to fill the deep bulk traps with the majority carriers injected from the substrate and subsequently empty them if the gate bias (V_g) sweep levels from the accumulation to inversion regimes are carefully selected.[18] The temperature-dependent response of the majority carrier traps leaves its signature in ΔV_{FB} and, thus, enables the defect characterization.

Experimental

Hafnium silicate ($HfSi_xO_y$ – 20% SiO_2) film and TiN metal gate were deposited by MOCVD[3] on both n- and p-type Si substrates after ozone treatment that had been performed for the predielectric deposition cleaning, which resulted in ~10 Å of chemical oxide growth at the dielectric and Si substrate interface.[4] The precursor used during MOCVD deposition of gate dielectric was tetrakis[ethylmethylaminohafnium] (TEMA-Hf). The films were deposited at 400°C in O_3 ambient. The devices were then subjected to NH_3 postdeposition anneal (PDA) at 700°C for 60 s to improve leakage performance. Isolation edge and n^+/p^+-ringed MOS capacitors were fabricated using the standard complementary MOS (CMOS) process flow. Using high-resolution transmission electron microscopy (HRTEM), the physical thickness has been measured to be 4.5 nm, including an IL of 1 nm.[3] Physical characterization details can be found elsewhere.[3] An effective oxide thickness (EOT) of 1.8–2 nm was estimated from high-frequency C–V measurements after quantum mechanical corrections.[4] Isolated and active-edge n-/p-channel MOS capacitors (nMOS-C/pMOS-C and n^+-ringed nMOS-C/p^+-ringed pMOS-C) were fabricated. The parallel capacitance and conductance measurements were carried out at various frequencies (1 kHz to 1 MHz) using an HP 4284A LCR meter. Different parameters, including interface state density (D_{it}), were estimated using these measurements.[19]

Results and Discussion

C–V measurements in the 275–78 K temperature range are plotted in Fig. 2a for pMOS-C. The shift of C–V curves to the right with decreasing temperature indicates that electron trapping occurred. Conductance–voltage (G–V) measurements (10 kHz) in the 275–78 K range are shown in Fig. 2b. The horizontal shift of the peak of the G–V plots to the right also confirms that electron trapping occurred as the temperature was lowered. It is obvious from Fig. 2b that the change in trapping at the interface states is negligible, as the magnitude of the peak does not change with temperature. This affirms that electron trapping took place at the bulk high-κ.

As V_g is swept from the accumulation to depletion regimes, the deep bulk traps, with the energy level lying below the Fermi level, were filled with electrons injected from the substrate. As V_g is swept from the depletion to inversion regimes, the bulk-trap energy levels move above the Fermi level and these traps tend to become empty as a result of the detrapping of electrons to the Si conduction band, E_c^{Si}. However, this detrapping process is thermally activated. Hence, the detrapping of electrons decreases as the temperature is lowered, which results in the increase in ΔV_{FB}, determined after the temperature and quantum mechanical corrections, with low temperatures as observed in Fig. 3. This is why the activation energies of these deep defects, responsible for electron trapping, can be determined from Arrhenius plots as shown in the inset of Fig. 3. The energy levels of these deep defects, therefore, can be determined with respect to the E_c^{Si} from their activation energies. The activation energies, E_a, of these deep defects were found to be 122 and 6 meV.

For nMOS-C, the C–V plots in Fig. 4a shift to the left as the temperature is varied from 275 to 100 K. This indicates that hole

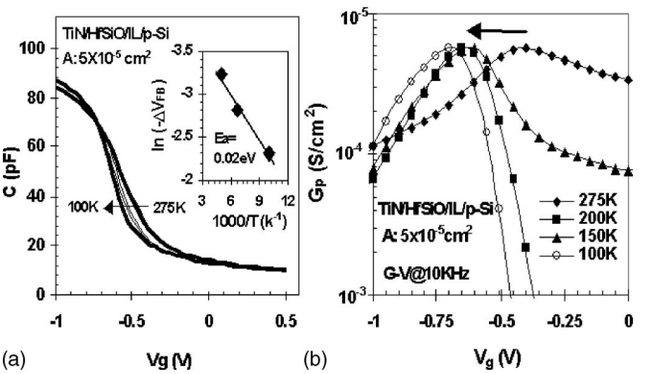


Figure 4. (a) 1 MHz C–V in 100–275 K temperature range for nMOS-C. (Inset) Arrhenius plot of $-\Delta V_{FB}$ shows a single bulk-defect level. (b) 10 kHz G–V in 100–275 K range for nMOS-C.

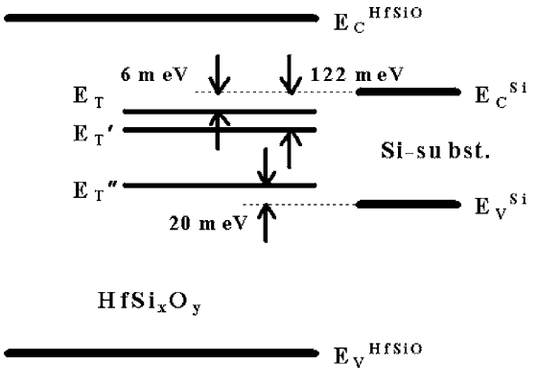


Figure 5. Deep bulk electron (E_T and E'_T) and hole (E''_T) trap levels in the context of MOS band diagram.

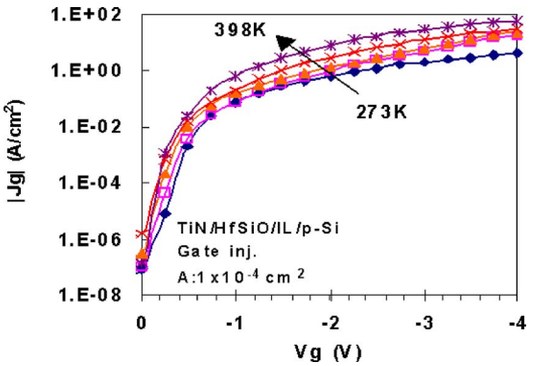


Figure 6. (Color online) I–V measurements in 273–398 K temperature range.

trapping dominates. The Arrhenius plot of the corrected- ΔV_{FB} in the inset of Fig. 4a shows a dominant defect level with activation energy of 20 meV. Figure 4b shows that peak of 10 kHz G–V plots shifts to the left as hole trapping took place, whereas the magnitude of the peak does not change as the trapping predominantly occurred within the bulk. The arguments, which were put forth in the previous section to show that the low-temperature-induced shift in flatband voltage is due to trapping at the deep defect levels, are also valid in this case. Therefore, the deep defect levels, which are physically located within the bulk high-κ and are responsible for hole trapping, lie within the Si bandgap as far as these gate stacks are concerned. Moreover, this defect level can be determined with respect to the Si valence band from the observed activation energy.

At low temperatures, the dopant atoms activation at the surface has been reported to cause dispersion in the C–V plots, especially at the flatband region.[20] When the Fermi level crosses the dopant atom energy level at the surface during C–V measurement, dopant atom charging/discharging responds to ac test frequency. This results in the observation of the "dip and peak" in the measured capacitance near the flatband region at low temperatures as reported in Ref. 21 and 22. In our devices, such discrepancies were not observed in the capacitance in the flatband region even when the test frequency was varied from 10 to 100 kHz at low temperatures (not shown). This furthers confirms the earlier assumption that low-temperature-induced dispersion in C–V is due to the trapping within the bulk high-κ.

The energy levels of these deep defects can be determined with respect to Si band edges from their activation energies as shown in Fig. 5. The bulk electron (E_T and E'_T) and hole (E''_T) trap levels are shown with respect to E_c^{Si} and E_v^{Si}, respectively, in the context of the MOS energy-band diagram in the figure.

Hf-based high-κ dielectrics are shown to be O deficient.[23] Moreover, O diffusion during growth is also observed by Guha et al.[23] The following defect reactions are possible between vacancies (V^0/V^+) and interstitials (O^0/O^-), as calculated in Ref. 10, at high temperatures during the growth

$$O^0 + V^0 \Rightarrow O^- + V^+ \qquad [1]$$

$$O^- + V^+ \Rightarrow O^{2-} + V^{2+} \qquad [2]$$

As PDA at 700°C took place during the fabrication of these devices, which was subject to the conventional CMOS process flow, it is quite reasonable to expect that such charged vacancies are present in these films. As such, the equilibrium in the numbers of charged vacancies and interstitials, i.e., the charge neutrality, is maintained in the fresh devices. As clearly mentioned earlier, the shallow V^{2+} level shows the negative-U transition to deep V^0 level after successively capturing two electrons ($V^{2+} + e \rightarrow V^+$; $V^+ + e \rightarrow V^0$). According to the calculation by Torii et al.,[12] V^0 lies ~1.6 eV below the conduction edge, which was also experimentally observed. Considering the Hf-silicate/Si conduction edge band offset to be ~1.5 eV,[24] the E'_T lies ~1.6 eV below the high-κ conduction edge in these films. Therefore, it affirms the assumption regarding the presence of O vacancy defects in the bulk high-κ films. Furthermore, the V^0 level lies within the Si bandgap range, i.e., it induces a deep defect level and gives rise to the slow transient trapping. Moreover, in order to maintain charge neutrality, O^{2-}/O^- levels also need to be present in the film. After capturing the hole, the O^0 level moves upward and may lie within the Si bandgap range. Based on this, we may tentatively assign E'_T and E''_T to V^0 and O^0 defect levels, respectively.

It is well known that Poole–Frenkel (P–F) emission is due to the field-enhanced thermal excitation of trapped electrons into conduction. Conduction across the oxide in the MOS structure due to PF emission can be described with the following equation[25]

$$J \approx E_{OX} \times \exp\left[\frac{-q \times (\phi_B - \sqrt{qE_{OX}/\pi\varepsilon_i})}{kT}\right] \qquad [3]$$

Here, J is the leakage density, E_{OX} is the oxide electric field, q is electron charge, ϕ_B is the barrier height of the trap, ε_i is the insulator permittivity, k is the Boltzmann's constant, and T is device temperature. It is obvious that the trap barrier heights can be determined from the Arrhenius plot of $\ln(J/E_{ox})$ if the leakage current is measured under substrate and gate-injection conditions as a function of temperature. The observed barrier height is δE less than the origi-

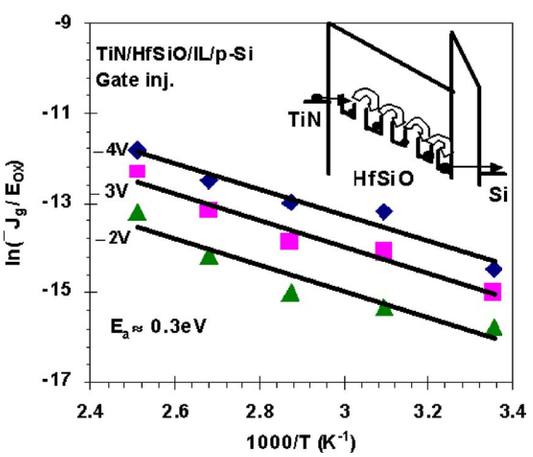


Figure 7. (Color online) Arrhenius plot of $\ln(-J_g/\mathcal{E}_{OX})$ for nMOS-C for different negative gate biases. (Inset) Transport through deep localized states under gate injection.

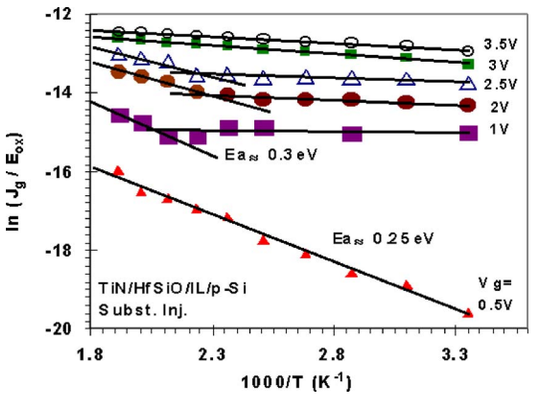


Figure 8. (Color online) Arrhenius plot of $\ln(-J_g/\mathcal{E}_{OX})$ for n^+-ringed nMOS-C for different positive gate biases (substrate injection). N^+-ring is grounded.

nal ($E_C - E_T$) value under the electric-field-induced band-bending condition.

Gate current vs gate voltage (I–V) measurements were taken for negative gate-bias conditions in the 273–398 K temperature range as shown in Fig. 6. It is obvious from the figure that a thermally and field-activated conduction mechanism dominates during gate injection. This is further evident from Fig. 7, which shows the straight-line behavior of Arrhenius plots of $\ln(-J_g/\mathcal{E}_{OX})$ for different negative gate biases applied on nMOS-C. The activation energy, E_a was calculated to be ≈0.3 eV for $V_g = -2$ to -4 V. Here, the electric field is $\mathcal{E}_{OX} = (V_g - V_{FB} - \Psi_s)/t_{OX}$, where Ψ_s and t_{OX} are surface potential and gate-stack thickness, respectively.

The ratio of the potential drops at the high-κ layer (V_{HK}) and IL (V_{IL}) are estimated from their respective dielectric constants (κ_{HK} and κ_{IL}) and thicknesses (t_{HK} and t_{IL}) using the following equation[28]

$$\frac{V_{HK}}{V_{IL}} = \frac{\kappa_{IL}}{\kappa_{HK}} \times \frac{t_{HK}}{t_{IL}} \quad [4]$$

As $t_{HK}/t_{IL} \approx 3.5$ and $\kappa_{HK}/\kappa_{IL} \approx 3.5$ in the gate stacks, equal potential drops at the high-κ layer and IL occur. Moreover, V_{HK} and V_{IL} are directly related to the band bending in high-κ layer and IL, respectively, and $V_{HK} = (V_g - V_{FB} - \Psi_s)/2$, where $V_{FB} + \Psi_s \approx -1$ V in nMOS-C devices. Considering the barrier height at the TiN/Hf–silicate interface to be ~2 eV,[26] the band bending at the bulk high-κ for $V_g = -2$ V ($V_{HK} \rightarrow -0.5$) is not enough for electrons to tunnel from the gate into the shallow traps with levels of 0.3 eV below the bulk high-κ conduction edge. The same also holds for $V_g = -4$ V ($V_{HK} \rightarrow -1.5$ V) as far as the traps located within the direct tunneling distance from the gate are concerned. Therefore, electrons do not enter the bulk high-κ conduction band, due to the thermal emission or field-assisted tunneling,[27] at any stage during their transport across the gate stack. Transport rather takes place through the deep localized states within the high-κ bandgap[27,28] as shown in the inset of Fig. 7.

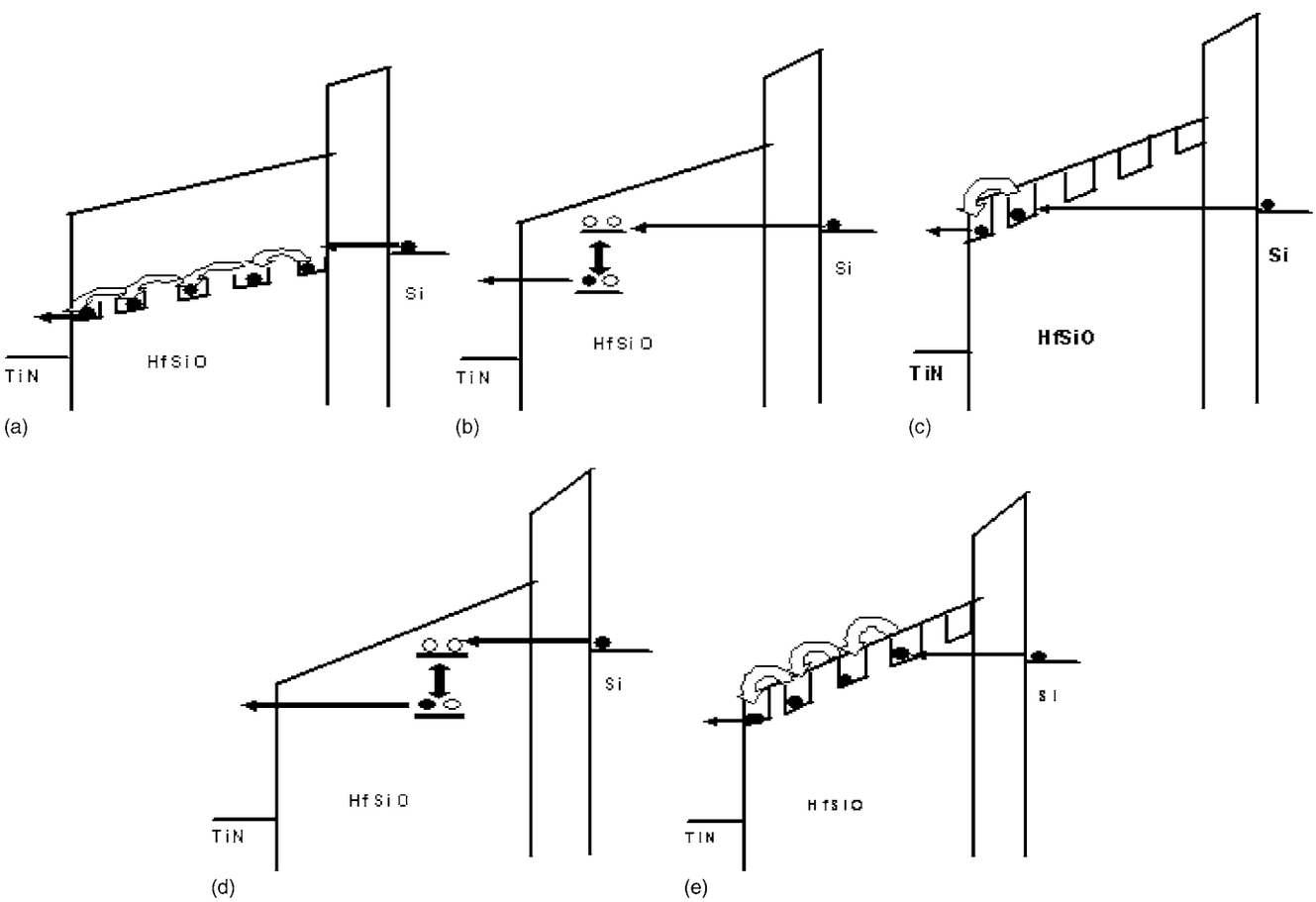


Figure 9. Transport mechanisms during substrate injection $TiN/HfSi_xO_y$-based gate stacks: (a) low gate bias, V_g(~0.5 V); (b) moderate V_g(~1 V) and temperature, $T < 200$ K; (c) moderate V_g(~1 V) and $T > 200$ K; (d) high V_g(~2 V) and $T < 175$ K, and (e) high V_g(~2 V) and $T > 175$ K.

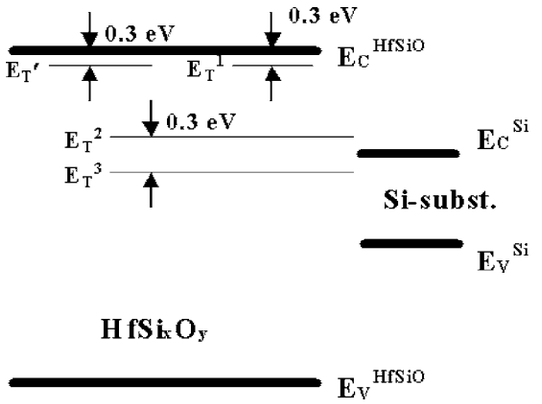


Figure 10. Defect levels in the context of MOS band diagram.

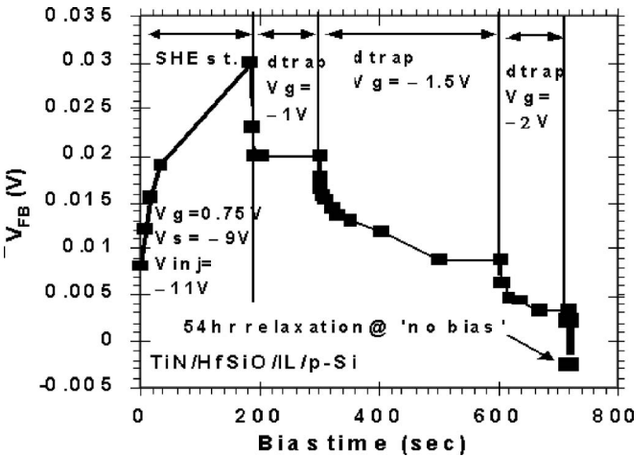


Figure 11. Time-dependent electron detrapping characteristics under different post-stress reverse-bias conditions.

Calculations show that the midgap V^0 and V^+ states are the potential candidates for electron transport.[13] We have already shown the strong possibility of the presence of V^0/V^+ levels in the oxide. Moreover, the difference between V^0 and V^+ levels was calculated to be 0.3 eV, which shows an excellent match with the experimentally observed E_a. Therefore, it is possible that electrons tunnel from metal gate to V^+ level, which relaxes to V^0 level after trapping an electron. Under strong electric field it thermally emits to the adjacent V^+ level, which lies 0.3 eV above. Thus, carrier transport may take place across the oxide during gate injection. This, in turn, gives rise to the experimental observation of V^+ level in this film.

P–F plots are shown in Fig. 8 for different positive gate biases, applied on n^+-ringed nMOS-C where n^+-ring was grounded to prevent minority carrier shortage during substrate injection. For positive gate biases (V_g), it can be approximated that $V_{FB} + \Psi_s \approx -0.5$ V, so that $V_{HK} = (V_g + 0.5)/2$. For very low $V_g(\sim 0.5$ V), conduction through deep states dominates as described in the previous section. E_a of ~ 0.25 eV implies that the $V^{+/}V^0$ pair, predicted for gate injection, may be responsible for substrate injection also. This is shown in Fig. 9a. The difference in activation energies may be due to the different band-bending conditions as specified in the P–F emission model. For moderate $V_g(\sim 1$ V), the leakage shows almost no change with temperatures below 200 K. At this bias, band bending does not allow Fowler–Nordheim (F–N) tunneling. Direct tunneling is another possibility. However, high leakage points toward the high concentration of defects within high-κ oxides that makes the trap-assisted tunneling (TAT) a more probable option. Negative-U transition of shallow V^{2+} levels, which are resonant with the Si conduction band, is a possible fit to TAT. This is depicted in Fig. 9b. Above 200 K, P–F emission to high-κ conduction edge dominates. $E_a = E_C - E_T \approx 0.3$ eV matches with V^-/V^{2-} trap levels. This shows that negatively charged vacancy levels are possibly present in these films. This is depicted in Fig. 9c. For moderately high $V_g(\sim 2$ V), TAT due to negative-U transitions dominates below 175 K, whereas P–F emission to the conduction band is significant above 175 K as shown in Fig. 9d and e, respectively. For high $V_g(\sim 3$ V), the dependence of leakage on temperature is not noticeably high.

The defects levels observed from leakage-current measurements under substrate and gate-injection conditions are depicted in Fig. 10. It is already shown that O vacancies are the primary defect centers for electron trapping. Calculations further indicate that these centers are responsible for electron transport. Torii et al.[12] reported TAT due to the negative-U transition of V^{2+} levels. The presence of O vacancies in Hf–silicate films can be reasonably established from low-temperature measurements. Shallow level, E_T^1, is observed to be lying 0.3 eV below the bulk high-κ conduction edge in this case. It is a good match with the calculated value of ~ 0.4 eV for V^-/V^{2-} in bulk HfO_2, shown by Gavartin et al.[11] The likely role of mid-gap V^+/V^0 states in P–F-like conduction[6] is already outlined. Hence, relative locations of the defect levels E_T^2 and E_T^3, shown in the figure, and consistent with the observations and predictions. Therefore, tentative physical origins of E_T^1, E_T^2, and E_T^3 are V^-/V^{2-}, V^+, and V^0, respectively. For E_T', it is speculated to be V^{2+} level.

In order to experimentally confirm O vacancy generation, substrate hot electron (SHE) stress was applied on n^+-ringed nMOS-C (Ref. 29) with incident carrier energies (E_{inc}) above the calculated O vacancy formation threshold (~ 7 eV). Carriers impinge on the Si/IL interface with $E_{inc} \approx q|V_s|$, where V_s is the applied substrate bias. Figure 11 shows a flatband voltage shift, ΔV_{FB}, during stress and recovery periods. Interface state generation was reported to be negligible,[29] hence, electron trapping occurred mostly within the bulk Hf–silicate. Detrapping from the bulk shallow traps to E_c^{HfSiO} (Ref. 30 and 31) at gate bias $V_g = -1$ V, quickly (~ 1 s) recovers ΔV_{FB} by $\sim 30\%$, but later it saturates. Detrapping at -1.5 and -2 V shows comparatively slow reduction, which can be attributed to the

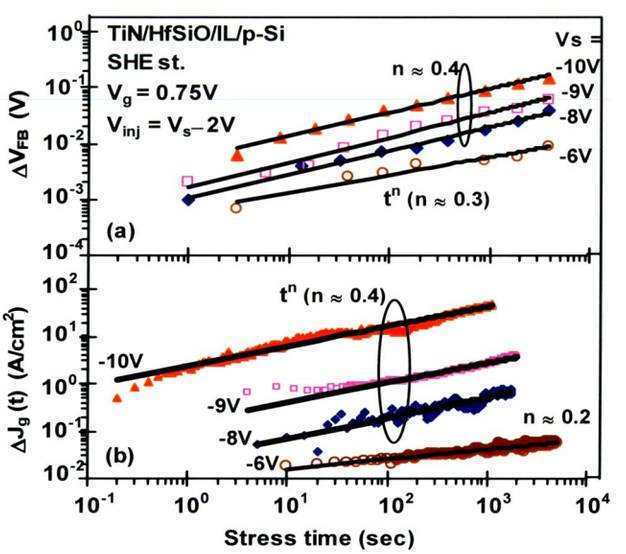


Figure 12. (Color online) (a) ΔV_{FB} and (b) $\Delta J_g(t)$ vs stress time under SHE stress for different V_s.

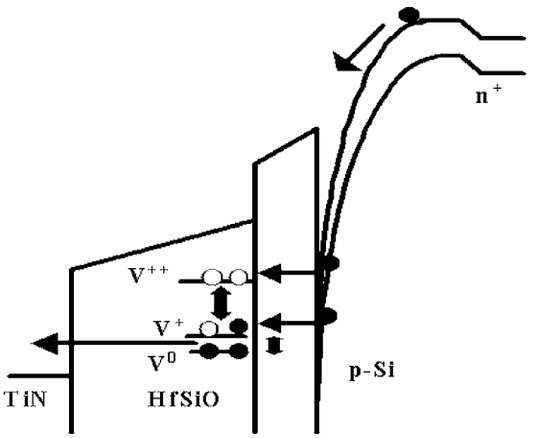


Figure 13. Energy-band diagram during SHE stress.

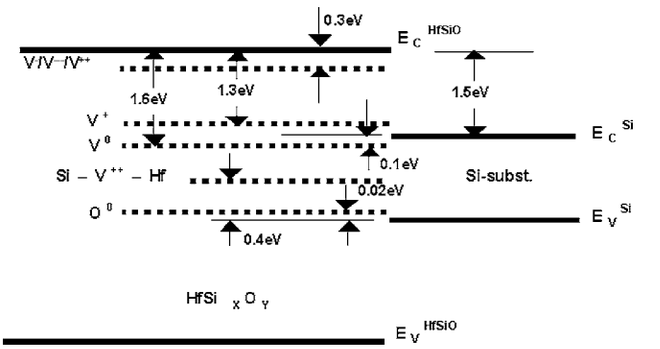


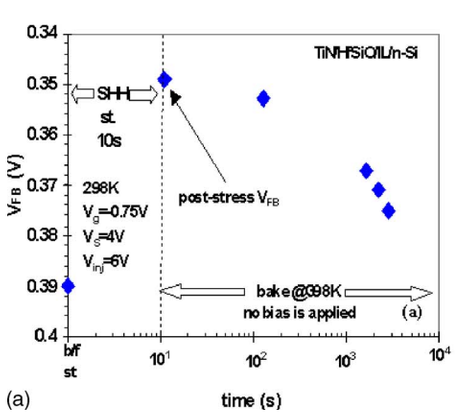
Figure 15. Defect levels in the context of MOS band structure.

trapping at the deep defects with lateral distribution.[17,29] Relaxation at the no-bias condition for 54 h, however, shows that hole trapping during high-bias recovery is partly responsible for the observed decrease in ΔV_{FB}. Hole trapping under gate injection under similar condition was reported earlier.[29]

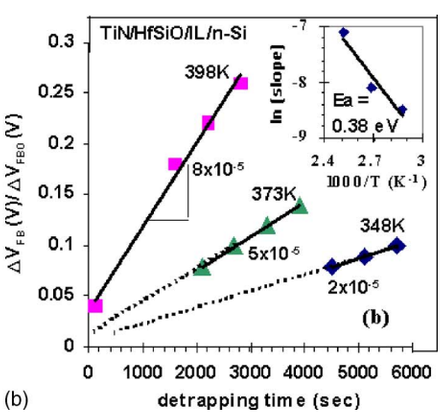
It is obvious that the slow transient trapping dominates under SHE stress. However, the effect of the fast transient trapping at the shallow levels on ΔV_{FB} needs to be eliminated to accurately study the slow transient trapping at the deep levels. To avoid restressing, each period of stress was followed by $V_g = -1$ V for 1 s before ΔV_{FB} was measured. Both ΔV_{FB} and the increase in leakage during stress, $\Delta J_g(t) = J_g(t) - J_g(0)$, follow t^n power-law dependence as shown in Fig. 12a and b respectively. $\Delta J_g(t) > 0$ is due to either enhanced trap-assisted tunneling[32] or increased hole trapping near the substrate.[33] The latter may be ruled out as $\Delta V_{FB} > 0$. Moreover, the release of the energy of plasmons at the metal/high-κ interface may induce the energetic anodic hole injection,[34] which initiates the positive-charge buildup near the substrate. But, the most obvious signature of this process is the interface state generation,[19] which is not observed in this case. For $V_s \leq -8$ V, exponent, $n \approx 0.4$ for both ΔV_{FB} and $\Delta J_g(t)$. This strong correlation, therefore, indicates that the same stress-induced deep defects are responsible for both enhanced slow transient trapping and trap-assisted tunneling. This trend, however, does not hold for $V_s = -6$ V. This disparity may be due to the difference in the defect generation mechanisms. $E_{inc} \approx 4$ eV is known as the threshold for the defect generation in Hf-based dielectrics.[33] But, O vacancy formation energy was calculated to be ~ 7 eV under equilibrium conditions (Table II). We observed a change in the defect generation mechanism for $E_{inc} \geq 8$ eV, confirming the generation of O vacancies.

To explain the role of O-vacancy-induced deep defects in trapping and transport during SHE stress at high V_s and low V_g, a coherent physical model consistent with experimental observations and the signature negative-U behavior of O vacancies is depicted in Fig. 13. Electrons impinge on Si/IL interface with high $E_{inc} >$ O vacancy formation threshold and generate V^{2+} defects. The relaxation to deeper V^+ and V^0 levels due to the trapping and subsequent tunneling from them towards the gate under the given band-bending condition increase the leakage. Defect levels other than V^{2+}/V^+ are also possibly resonant with the injected electrons as far as the band bending at low V_g is concerned. Hence, fast transient trapping at the shallow levels is observed; however, it is found to be partially responsible for ΔV_{FB}. A small fraction of the injected electrons ($\Delta V_{FB} \times C'_{ox}/\Delta Q_{in} \approx 1 \times 10^{-10}$; C'_{ox}=oxide capacitance/cm^2) remains trapped at the stress-induced deep V^0 levels and gives rise to the significant slow transient trapping. Without the negative-U transitions tunneling realized through the shallow levels alone, trapping would have been mostly limited to the shallow traps, and the correlation between slow transient trapping and trap-assisted tunneling would have been absent. However, observations are contrary to this, which further justifies the physical model.

In order to observe the defect levels of "arm" O vacancies (Hf–V^{2+}–Si), responsible for hole trapping, substrate hot hole (SHH) stress was applied.[31] The calculated formation energy of Hf–V^{2+}–Si is ~ 4 eV. Therefore, SHH stress with $E_{inc} \approx 4$ eV, i.e., $V_s = 4$ V, is expected to generate Hf–V^{2+}–Si defects. Moreover, an experiment involving time and temperature detrapping of holes to Si substrate was designed to find the defect level with respect to the Si valence band, E_V^{Si}.



(a)



(b)

Figure 14. (a) V_{FB} during 10 s of SHH stress followed by bake at 398 K under no-bias conditions. (b) $\Delta V_{FB}/\Delta V_{FB0}$ is plotted for different bake temperatures. (Inset) Arrhenius plot of the slopes shows a single bulk-defect level.

SHH stress (10 s) with $V_s = 4$ V was followed by baking at 398 K under no-bias conditions as shown in Fig. 14a. Periodically the bake was interrupted to measure V_{FB} at room temperature. It can be observed from the figure that V_{FB} decreased after stress, which signifies hole trapping in the generated traps. During the bake, V_{FB} increased as hole detrapping to substrate occurred. ΔV_{FB} is calculated from the difference of V_{FB} during the bake with respect to poststress V_{FB} ($\Delta V_{FB} = V_{FB}$ at bake time–poststress V_{FB}). It is normalized with respect to the initial increase in V_{FB} during stress ($\Delta V_{FB}/\Delta V_{FB0}$) and plotted as a function of detrapping time for different bake temperatures in Fig. 14b. It is obvious from the figure that slopes of hole detrapping, that is, hole emission rate, increase with even a moderate increment in temperature under no-bias conditions. The generated bulk high-κ trap levels lie within the Si bandgap range.[34] The Arrhenius plot of the slopes (Fig. 14b inset) shows an activation energy of ~0.4 V. Therefore, we may conclude that the physical origin of the stress-induced defects is arm vacancy. After capturing holes, the Hf–V^0–Si level, which lies below E_V^{Si}, relaxes to the Hf–V^{2+}–Si level (Hf–V^0–Si + 2 h → Hf–V^{2+}–Si), lying within the Si bandgap.

Defect levels, observed from different types of experiments, are shown in a comprehensive manner in the context of the MOS band diagram in Fig. 15. All the major defect levels, stipulated by theoretical models to be responsible for transient trapping and trap-assisted carrier conduction across the gate stack, have been put in the figure. Speculated physical origins of the defects are also stated. Calculated V^+ and V^{2+} levels are also shown for the sake of completeness.

Conclusions

Experimentally observed defect levels, which are responsible for both transient trapping and transport in Hf-based gate stacks, are discussed in the context of MOS band structure. An excellent match with calculations-based theoretical models is shown to exist. As a result, the probable physical origins of the defects have been tentatively stipulated. Slow transient trapping at the O-vacancy-induced deep defects is shown to prevent fast detrapping and thus remains as the major hurdle for the long-term reliability of high-κ gate stacks. P–F-like conduction through mid-gap states and trap-assisted tunneling due to negative-U transitions are found to be the major defect-modulated conduction mechanisms. On the basis of these observed defect levels, effective physical models can be formulated to provide a relevant explanation for the results obtained from different electrical stress tests, which are the integral parts of the high-κ reliability studies.

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