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Effect of Nitridation on Low-Frequency (1/f) Noise in n- and p-MOSFETS with HFO_2 Gate Dielectrics

P. Srinivasan,[a,b] E. Simoen,[a,*] Z. M. Rittersma,[c] W. Deweerd,[a] L. Pantisano,[a] C. Claeys,[a,d,] and D. Misra[b,*]**

[a]*IMEC, Kapeldreef 75, B-3001 Leuven, Belgium*
[b]*Department of Electrical and Computer Engineering, New Jersey Institute of Technology, Newark, New Jersey 00712, USA*
[c]*Philips Research Leuven, Belgium*
[d]*Electrical Engineering Department, KU Leuven, Belgium*

The nitridation effects on low-frequency (1/f) noise in metallorganic chemical vapor deposited HfO_2 n- and p-metal oxide semiconductor field effect transistors (MOSFETs) are reported. Devices with a postdeposition anneal (PDA), performed after HfO_2 deposition, in a N_2 or NH_3 ambient were investigated. A significant variation in noise was observed when different PDAs were employed. Devices annealed with N_2 showed lower input referred noise S_{VG} ($\sim$125 $\mu V^2/Hz$) for $|V_G\text{-}V_T| \sim 0.1$ V, close to the ITRS specifications when compared to NH_3 anneals ($\sim$1100 $\mu V^2/Hz$). Carrier trapping is shown to be the origin of the 1/f fluctuations for most n-MOSFET process splits. For p-MOSFETs, no significant impact of the PDA was observed, yielding a constant S_{VG} ($\sim$200 $\mu V^2/Hz$). Additionally, two types of interfacial layers were considered for n-MOSFETs, i.e., nitrided and non-nitrided interfaces, prepared by a decoupled plasma nitridation before HfO_2 deposition. Different trap density profiles were derived from the noise spectra for the nitrided- and non-nitrided-interface n-MOSFETs. This suggests that nitridation can induce nitrogen-related defects which lead to a variation in the concentration of oxygen vacancies in the bulk HfO_2. The binding configuration between the atoms may also play an important role.
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To reduce the high gate leakage current caused by the reduction of the SiO_2 layer thickness in metal oxide semiconductor field effect transistors (MOSFETs) for complementary metal oxide semiconductor (CMOS) Hf-based high-κ materials emerge as one of the major contenders to replace ultrathin SiO_2.[1-4] In spite of the recently reported successes, the performance of high-κ transistors requires further improvement to meet industry needs. Due to the intrinsic properties of Hf-materials, which greatly differ from Si-based dielectrics, various reliability-related issues exist. Problems that remain to be solved are the instability of the threshold voltage[3] and the significantly lower mobility compared with thermal SiO_2 gate devices.[4] These are related to a high density of traps present in the bulk or at the interface of a high-κ gate dielectric stack that can be charged or discharged depending on the operating conditions. In view of this, one can also expect a strong increase of the low-frequency (1/f) noise. For analog and radio-frequency applications, one of the important operation parameters is the 1/f noise. Because carrier trapping and detrapping within a few nm from the silicon interface govern the fluctuations in the channel current,[5,6] it is likely that the 1/f noise is an important issue to be considered for analog applications of devices with high-κ gates.[7,8]

It was earlier shown, that the interfacial layer has a strong dependence on the low-frequency noise performance in Hf-based MOSFETs.[9] The noise parameters—normalized noise and input-referred noise—are found to vary based on the thickness of the interfacial layer. Any treatment given to such interfacial-layer dependent gate stacks may or may not impact the low-frequency noise in these devices. It is expected that postdeposition anneal (PDA) will help in improving the quality of the gate stack as it can reduce its effective capacitance, due to a reduced physical thickness. Nitrogen-rich ambients, including remote nitrogen plasma, ammonia, nitrogen monoxide, and nitrogen dioxide, have been utilized for PDA. Various advantages have been seen and reported extensively in the literature.[10-16] Nitridation has been shown to reduce dopant penetration providing more thermal stability to the gate oxides. The effective κ value of the oxide and its crystallization temperature are found to increase. The gate leakage current in nitrogen-incorporated devices is found to be lower due to a variation in the effective barrier height of the dielectric. The role of nitrogen induced defects was also studied and was found to affect the intrinsic defects of the oxides–oxygen vacancies.[22-27] The nitrogen content in the interfacial layer is seen to prevent the degradation of the mobility with Hf-aluminate gate dielectrics as it acts as a barrier to both Si and O diffusion.[22]

Several investigations on 1/f noise and the underlying mechanisms have been performed at the device level with a focus on the processing parameters that may influence the noise. The present work attempts to study the impact of the incorporation of nitrogen by a PDA on the 1/f noise performance of n- and p-channel MOSFETs, with a metallorganic chemical vapor deposited (MOCVD) HfO_2 gate dielectric on nitrided and non-nitrided-interface devices. N_2 and NH_3 PDAs are compared with no-anneal devices as reference to complete the study.

Significant differences are observed in nitrided-interface and non-nitrided-interface n-MOSFETs, while a marginal impact of the PDA is found for the noise of non-nitrided-interface p-MOSFETs. The underlying reason for these differences was studied by deriving the qualitative trap density profile behavior in these devices.

Experimental

n- and p-channel MOSFETs of dimensions $W/L = 10/1$ (μm) with pure HfO_2 as gate dielectric were fabricated using a CMOS process flow. The main process steps for nitrided and non-nitrided interface are indicated in Table I. On top of a 0.8 nm thin interfacial chemical oxide (SiO_2), resulting from the use of an ozone chemistry, HfO_2 was deposited by MOCVD. Physical vapor deposited TiN/TaN metal gate was employed as the gate material. The estimated equivalent oxide thicknesses (EOT) of the studied devices is listed in Table II.

Two types of interfaces are investigated for n-MOSFETs, non-nitrided and nitrided. For the latter, decoupled plasma nitridation (DPN) was employed. "Soft" nitridation of the interface was done with a plasma energy (PE) close to 25 kJ. Following the DPN, a postnitridation anneal (PNA) was carried out in an O_2 ambient at 800°C for $\sim$15 s. In this case, the percentage nitrogen involved is $\sim$7–9%, estimated from X-ray photoelectron spectroscopy (XPS).[28]

Nitrided-interface n-MOSFETs involved NH_3, O_2, and no anneal conditions, while non-nitrided-interface devices had no anneal, N_2, and NH_3 anneals. The non-nitrided-interface p-MOSFET devices involved four different post deposition anneals—O_2, N_2, and NH_3,

* Electrochemical Society Active Member.
** Electrochemical Society Fellow.

Table I. CMOS fabrication flow showing important process steps required for nitrided and non-nitrided interface n-MOSFETs.

Non-nitrided interface	Nitrided interface
Chemical oxide growth (0.8 nm interfacial layer SiO_2)	Chemical oxide growth (0.8 nm interfacial layer SiO_2)
	Decoupled plasma nitridation (7–9% N_2 incorporated)
HfO_2 deposition (MOCVD)	Post-nitridation anneal (800°C) in oxygen ambient
PDA 800°C (NH_3 or N_2)	HfO_2 deposition (MOCVD)
Metallization (PVD–TiN/TaN)	PDA 800°C (NH_3, O_2 or N_2)
Gate electrode FGA anneal 520°C – H_2 +N_2 ambient–30 min	Metallization (PVD–TiN/TaN)
	Gate electrode FGA anneal 520°C–H_2 +N_2 ambient–30 min

and a no-anneal condition. All of the anneals were performed at 800°C for 60 s before the metal gate formation. In the case of no-anneal condition, the metallization process was carried out after gate dielectric deposition. After gate electrode metallization, the wafers were subjected to a forming gas anneal (FGA) at 520°C for 20 min.

On-wafer noise measurements were performed in linear operation at a constant drain voltage $|V_{DS}| = 0.05$ V for gate voltages $|V_G|$ of 0.5 to 2 V in steps of 50 mV using a BTA9812 noise analyzer and NoisePro software from Cadence. A channel length of 1 μm was chosen, to reduce device-to-device scatter in the noise magnitude.

Figure 1a-c shows the device transfer characteristics I_D-V_G of non-nitrided and nitrided-interface n-MOSFETs and non-nitrided-interface p-MOSFETs, respectively, for the various PDAs studied. Devices with no-anneal condition have the highest drive current with the lowest threshold voltage V_T compared to other PDA conditions for n-MOSFETs, while the NH_3 PDA results in the highest drive current for p-MOSFETs. Also inferred from Fig. 1b is that an O_2 or NH_3 PDA in devices with a nitrided interface reduces the saturation drive current I_D.

Results

Effect of non-nitrided interface on 1/f noise characteristics in n- and p-MOSFETs.— Figure 2a and b shows the low frequency noise spectra at $|V_{DS}|$ of 0.05 V and a gate voltage overdrive $|V_G$-$V_T|$ of ~0.1 V for various PDAs of the HfO_2 gate dielectric for non-nitrided-interface n- and p-MOSFETs, respectively. Predominantly $1/f^{\gamma}$ like spectra are obtained with the frequency exponent γ in the range 0.9-1.05. For n-MOSFETs, differences exist in the drain current noise spectra (S_{ID}) where N_2 anneals yield the lowest noise spectral densities. Devices annealed with NH_3 show higher noise values, which are comparable with the S_{ID} spectra for a no-anneal condition. Unlike n-MOSFETs, the drain current noise spectra are found to be similar for all PDA conditions for p-MOS devices.

For a proper comparison of the noise magnitude for the different PDA conditions, one has to compare the corresponding normalized current noise current spectral density S_{ID}/I_D^2, represented in Fig. 3a and b vs the gate voltage overdrive $|V_G$-$V_T|$ for $f = 25$ Hz and $|V_{DS}| = 0.05$ V, corresponding with n- and p-MOSFETs, respectively. Clearly, for all anneal conditions the normalized noise reduces as the gate voltage overdrive $|V_G$-$V_T|$ increases for n-MOSFETs. For any given $|V_G$-$V_T|$, NH_3 annealed devices show the highest values, approximately an order of magnitude higher than that of N_2 or no anneal devices. Irrespective of the anneal conditions, the power law dependence of S_{ID}/I_D^2 on $|V_G$-$V_T|$ is found to be ~1.5. This suggests that the 1/f noise in these devices can be described in the frame of the theory of correlated number fluctuations,[6] based on carrier trapping/detrapping and scattering in the dielectric. For p-MOSFETs, except for the no-anneal condition, the normalized noise S_{ID}/I_D^2 is inversely proportional to $|V_G$-$V_T|$ and hence these devices are explained in the frame of mobility fluctuations theory,[17] which confirms our earlier observations on metal gate p-MOSFETs.[18]

As shown in Fig. 4a, the input-referred voltage spectral density ($S_{VG} = S_{ID}/g_m^2$) at $f = 25$ Hz vs the gate voltage overdrive $|V_G$-$V_T|$ is seen to be dependent on the type of post-deposition anneal for n-MOSFETs. As can be observed for all $|V_G$-$V_T|$, lower values of

Table II. Device and noise parameter values for the different nitrided and non-nitrided interface n-MOSFET and p-MOSFET devices studied.

No.		Anneal condition	HfO_2 thickness (nm)	EOT (nm)	$S_{ID}f$=25 Hz [A^2/Hz]	$\sqrt{S_{VG}\lvert V_{GS}-V_T\rvert}$~0.1 V [V/$\sqrt{Hz}$]	WLS_{VG} $V_{GS}-V_T$~0.1 V [V^2 μm^2/Hz]	Normalized S_{VG} $V_{GS}-V_T$~0.1 μV [V^2/Hz]	$N_T\times10^{16}$ [1/cm^3 eV]	$D_T\times10^{10}$ [1/cm^2]
1	n-MOSFET	No anneal	2	1.50	1.50×10^{-20}	8.5×10^{-7}	7.3×10^{-12}	125 ~ 175	7.3	3.9
2		N_2	2	1.42	1.4×10^{-20}	7.2×10^{-7}	5.3×10^{-12}	100 ~ 150	5.2	2.2
3		NH_3	2	1.44	1.1×10^{-19}	2.4×10^{-6}	5.9×10^{-11}	900 ~ 1500	59	70
4		DPN NH_3	2	1.21	6.2×10^{-20}	1.9×10^{-6}	3.6×10^{-11}	850 ~ 900	36	15
5		DPN O_2	2	1.24	3.8×10^{-20}	1.6×10^{-6}	2.6×10^{-11}	850 ~ 900	26	11
6		DPN No anneal	2	1.25	8.8×10^{-20}	2.3×10^{-6}	5.4×10^{-11}	950 ~ 1050	55	23
7	p-MOSFET	No anneal	2	1.34	2.14×10^{-21}	6.42×10^{-7}	4.12×10^{-12}	95 ~ 105	—	—
8		NH_3	2	1.34	4.38×10^{-21}	9.31×10^{-7}	8.66×10^{-12}	200 ~ 225	—	—
9		O_2	2	1.39	3.25×10^{-21}	8.13×10^{-7}	6.61×10^{-12}	150 ~ 175	—	—
10		N_2	2	1.39	3.00×10^{-21}	9.20×10^{-7}	8.47×10^{-12}	200 ~ 225	—	—

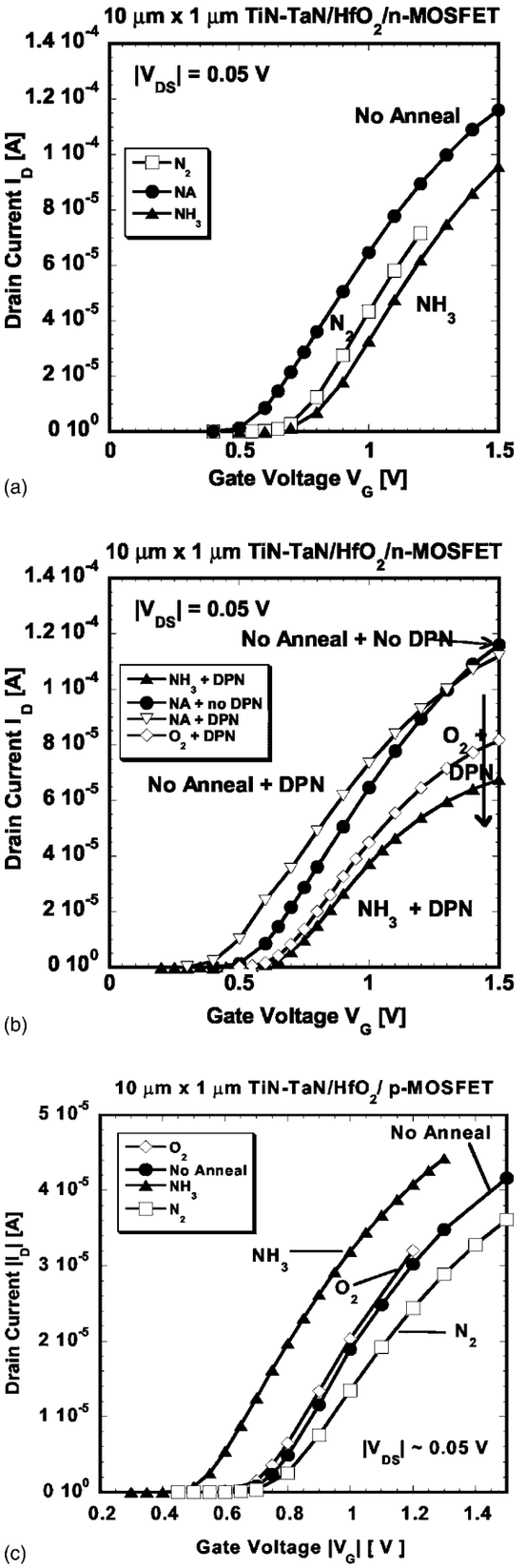

Figure 1. Device transfer characteristics I_D-V_G for (a) non-nitrided interface and (b) nitrided-interface devices, with different postdeposition anneals for n-MOSFETs (c) non-nitrided interface with different postdeposition anneals for p-MOSFETs.

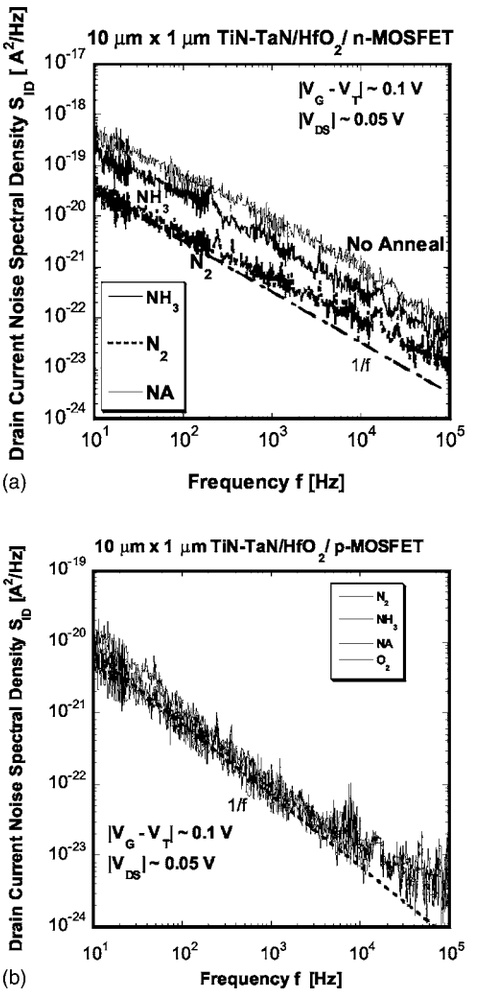

Figure 2. Drain current noise spectral density S_{ID}[A^2/Hz] vs frequency f [Hz] for HfO_2 devices with different PDA for non-nitrided interface in (a) n-MOSFETs and (b) p-MOSFETs.

S_{VG} are noted for N_2 and no anneal conditions while higher values up to an order of magnitude are noticed for NH_3 anneal conditions, in agreement with the results observed in Fig. 3a.

For p-MOSFETs, as shown in Fig. 4b, the input-referred voltage spectral density at f = 25 Hz vs the gate voltage overdrive $|V_G\text{-}V_T|$ is seen to have a similar variation for all the PDA conditions. A slightly higher S_{VG} for the NH_3 anneal condition was observed while it is comparatively lower for a no-anneal condition similar to the n-MOSFET case. The S_{VG} variation with gate voltage overdrive is also seen to be different than for the n-MOSFETs studied, where a lower dependency on $|V_G\text{-}V_T|$ is noted. This again points to a fundamentally different noise origin between the n- and p-channel devices: correlated-mobility fluctuations for the n-channel devices, giving rise to a quadratic dependence on $|V_G\text{-}V_T|$ or mobility fluctuations,[5] responsible for a proportional increase with gate voltage overdrive.[5,17]

Effect of interface nitridation on 1/f noise characteristics in n-MOSFETs.— Figure 5 shows the low-frequency noise spectra at $|V_{DS}|$ of 0.05 V and a gate voltage overdrive of $|V_G\text{-}V_T|$ of 0.1 V for various postdeposition anneals of an HfO_2 gate dielectric on a nitrided interfacial layer. Unlike for the non-nitrided-interface case shown in Fig. 2a, no differences were observed in the drain current noise spectra where N_2 and NH_3 postdeposition anneals have almost similar S_{ID} values. Devices with no postdeposition anneal and ni-

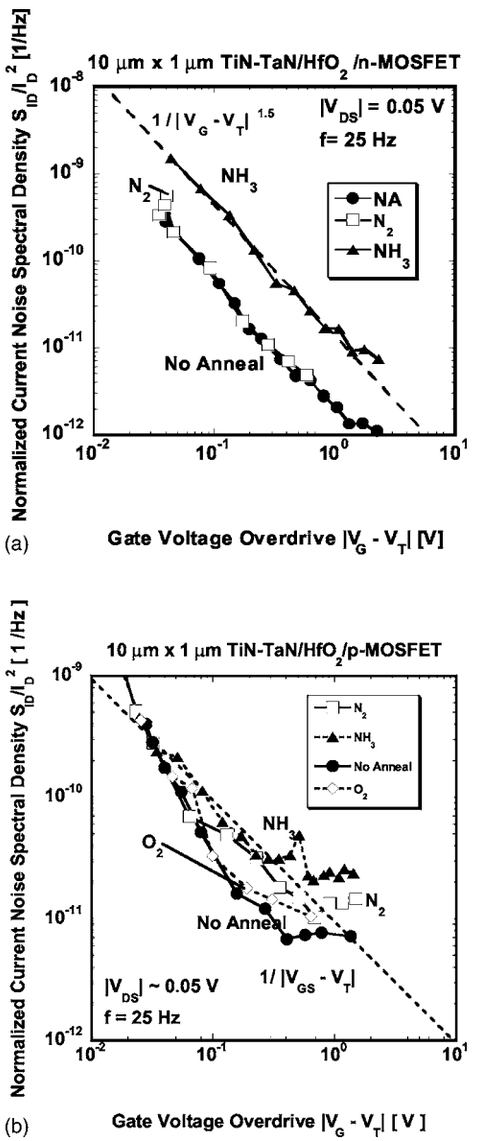

Figure 3. Normalized current noise spectral density $S_{ID}/I_D^2[1/Hz]$ vs gate voltage overdrive $|V_G\text{-}V_T|$ [V] for non-nitrided interface postdeposition anneals for (a) n-MOSFETs (b) p-MOSFETs.

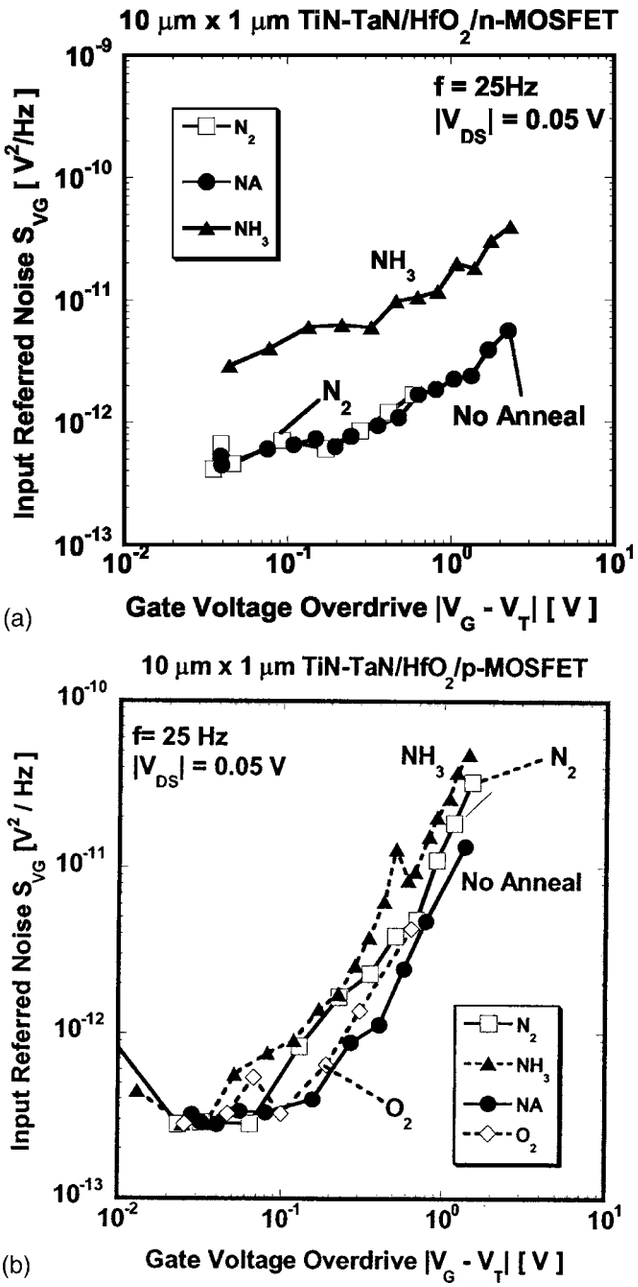

Figure 4. Input-referred noise $S_{VG}[V^2/Hz]$ vs gate voltage overdrive $|V_G\text{-}V_T|$ [V] for non-nitrided interface devices with different postdeposition anneals for (a) n-MOSFETs and (b) p-MOSFETs.

trided interface (NA + DPN) have also similar values compared to other post-anneals. No anneal and no DPN condition (NA + No DPN) has higher S_{ID} values, mainly due to higher drain current I_D observed in these devices.

Figure 6a shows the corresponding normalized noise current spectral density S_{ID}/I_D^2 against the drain current I_D for $f = 25$ Hz and $|V_{DS}| = 0.05$ V. Except for a nitrided-interface and no anneal case, a clear plateau in the normalized noise at lower drain currents and a roll-off at higher frequencies is observed, suggesting that the noise mechanism is due to number fluctuations.[19] Only for nitrided interface and no postdeposition anneal, the noise mechanism follows $1/I_D^{1.5}$ suggesting that the noise mechanism involves additional scattering-related effects also.[6]

Figure 6b shows the input-referred noise S_{VG} plotted against the gate voltage overdrive $|V_G\text{-}V_T|$ for various PDA conditions. While all PDAs yield similar S_{VG} values and similar variation with gate voltage overdrive, an order of magnitude lowering occurs for the non-nitrided and no-anneal condition, indicating the presence of nitrogen-related "noisy" traps.[6,13-16]

From the above results, it is clear that (*i*) nitridation of the interface has an impact on both the noise magnitude and the noise mechanism in these devices, (*ii*) nitridation of the interface suppresses the effect of the postdeposition anneal, and (*iii*) interface nitridation with no anneal has a different noise behavior when compared to a nitrided interface and postdeposition anneal conditions.

Discussion

Trap density profiles of non-nitrided and nitrided-interface in n-MOSFETs.— Figure 7 compares the qualitative trap density profiles obtained by plotting the product of frequency f and input-

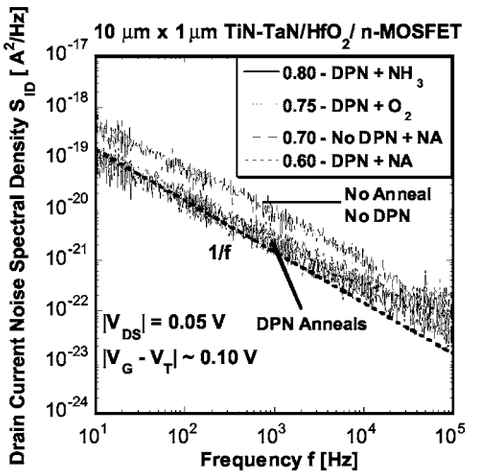

Figure 5. Drain current noise spectral density $S_{ID}[A^2/Hz]$ vs frequency f [Hz] for HfO_2 devices for nitrided-interface devices with different post-deposition anneals for n-MOSFETs.

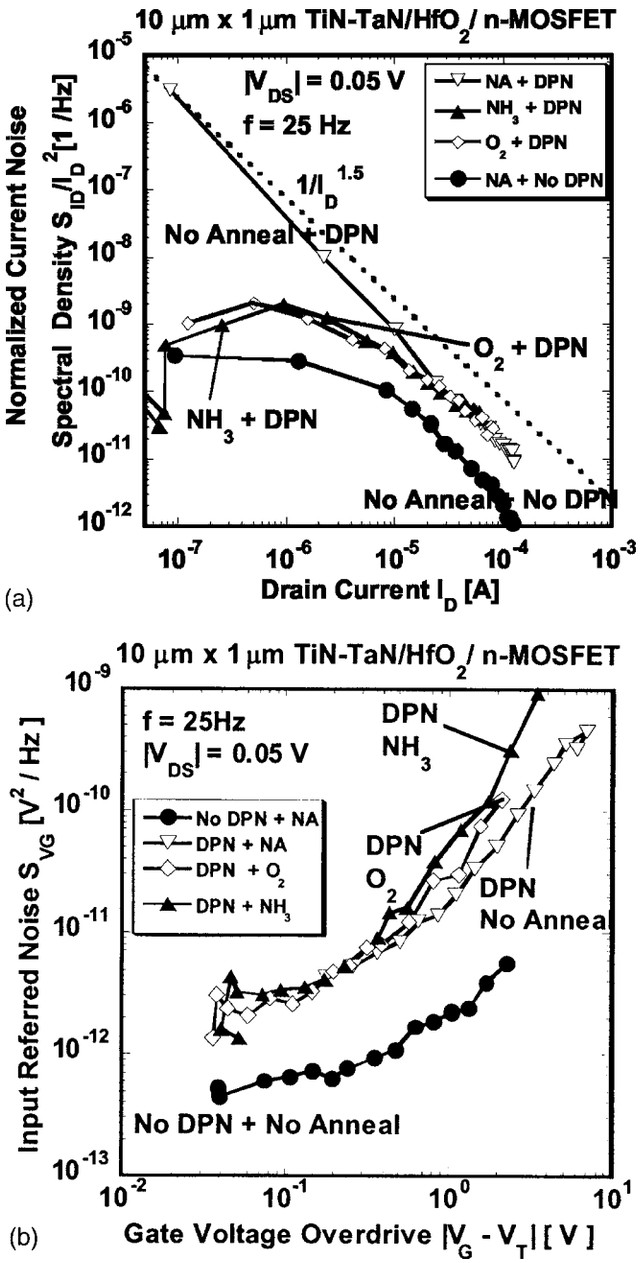

Figure 6. (a) Normalized current noise spectral density $S_{ID}/I_D^2[1/Hz]$ vs drain current I_D [A]. (b) Input-referred noise $S_{VG}[V^2/Hz]$ vs gate voltage overdrive $|V_G\text{-}V_T|$ [V] for nitrided-interface devices with different post-deposition anneals for n-MOSFETs.

referred gate noise spectra ($f \times S_{VG}$) vs the frequency for a non-nitrided and a nitrided-interface n-MOSFET and a NH_3 anneal condition. The frequency axis can also be interpreted in terms of the tunneling depth from the Si substrate based on the equation[20,21]

$$\frac{1}{2\pi f} = \tau_0 e^{\alpha_t z} \qquad [1]$$

with τ_0 the time constant at the interface (10^{-10} s) and α_t is the attenuation coefficient, z is the tunneling depth. In this case, we consider only tunneling at constant energy, neglecting thermal activation. It is, however, the usual assumption for the number fluctuations model.[5] Nevertheless, one should keep in mind that the obtained trap density profiles are rather first-order estimates or qualitative and should mainly be used for comparison purposes. The same remark goes for the trap densities derived from the input-referred noise spectral density later on.

With this in mind, effective trap density profile differences between nitrided-interface and non-nitrided-interface devices are observed for n-type high-κ MOSFETs with NH_3 postdeposition annealing. It is almost constant with depth throughout the high-κ and the interfacial layer for non-nitrided-interface devices, while for a nitrided-interface, an increasing trap density profile is observed around the interfacial layer, at high frequencies. This shows that the nitridation of the interface may have an additional impact on the stoichiometry of the interfacial layer by creating a high density of N-related noisy traps close to the Si–SiO_2 interface.[6,13-16]

Relation between nitrogen related defects, oxygen vacancies, and the impact of 1/f noise in nitrided-interface and non-nitrided-interface n-MOSFETs.— Depending on the ambient during PDA and the use of DPN, it is clear that different amounts (and profiles) of nitrogen will be introduced in the gate stack, which may influence the density and profiles of the N-and oxygen-vacancy-related traps. These concentration profiles are also important to determine the impact on 1/f noise. It has been recently established that the nitrogen related defects have a strong correlation with the oxygen vacancies and interstitials induced in high-κ devices.[22-27,29-33] In the case of nitrided-interface and non-nitrided-interface conditions, involving N_2 and NH_3, different nitrogen-defect mechanisms seem to exist.

It is widely believed that "molecular" N_2 is involved in the case of N_2 anneal condition in n-MOSFETs,[32] which is observed to have a minimal effect on the oxygen vacancies. This would mean that N_2 is ineffective in inhibiting the oxygen transport into the oxide. It is always possible that the mobile oxygen can diffuse in the interfacial layer (SiO_2), as oxygen has a higher affinity for Si than Hf, as the Gibbs free energy for the chemical reaction with SiO_2 is lower.[34]

In the case of interfaces involving plasma nitridation (DPN) as in Fig. 5 and 6, "atomic" N is involved in n-MOSFETs[32] where atomic nitrogen can react with oxygen unlike the earlier case. Due to this reaction, the total number of oxygen vacancies would be lower. In that case, lesser mobile oxygen is involved in transport. The role of this atomic nitrogen is also believed to passivate the Si–SiO_2 (substrate-interfacial layer) interface. It is possible that this interface passivation can suppress the effect of postdeposition anneals, which may explain similar values of 1/f noise observed in plasma nitrided interface devices.

Because the mobile oxygen involved is higher in non-nitrided-

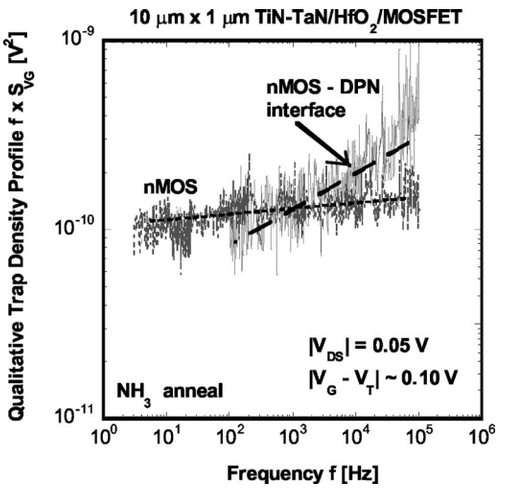

Figure 7. f × input-referred noise $S_{VG}[V^2]$ vs frequency f [Hz] for devices with non-nitrided interface and nitrided-interface n-MOSFETs after a NH_3 anneal.

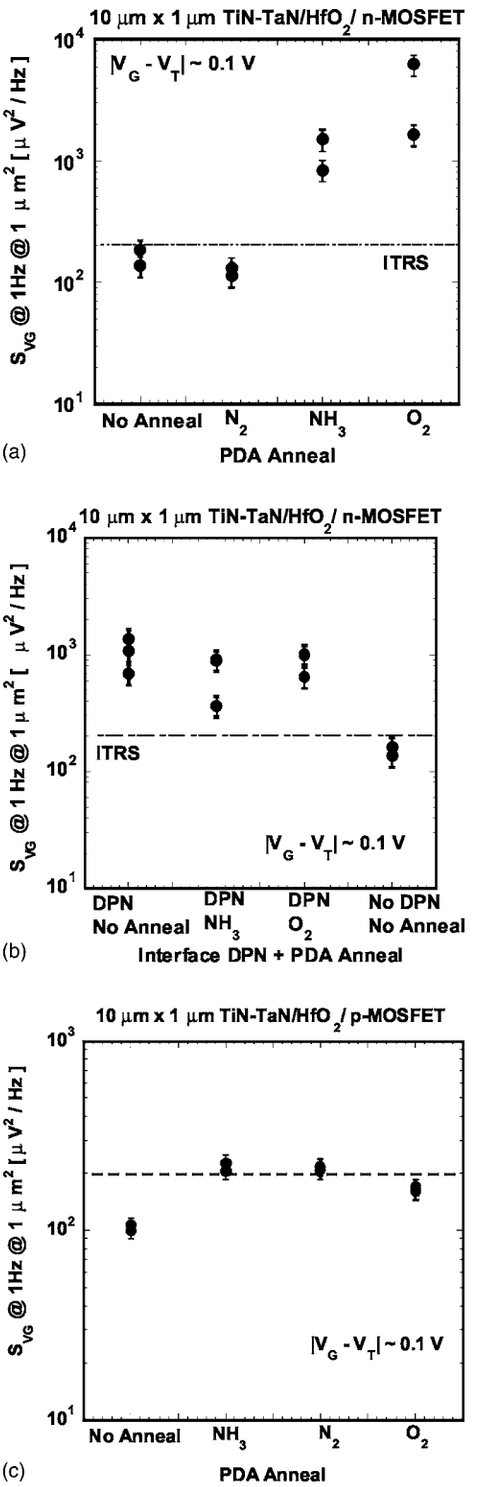

Figure 8. Normalized input-referred noise $S_{VG}[\mu V^2/Hz]$ at $|V_G\text{-}V_T| \sim 0.1$ V and $V_{DS} \sim 0.05$ V vs various PDA anneals for (a) non-nitrided interface, (b) nitrided-interface n-MOSFETs, (c) non-nitrided interface p-MOSFETs with different postdeposition anneals.

interfaces as in Fig. 2a, 3a, and 4a, it is possible that this oxygen can diffuse in the SiO_2 interfacial region, which increases the possibility of regrowth of the interfacial layer. Due to this regrowth, the thickness of the interfacial layer may increase, as is confirmed by the corresponding higher EOT values in Table II. The increase in interfacial layer thickness yields a reduced 1/f noise,[34] which is in line with the observation of a lower 1/f noise in the case of non-nitrided N_2 anneal when compared to nitrided anneal conditions where nitrogen (DPN) is involved as shown in Table II.

But in the case of NH_3 anneal condition, two different species are believed to be involved,[32] $NH_2^{\pm}$ and a proton (H^+). The likelihood that the proton (H^+) can bond to O is seen to be lower and hence there is charge build up due to the generation of protons and, hence, more electron trapping related events can occur. As additional trapping may be involved, higher 1/f noise is observed in these devices as seen in Fig. 3a and 4a.

Relating the above discussions of (I) trap profiles and (II) nitrogen-defect induced oxygen transport, it looks like that the binding configuration between various atomic species seem to play an important role, which can explain further the differences observed between plasma nitrided and nonplasma nitrided devices and their relationship to the observed differences in the trap density profile behavior. In the case of decoupled plasma nitrided (DPN) devices, it is possible that Si is mostly bonded to O and Hf has a preferential bonding to O,[31-33] while few Hf–N bonds may exist at the high-κ/IL interface, leaving a lower number of oxygen vacancies. Hence, more Si–O–N and Hf–O bonds exists at the high-κ/IL interface, giving rise to an increasing trap concentration in the vicinity of the interfacial layer of the gate stack.

With respect to the results for the p-MOSFETs, no conclusions can be drawn on a possible effect of N on the local trap density profile from the 1/f noise results. This is due to the fact that the fluctuation mechanism is related to scattering and not to trapping. Apparently, a PDA has a small effect (if any) on the scattering centers in the gate dielectric of p-channel devices (Fig. 2c, 3b, and 4b), which may be different than the trapping centers responsible for the 1/f noise in n-MOSFETs.

Estimation of volume and surface trap densities and comparison with ITRS specifications.— Figure 8a-c show the normalized input-referred noise S_{VG} for $|V_G\text{–}V_T| \sim 0.1$ V and $|V_{DS}| \sim 0.05$ V for different PDAs and nitrided-interface postdeposition anneals for n-and p-MOSFETs. Normalized noise refers here the value of input-referred gate noise normalized to unit area at a frequency of 1 Hz. The ITRS specification of 200 μV^2/Hz for a MOSFET rf device is also shown as a dotted line in the figures. While the no anneal condition has a lower value ($\sim$150 μV^2/Hz) meeting the ITRS specs, differences due to postdeposition anneals are noticed in

non-nitrided-interface devices. NH_3 ($\sim$1150 μV^2/Hz) and O_2 ($\sim$3000 μV^2/Hz) anneal show noise values higher by an order of magnitude when compared to other PDA conditions. In the case of nitrided-interface devices, the effect of postdeposition anneal is suppressed as explained earlier due to which a similar value of S_{VG} is noticed for all the PDA conditions ($\sim$900 μV^2/Hz). In the p-MOSFET case, the effect of PDA anneal is not seen as the values are found to be more or less similar ($\sim$200 μV^2/Hz).

From the values of S_{VG}, an effective volume trap density N_T can be estimated for n-MOSFETs using the formula[35,36]

$$S_{VFB} = q^2 kTN_T/(WT\, C_{EOT}^2 \alpha_t f) \quad [2]$$

where kT is the thermal energy, q is the electron charge, and the oxide capacitance density $C_{EOT} = \varepsilon_{ox}/EOT$ with ε_{ox} the permittivity of SiO_2. The tunneling parameter α_t is estimated semiempirically from the expected values of the effective tunneling mass for electrons (m_e^*) in the dielectric[37] and the potential barrier for electron emission at the silicon-oxide interface (ϕ_b) using the formula[6,20,21,35]

$$\alpha_t = \frac{1}{\hbar}\sqrt{2m_e^*\Phi_b} \quad [3]$$

where $\hbar$ is Planck's constant divided by 2π.

The surface trap density, calculated from N_T, is estimated using the formula 4 $kTzN_T$, where z is the tunneling distance of the electron from the Si/high-κ interface at f = 25Hz. The traps may be considered as "border-traps"[38] located near the substrate-dielectric interface. Table II shows the S_{ID}, S_{VG}, normalized S_{VG}, volume trap density N_T and surface trap density D_T for all the devices studied.

For non-nitrided-interface n-MOSFETs, N_2 PDA shows the lowest volume (N_T) and surface trap densities (D_T) indicating its beneficial effect, while NH_3 PDA has the highest trap values. On the other hand for the nitrided interface devices, the trap values are found to be almost similar in the range of $3 \sim 5 \times 10^{17}$ l/cm^3 eV for N_T and $1 \sim 2 \times 10^{11}$ l/cm^2 for D_T.

Conclusions

The low-frequency noise in n- and p-type MOSFETs with high-κ gate dielectric layers has been studied. Nitridation of the MOCVD HfO_2 oxide was carried out by a postdeposition anneal process where N_2 or NH_3 is used. Interface nitridation was carried out by a decoupled plasma nitridation process resulting in a $7 \sim 9\%$ N_2 in the interfacial oxide. Significant differences between PDAs were noticed in non-nitrided-interface devices where N_2 anneals have lower noise when compared to other anneal conditions. Devices with nitrided interface show a different behavior, where similar noise values were found, indicating the suppression of postdeposition anneals and also illustrating the stability of the interfacial layer due to N incorporation in SiO_2. Noise levels are also found to be largely independent on the PDA anneals for p-MOSFETs, owing to a different fundamental origin (mobility fluctuations). Differences in trap density profiles were observed between nitrided-interface and non-nitrided-interface n-MOSFETs, where an increasing trap profile is noticed for nitrided-interface devices and a more or less constant profile for non-nitrided-interface n-MOSFETs. Comparison of volume and surface trap densities for the different devices yields the lowest values for N_2 anneals whereas NH_3 anneals have the highest noise.

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