

CURRICULUM VITAE

NAME: Durga Misra

PERSONAL: Married, 2 children
U.S. Permanent Resident

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I. EDUCATION

Ph.D., Electrical Engineering, University of Waterloo, Waterloo, Canada, 1988
M.S., Management, New Jersey Institute of Technology, 1997
M.A.Sc., Electrical Engineering, University of Waterloo, Waterloo, Canada, 1985
M.Tech., Solid-State, IIT Delhi, India, 1983
M.S., Physics, Utkal University, Bhubaneswar, India, 1981
B.S., Physics, Utkal University, Bhubaneswar, India, 1978

I.a. PROFESSIONAL DEVELOPMENT

1995	Intensive Course on "Introduction to Modeling in VHDL with QuickVHDL,"	Mentor Graphics Product Training Course, Chicago, Aug. 7-11, 1995
1991	GDT Designer Tools	Mentor Graphics Product Training, San Jose, CA, Aug. 12-16, 1991
1990	Conference/Tutorials, Microelectronics System Education Conference/Expositions	San Jose, CA, July 29-Aug. 1, 1990
1989	NATO Advanced Study Institute, Novel Silicon Base Technologies	Boca Raton, FL, July 16-28, 1989
1989	Intensive Course on MOS Transistor Operation and Modeling	Columbia University, NY, May 22-26, 1989

II. RESEARCH INTERESTS

Solid State Electronic Devices and Materials includes Nanoscale semiconductor devices; Device reliability due to advanced fabrication principles; Understanding and minimization of process-induced damage mechanisms in semiconductor devices; and Very Large Scale Integration (VLSI) design includes CMOS Circuits for application specific integrated circuits (ASIC).

III. PROFESSIONAL EXPERIENCE

New Jersey Institute of Technology, Newark, NJ	2002 - 1993 - 2002	Professor, Electrical & Computer Eng. Dept. Associate Professor, Electrical & Computer Engineering Department
	1996 - 1997	Acting Director, Microelectronics Research Center, Newark College of Engineering
	1988 - 1993	Assistant Professor, Elect & Comp Eng Dept
Bell Laboratory, Lucent Technologies	1997 - 1997	Visiting Professor in VLSI Research

Murray Hill, NJ		Department
University of Waterloo, Waterloo, Ontario	1991 & 1992 1985 – 1988 1984 – 1988	Visiting Research Professor, Electrical Engineering Research Assistant Teaching Assistant
Sarnoff Corporation, Princeton, NJ	1990 – 1990	Visiting Professor at SEMATECH Center of Excellence in Plasma Processing
Cement Research Corporation, New Delhi, India	1983 – 1983	Research Engineer

III.a. CONSULTING EXPERIENCE

Keystone Venture Capital	2000-2001	High Speed CMOS Circuits
Lucent Technologies Murray Hill, NJ	1996-1998,	Plasma Process Induced Damage
Infinite Computer Technologies Alexandria, VA	1996-1998,	Non-volatile Random Access Memory
Rubicon, Inc., Princeton, NJ	1997-1998,	Development of Circuits for Ferroelectric Memory
Semiconductor Assembly Council, Mountain View, CA	1996-1997,	Development of a Standard Qualifying Die for SAC Member Companies.

III.b. RESEARCH COLLABORATION WITH INDUSTRIES

Lucent Technologies, Murray Hill, NJ
 Infinite Computer Technologies, Alexandria, VA
 Rubicon, Inc., Princeton, NJ
 Sarnoff Corporation, Princeton, NJ
 Semiconductor Assembly Council, Mountain View, CA
 Amkor Electronics Inc., Chandler, AZ
 Radiation Monitoring Devices, Watertown, MA
 Alphasel, Mendham, NJ
 Affiliated Engineering Laboratories, Inc., Edison, NJ

III.c. RESEARCH COLLABORATION WITH FEDERAL LABORATORIES

Naval Research Laboratories, Washington, DC
 ARMY Research Laboratory, Ft Monmouth, NJ

IV. HONORS AND AWARDS

- Associate Editor, IEEE Circuits and Devices Magazine.
- Awards Committee Chair, Thomas D. Callinan Award, Electrochemical Society, May 2000-Present.

- Program Chair, International Conference on Information Technology, India, Dec. 21-23, 2000.
- National Science Foundation Panel Review Member, June 1998 and May 2001.
- Board Member of Educational Consultants, National Institute of Science & Technology, India.
- Certificate of Achievement by McNair Achievement Program, NJIT, April 14, 2000.
- Certificate of Achievement by University Research Experience Program, NJIT, April 17, 1998.
- Recognition award by The Minority Academic Carriers Program, State of New Jersey, 1997.
- Recognition award by The Minority Academic Carriers Program, State of New Jersey, 1996.
- Canadian Commonwealth Scholarship Sept. 1983-July, 1988 at Univ. Of Waterloo.
- Dean of Graduate Studies Scholarship Sept.85 & May86 at Univ. Of Waterloo.
- M.Tech Scholarship 1981-1983 at Indian Institute of Technology, New Delhi.
- National Scholarship from Govt. of India 1974-1980.

IV.a. AWARDS RECEIVED by My STUDENTS

- PhD Student Wei Zhong received ECE Department **Hashimoto Award** in 2001, \$2,500.
- Undergraduate Student Nasif Akand received ECE Department **Best Senior Project Award**, May 3, 2001, \$250.
- Undergraduate Student Rafal Korczeniewski received **Honorable Mention** for Senior Project, First Industry-University Senior Project with Lucent Technologies, May 3, 2001.
- **Best Poster Paper Award** in Ninth Annual UNI-Tech Conference, Newark, NJ, April 2000.

V. RESEARCH, TEACHING AND LABORATORY DEVELOPMENT (NJIT)

Professor Misra is the director of Device and Materials Characterization Laboratory at NJIT and his research focus is in next generation fabrication technology for reliable electronic circuits involving nanometerscale silicon and silicon-germanium devices. Professor Misra's projects include deuterium implantation into silicon to neutralize the unwanted electrically active sites that enhances the performance and reliability of 2nm to 3nm gate oxide, an insulator used in Complementary Metal-Oxide-Semiconductor (CMOS) transistors. He also does research and teaching in the area of Very Large Scale Integration (VLSI) design involving application specific CMOS chips. In addition to graduate students, Professor Misra has so far supervised 20 undergraduate research assistants as a part of Research Experience for Undergraduates supported by NSF, State of NJ (NJIT-Tower) and NJIT. Eight went to graduate school. Seven undergraduates are co-authors in refereed publications.

VI. TEACHING

Courses Taught

FED	101 Fundamental of Engineering Design: Electrical Engineering Module
EE	291 Electrical Engineering Laboratory
EE	310 Cooperative Education and Internship
EE	405 Electrical Engineering Principle
EE	413 Introduction To Professional Engineering Practice
EE	463 Microelectronics Devices
EE	478 VLSI Semiconductor Circuits (Introduced New Course)
ECE	648 Digital Microelectronics
ECE	650 Electronic Circuits (Analog)
ECE	658 VLSI Design – I (Introduced New Course)
ECE	758 VLSI Design – II (Introduced New Course)
ECE	789 Introduction to Design Using VHDL (Introduced initially as a Special Topic Course)

VI.a. SHORT COURSES:

1. **D. Misra**, Introduction to VLSI Design Using VHDL, A Two Days Intensive Course at **Computer Science Department, Texas A&M University**, College Station, Texas, June 14-15, 1999.
2. **D. Misra**, "Introduction to VLSI Design and VHDL," at Sarnoff Corporation, Princeton, New Jersey, May 18, 1998 to July 7, 1998 (8 weeks), **Sponsored by Sarnoff Corporation**.
3. **Misra**, Two Days Intensive Course on "Principles and Recent Advances in VLSI Design - Use of VHDL as VLSI Design Tool," at National Institute of Science and Technology, Palur Hills, Berhampur, India, July 20th and 21st, 1998, **Sponsored by Council for Industrial and Scientific Research (CSIR), India**.

VI.b. NEW COURSES DEVELOPED:

EE 478-001 VLSI Semiconductor Circuits.

ECE 658-101 VLSI Design - I.

ECE 758 VLSI Design – II.

VI.c. OTHER TEACHING RELATED ACTIVITIES

Nominated by ECE Department for Excellence in Teaching Award for Graduate Instruction.

My Profile in Teaching Methodology is included in Appendix IV.E.

Course Supervisor for the courses EE 478 (since Fall 1990) and EE 658 (since Fall 1988).

Receiving \$1,500 to \$5,000 per year from **National Science Foundation/DARPA** to fabricate students' designs as part of their course projects.

Received Grants as PI and Co-PI for instructional laboratory development.

Contributing to the Computer Engineering program through CAD services.

First time introduced VHDL course at NJIT.

VI.d. GRADUATE STUDENT ADVISING

Post-Doctoral Graduates

R.K. Jarwal, January 1999 to Present, **Research Work:** Simulation of Ultra High Frame Rate Imager) and CMOS Device Physics and reliability, Supported by New Jersey Center for Optoelectronics.

P.K. Swain, March 1995 to May 1997, **Research Work:** Processing of SiGe Devices and materials, as per NSF proposal, **Development Work:** Developed the CMOS process in NJIT clean room.

Doctoral Students

T. Kundu, "Novel Interconnections for Nanoelectronics,"
PhD Thesis, Expected Graduation Date: May 2004.

M. Kim, "Microconcentrator Interface for Chemical Sensors," Supported by MRC, Jointly supervised by Dr. S. Mitra of Chem. Eng.
PhD Thesis, Expected Graduation Date: Summer 2002.

Wei Zhong, "Process Induced Damage and Defects to Materials and Devices," Supported by NSF and Anadigics.
PhD Thesis, May 2001. **Winner of ECE Department's 2001 Hashimoto Award.**
Current Employment: Anadigics, Warren, NJ

R.K. Kabra, "Design and Characterization of Ultra High Frame Rate Burst Image Sensors," Supported by PSI Inc and Sarnoff Corp.
PhD Thesis, January 1998
Sarnoff Corporation, Princeton, NJ.

K.R. Linga, Design, "Fabrication and Characterization of High Performance InGaAs/InP Focal Plane Arrays in the 1-2.6 μ m Wavelength Region," Supported by PSI Inc and Epitaxx.
PhD Thesis, May 1997
Laser Diode Inc., Edison, NJ

Masters Graduates

K. Gururaj, "VLSI Architecture for Deadlock Avoidance in Wormhole Networks,"
M.S. Thesis, August 2002.

S. Polturi, "Hyperbolic Position Location Estimator with TDOA from Four Stations,"
M.S. Thesis, Fall 2001.

R. Bucher, "A Synthesizable Low Power VHDL Model of the Exact Solution of Three Dimensional Hyperbolic Positioning System,"
M.S. Project, January 2000.

S. Kishore, "Investigation of Gate Oxides Grown on Light Deuterium Implanted Silicon Substrate,"
M.S. Thesis, August 1999.

P. Mohare, "Generic Emulation of Microprocessors,"
M.S. Thesis, May 1999.

S. Madapur, "Design, Simulation and Fabrication of a Two-Part Non Volatile Random Access Memory Circuit," M.S. Thesis, January 1998.

S. Ganesh, "Design, Simulation and Fabrication of a MEMS In-situ, Contactless Sensor to Detect Plasma Induced Damage During Reactive Ion Etching,"
M.S. Thesis, January 1997.

Y. Qiu, "The Study of SiGe-Channel Heterostructure MOS Device,"
M.S. Thesis, May 1996.

P. Patel, "Design of Neuron Cell Using FPGA."
M.S. Project, May 1996.

J. Shah, Graduated, "Automation of Reactive Ion Etching Process using a MC 68000 Microprocessor,"
M.S. Thesis, August 1993.

B. Wang, "Three Dimensional Magnetic Sensors and Array in BiCMOS Technology"

M.S. Thesis, January 1993.

L. Simhadri, "A Verilog Model for VLSI Implementation of Mathematical Morphology Operations,"
M.S. Project, May 1992.

A. Shah, "A Novel Micromachined Beam-Diaphragm Structure for High Performance Pressure Transducers,"
M.S. Thesis, August 1991.

V. Satyanarayana, "A 4-Bit BiCMOS Full Adder for ALU,"
M.S. Project, May 1991.

O. Ezebuirach, "Offset Cancellation in a MAGFET,"
M.S. Project, May 1991.

T. Jaswal, "A CMOS Logic Circuit to Reduce Substrate Current/Hot Carrier Effect,"
M.S. Thesis, May 1991.

S. Patel, "An n-Channel MOSFET with Schottky Source and Drain,"
M.S. Project, December 1990.

M. Zhang, "3-D Magnetic Field Sensor Design Based on Standard IC Technology,"
M.S. Thesis, December 1990.

D.K. Sampath, "A Novel CMOS Magnetic Field Sensor with Temperature Compensation Scheme,"
M.S. Thesis, December 1990.

V.S. Simhadri, "A Novel Schottky Barrier MOSFET for VLSI Applications,"
M.S. Thesis, August 1990.

B. Pathak, "Investigation of Micromechanical Properties of Tungsten Silicide Thin Films,"
M.S. Thesis, August 1990.

M.D. Bunyan, "Damage Effects in Si-SiO₂ Structures Due to Reactive Ion Etching,"
M.S. Thesis, May 1990.

Y. Chakravarthy, "A 512x512 Random Addressable Variable Resolution Image Sensor,"
M.S. Thesis, March 1990.

VII. PUBLICATIONS

VII.a. BOOKS EDITED

1. M.J. Deen, **D. Misra** and J. Ruzyllo (Editors), Integrated Optoelectronics, Electrochemical Society Proceedings Volume PV-2002-4, 444 pages, 2002 (ISBN 1-56677-370-5).
2. P.J. Hesketh, S.S. Ang, J.L. Davidson, H.G. Hughes, and **D. Misra**, (Editors), *Microfabricated Systems and MEMS-VI*, Electrochemical Society Proceedings Volume PV-2002-6, 260 pages, 2002 (ISBN 1-56677-272-5).

3. K.B. Sundaram, M.J. Deen, D. Landheer, W.D. Brown, **D. Misra**, M.D. Allendorf and R.E. Sah, (Editors), *Silicon Nitride and Silicon Dioxide Thin Insulating Films - VI*, Electrochemical Society Proceedings Volume PV-2001-7, 286 pages, 2001 (ISBN 1-56677-3136-X).
4. R.K. Ghosh, and **D. Misra** (Editors), CIT 2000, Proceedings of the Third International Conference on Information, Tata McGraw-Hill Publishing, New Delhi, 308 pages, 2001. (ISBN 0-07-043546-4).
5. P.J. Hesketh, S.S. Ang, W.E. Bailey, J.L. Davidson, H.G. Hughes, **D. Misra**, (Editors), *Microfabricated Systems and MEMS-V*, Electrochemical Society Proceedings Volume PV-2000-19, 394 pages, 2000 (ISBN 1-56677-286-9).
6. K.B. Sundaram, M.J. Deen, W.D. Brown, R.E. Sah, E. Poindexter, **D. Misra**, M.D. Allendorf, and S.I. Raider, (Editors), *Silicon Nitride and Silicon Oxide Insulating Film - V*, Electrochemical Society Proceedings Volume PV-99-6, 284 pages, 1999. (ISBN 1-56677-228-1)
7. G.S. Mathad, D.W. Hess, Y. Horiike, T. Lii, **D. Misra**, and L. Simpson, (Editors), *Plasma Etching Processes For Sub-Quarter Micron Devices*, Electrochemical Society Proceedings Volume PV-99-30, 378 pages, 1999. (ISBN 1-56677-253-2)
8. G.S. Mathad, **D. Misra**, K.B. Sundaram, (Editors), *Plasma Processing - XII*, Electrochemical Society Proceedings Volume PV-98-4, 292 pages, 1998. (ISBN 1-56677-198-6)

VII.b. FEATURE BOOK ARTICLES

1. **D. Misra**, Damage Due to Reactive Ion Etching - A Review, Trends in Electrochemistry, Editor: J. Menon, Publisher: Research Trends, Trivandrum, India, 1992, pp. 25-37.
2. **D. Misra**, "MIS, MIM, and MSM STRUCTURES." Wiley Encyclopedia of Electrical and Electronics Engineering: Semiconductor Manufacturing, Edited by J.G. Webster, John Wiley & Sons, Inc. New York (Published: September 26, 2001).

VII.c. REFEREED JOURNAL PUBLICATIONS

1. Ralph Bucher, and **D. Misra**, "A Synthesizable VHDL Model of the Exact Solution for Three-dimensional Hyperbolic Positioning System," vol. 15, No. 2, pp. 507-520, November 2002.
2. R.K. Jarwal and **D. Misra**, "Interface Hardening with Deuterium Implantation," Journal of Electrochemical Society, vol. 149, No. 8, pp. G446-G450, August 2002.
3. **D. Misra**, "Effect of Reverse Biased Floating Voltage at Source and Drain on Plasma Damage," IEEE Transaction on Electron Devices, vol. 49, No. 6, pp. 1090-1093, June 2002
4. R.K. Jarwal and **D. Misra**, "Reliability of Thin Oxides Grown on Deuterium Implanted Silicon Substrate," **IEEE Transaction on Electron Devices**, vol. 48, No. 5, pp 1015-1016, May 2001.
5. R.K. Jarwal, **D. Misra** and J.L. Lawrance, "Charge Transfer in a Multi-Implant Pinned-Buried Photodetector," **IEEE Transaction on Electron Devices**, vol. 48, No. 5, pp. 858-862, May 2001.

6. **D. Misra** and R.K. Jarwal, "Metal-Oxides-Semiconductor Diodes on Deuterium-Implanted Silicon Substrate," **Applied Physics Letters**, vol. 76, No. 21, pp. 3076-3078, May 2000.
7. **D. Misra** and S. Kishore, "Gate Oxides Grown on Deuterium Implanted Silicon Substrate," **IEEE/ECS Electrochemical and Solid-State Letters**, vol. 2, No. 12, pp. 637-639, December 1999.
8. **D. Misra**, "Charge-Trapping Properties of Gate Oxide Grown on Nitrogen-Implanted Silicon Substrate," **Applied Physics Letters**, vol. 75, No. 15, pp. 2283-2285, October 1999.
9. P.K. Swain, S. Madapur, and **D. Misra** "Plasma Process-Induced Band Gap Modifications of Strained SiGe Heterostructure," **Applied Physics Letters**, vol. 74, No. 21, pp. 3173-3175, May 1999.
10. K.P.Cheung, **D. Misra**, J. I. Colonell, C-T. Liu, Y. Ma, C-P. Chang, W-Y-C. Lai, R. Liu and C-S. Pai, "Plasma damage immunity of thin gate oxide grown on very lightly N⁺ implanted silicon," **IEEE Electron Device Letters**, vol. 19, no. 7, pp. 231, 1998.
11. **D. Misra** and K.P. Cheung, "Effect of source and drain junctions on plasma charging" **Semiconductor Science and Technology**, vol. 13, No. 5, pp. 529-531, 1998.
12. **D. Misra** and P.K. Swain, "Strain relaxation in SiGe due to process induced defects and their subsequent annealing behavior," **Microelectronics and Reliability**, vol. 38, no. 6, pp. 1611-1619, 1998.
13. **D. Misra**, W. Zhong, B. Bartynski, V. Patel, and B. Singh, Etch Induced Damage in High Density Inductively Coupled Plasma Etching Reactor, **Semiconductor Science and Technology**, vol. 11, No. 5, pp. 816-821, May 1996.
14. P.K. Swain, **D. Misra**, and P.E. Thompson, Effect of Dry Etching and Subsequent Annealing of Si/SiGe/Si Heterostructure, **Journal of Applied Physics**, Vol. 79, No. 8, pp. 4402-4406, 15 April, 1996.
15. **D. Misra** and B. Wang, Three-Dimensional Magnetic Sensors in BiCMOS Technology, **Sensors and Materials**, vol. 5 (6), pp. 369-384, 1994.
16. **D. Misra**, and B. Wang, Elimination of Cross-Sensitivity in a 3-Dimensional Magnetic Sensor, **IEEE Transactions on Electron Devices**, vol. ED-41(4), pp. 622-624, April 1994.
17. O.W. Purbo, C.R. Selvakumar, and **D. Misra**, Reactive Ion Etching of SOI (SIMUX and ZMR) Silicon in Nitrogen Containing CF₄ + O₂ and SF₆ + O₂ Plasmas, **Journal of Electrochemical Society**, vol. 140, no. 9, pp. 2659-2668, Sept. 1993.
18. **D. Misra** and V.S. Simhadri, "A Survey of the Potential of IrSi Schottky Barrier MOSFET Based on Simulation Studies," **Solid-State Electronics**, vol. 35, no. 6, pp. 829-833, June 1992.
19. **D. Misra**, M. Zhang, and Z. Cheng, "A Novel 3-D Magnetic Field Sensor in Standard CMOS Technology," **Sensors and Actuators**, vol. 34, no. 1, pp. 67-75, 1992.

20. **D. Misra**, "Reactive Ion Etching (CF₄ + O₂ Plasma) Induced Deep Levels In MOS Devices," **Journal of Vac. Sc. And Technology (A)**, vol. 10(2), pp. 301-304, March/April 1992.
21. V. Patel, M. Patel, S. Ayyagari, **D. Misra**, W.F. Kosonocky, and B. Singh, "Wafer Temperature Measurements and End-Point Detection During Plasma Etching by Thermal Imaging," **Applied Physics Letters**, vol. 59, no. 11, pp. 1299-1301, Sept. 9, 1991.
22. **D. Misra** and E.L. Heasell, "Annealing Behavior of Reactive Ion Etching Induced Deep Levels," **Journal of Electrochemical Society**, vol. 137, No. 5, pp. 1559-1563, May 1990.
23. **D. Misra**, "A Novel CMOS Magnetic Field Sensor Array," **IEEE Journal of Solid State Circuit**, vol. SC-25, No. 2, April 1990.
24. **D. Misra** and E.L. Heasell, "Electrical Damage to Silicon Devices Due to Reactive Ion Etching," **Semiconductor Science and Technology**, vol. 5, No. 3, pp. 229-236, March 1990.
25. **D. Misra** and E.L. Heasell, "Investigation of dry etching damage using p⁺ _n diodes," **Journal of Electrochemical Society**, vol. 136, No. 1, pp. 234-238, 1989.
26. **D. Misra**, C.R. Selvakumar, E.L. Heasell and D.J. Roulston, "Effect of RIE on electrical characteristics of poly-emitter bipolar transistors," **Solid State Electronics**, vol. 31, No. 11, pp. 1647-1649, 1988.
27. **D. Misra** and E.L. Heasell, "A study of reactive ion etching (CF₄ + O₂ plasma) induced deep levels in silicon," **Journal of Electrochemical Society**, vol. 134, no. 4, pp. 956-958, April 1987.
28. **D. Misra**, T.R. Viswanathan and E.L. Heasell, "A novel high gain MOS magnetic field sensor," **Sensors and Actuators**, vol. 9, pp. 213-221, September 1986.

Journal Papers in Review

1. M. Kim, S. Mitra, and D. Misra, "Micro-machined Heater for Microfluidic Devices," *Sensors and Actuators (In Review)*.
2. R.K. Jarwal and **D. Misra**, "Degradation of NMOSFETs under Reverse Biased Floating Voltage at Source and Drain Junctions during High-Field Injection," *IEEE Transaction on Electron Devices (In Review)*.
3. K.R.Linga, C.S. Wang, W.F. Kosonocky and **D. Misra**, "Noise Sources in Long Wavelength InGaAs/InP Focal Plane Arrays" *Solid State Electronics (In Review)*.
4. **D. Misra** and R. K. Jarwal, "Inversion Layer Hole Mobility Degradation due to High-Field Stressing," *Applied Physics Letters (In Review)*.

VII.d. NON-REFEREED JOURNAL PUBLICATIONS

1. D. Misra and J. Brewer, "Crystal Radio Detector ("Cat's Whisker"): The First Wireless Device," *IEEE Circuits and Devices Magazine, Devices Unlimited Column*, vol. 17, No. 2, pp. 12, March 2001.

2. P.K. Swain, H.K. Sehgal, and **D. Misra**, Preparation and Characterization of HgMnSe Thin Films Prepared by Flash Evaporation Technique, Electrochemical Society *Interface*, Vol. 4, No. 3, pp. 179, 1995.
3. P.K. Swain, **D. Misra**, Y. Qui, and P.E. Thompson, Effect of Dry Etching and Subsequent Annealing of Si/SiGe/Si Heterostructure, Electrochemical Society *Interface*, Vol. 4, No. 3, pp. 180, 1995.
4. **D. Misra**, A Book Review: "VLSI Fabrication Principle: Silicon and Gallium Arsenide" 2nd Ed., by Sorab K. Ghandi, John Wiley Interscience, 1994," **Semiconductor Science and Technology**, Vol. 10, pp. 213-214, February 1995.
5. V. Patel, W. Zhong, **D. Misra**, J. Gaudani, B. Bartynski, and B. Singh, Etch Induced Damage in High Density Inductively Coupled Plasma Etching Reactor, Electrochemical Society *Interface*, Vol. 3, No. 1, pp. 130, 1994.
6. W. Zhong, **D. Misra**, H. Amin, J. Gaudani, and M. Patel, Electrical studies on SF₆ and O₂ plasma etched Si_{1-x}Ge_x/Si p⁺_n heterojunction, Electrochemical Society *Interface*, Vol. 2, No. 3, pp. 122, 1993.
7. O.W. Purbo, **D. Misra** and C.R. Selvakumar, "Reactive Ion Etching of SOI (ZMR and SIMOX) Silicon in CF₄ + O₂ and SF₆ + O₂ Plasmas," **Journal of Electrochemical Society**, Vol. 139, No. 3, pp. 151C, 1992.
8. **D. Misra** and E.L. Heasell, "Annealing Behavior of Reactive Ion Etching Induced Deep Levels," **Journal of Electrochemical Society**, Vol. 136, No. 3, pp. 121C, March 1989.

VIIe. INVITED TALKS IN NATIONAL AND INTERNATIONAL CONFERENCES AND MEETINGS

1. **D. Misra**, "Electrical Characterization of Thin Oxides Grown on Deuterium Implanted Silicon Substrate," **Fourth International Symposium on the Physics and Chemistry of SiO₂ and the Si-SiO₂ Interface**, 197th Meeting of the Electrochemical Society, Toronto, Ontario, Canada, May 14-18, 2000.
2. **D. Misra**, "Circuit Design For Integrated Sensors," **Workshop on Analog Circuit Engineering**, Sheraton - Silicon Valley East Milpitas, California, January 15-16, 1990.

VII.f. CONFERENCE PROCEEDINGS (Reviewed)

1. K. K Gururaj, L. Zakrevski, and **D. Misra**, VLSI Architecture for Deadlock Avoidance in Wormhole Networks, Proceedings of the Fifteenth International Conference On Systems Engineering, Las Vegas, 6-8 August, 2002.
2. T. Kundu, R.K. Jarwal, and **D. Misra**, Enhanced Electron Transit Time in Pinned-Buried Photodetector, **Proceedings of First International Symposium on Integrated Optoelectronics**, Electrochemical Society Proceedings Volume PV 2002-4, pp. 253-259, 2002.

3. **D. Misra** and R. K. Jarwal, Study of Hole Mobility of PMOSFETs in Inversion Layer During High-Field Stressing **Proceedings of Sixth International Symposium on Silicon Nitride and Silicon Dioxide Thin Insulating Films**, Electrochemical Society Proceedings Volume PV-2001-7, pp. 52-59, 2001.
4. R. K. Jarwal and **D. Misra**, "Degradation Of NMOSFETs During High-Field Injection With Reverse Biased Voltage At Source And Drain Junctions," **Proceedings of the 14th International Conference on VLSI Design, an IEEE Computer Society Publication**, Bangalore, India, pp. 485-490, January 4-7, 2001.
5. **D. Misra** and R. K. Jarwal, "Electrical Characterization of Thin Oxides Grown on Deuterium Implanted Silicon Substrate," **Proceedings of the Fourth International Symposium on the Physics and Chemistry of SiO₂ and the Si-SiO₂ Interface**, Electrochemical Society proceedings volume PV-2000-2, pp.79-88, 2000.
6. R. Bucher and **D. Misra**, "A Synthesizable Low Power VHDL Model of the Exact Solution of Three Dimensional Hyperbolic Positioning System," **Proceedings of the International Conference on Modeling and Simulation of Microsystems 2000**, San Diego, CA, pp. T51.03, March 27-29 2000.
7. R.K. Jarwal and **D. Misra**, Effect of Reverse Biased Floating Voltage at Source and Drain on the Performance of NMOSFETs, **Proceedings of the Symposium on Structure and Electronic Properties of Ultrathin Dielectric Films on Silicon and Related Structures**, Materials Research Society Fall Meeting, Vol. 592, Boston, MA, Nov. 29-Dec. 3, 1999.
8. **D. Misra** and R. K. Jarwal, "Effect of Plasma Damage on Gate Oxide Grown on Nitrogen Implanted Silicon Substrate for 0.25 μ m CMOS Technology," **Proceedings of the International Symposium on Plasma Etching Processes for Sub-Quarter Micron Devices**, Electrochemical Society proceedings volume PV-99-30, pp. 159-166, 1999.
9. **D. Misra** and S. Kishore, "Thin-Gate Oxides Grown on Light Deuterium Implanted Silicon Substrate," **Proceedings of the Symposium on Silicon Nitride and Silicon Dioxide Thin Insulating Films**, Electrochemical Society proceedings volume PV-99-6, pp. 270-278, 1999.
10. C. Sylla, H.J. Wen and **D. Misra**, A Road-map for the Evaluation of Information Technology (IT) Investment, **Proceedings of the International Conference on Information Technology, ICIT'98**, Bhubaneswar, India, December 21-23, 1998.
11. **D. Misra**, "Plasma Charging in NMOSFET Due to Forward and Reverse-Biased Source and Drain Junctions during Metal-1 Etching, **Proceedings of the Symposium on Plasma Processing XII**, Electrochemical Society proceedings volume PV-98-4, pp. 36-42, 1998.
12. P.K. Swain and **D. Misra**, "Strain Relaxation in SiGe Due to P-Implantation and Subsequent Annealing," **Proceedings of the Symposium on State-of-the-Art Program on Compound Semiconductors XXVII** at The 193rd Electrochemical Society Meeting, May 3-8, 1998, San Diego, CA.
13. K.P.Cheung, S. Martin, **D. Misra**, K. G. Steiner, J. I. Colonell, C-P. Chang, W-Y-C. Lai, C-T. Liu, R. Liu and C-S. Pai, "Impact of Plasma-Charging Damage Polarity on MOSFET Noise," **IEEE International Electron Device Meeting**, pp. 437-440, Washington, DC, Dec. 7-10, 1997.

14. R.Kabra, V. Patel, J. Tower, J. Lowrance, V. Mastrocola, **D. Misra**, "180 x 180 Element Ultra High Frame Rate Burst Image Sensor," **Proceeding of the 40th Midwest Symposium on Circuits and Systems**, Sacramento, CA, Aug 02 - Aug. 06, 1997.
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35. **D. Misra** and E.L. Heasell, "Side wall etching anisotropy due to CF₄ + O₂ RIE for the fabrication of V-groove emitter transistors," "**Proceedings of the Symposium on Dry Process**" J. Nishizawa, Y. Horiike, M. Hirose, and K. Suto, Editors, The Electrochemical Society Softbound Series PV-88-7, pp. 71-77, 1988.

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VII.g. CONFERENCE ABSTRACTS

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2. M. Kim, S. Mitra and **D. Misra**, Micro-Concentrator Interface for Real-Time VOCs Sensors, Charles W. Tobias Memorial Student Poster Session, 200th Meeting of The Electrochemical Society, Inc., and the 52nd Meeting of The International Society of Electrochemistry, San Francisco, CA, September 2-7, 2001.
3. **D. Misra** and R. K. Jarwal, Study of Hole Mobility of PMOSFETs in Inversion Layer During High-Field Stressing, Extended Abstract, 199th Meeting of the Electrochemical Society, March 25-29, Washington, DC, 2001.
4. M. Phillips, S. Halim, R.K. Jarwal and D. Misra, Reliability of Thin Oxides Grown on Deuterium Implanted Silicon Substrate, Students' Poster Session, 198th Meeting of the Electrochemical Society, Phoenix, Arizona, October 22-27, 2000.
5. M. Kim, S. Kishore, S. Mitra and **D. Misra**, Design Fabrication, Testing and Simulation of MEMS Heater, Students' Poster Session, 197th Meeting of the Electrochemical Society, Toronto, Ontario, Canada, May 14-18, 2000.
6. R.K. Jarwal and **D. Misra**, Effect of Reverse Biased Floating Voltage at Source and Drain on the Performance of NMOSFETs, Proceedings of the Symposium on Structure and Electronic Properties of Ultrathin Dielectric Films on Silicon and Related Structures, Materials Research Society Fall Meeting, Boston, MA, Nov. 29-Dec. 3, 1999.
7. **D. Misra** and R. K. Jarwal, "Effect of Plasma Damage on Gate Oxide Grown on Nitrogen Implanted Silicon Substrate for 0.25 μ m CMOS Technology," Extended Abstracts (Abstract #684), 196th Meeting of the Electrochemical Society, Honolulu, Hawaii, October 17-22, 1999.

8. S. Kishore and **D. Misra**, "Thin-Gate Oxides Grown on Light Deuterium Implanted Silicon Substrate," Extended Abstracts (Abstract #3), 195th Meeting of the Electrochemical Society, Seattle, Washington, May 2-6, 1999.
9. **D. Misra**, "Plasma Charging in NMOSFET Due to Forward and Reverse-Biased Source and Drain Junctions during Metal-1 Etching, Extended Abstract (Abstract # 173), The 193rd Electrochemical Society Meeting, May 3-8, 1998, San Diego, CA.
10. P.K. Swain and **D. Misra**, "Strain Relaxation in SiGe Due to P-Implantation and Subsequent Annealing," Extended Abstract (Abstract # 420), The 193rd Electrochemical Society Meeting, May 3-8, 1998, San Diego, CA.
11. K. Linga, R. Kabra and **D. Misra**, "Noise sources in longwavelength InGaAs/InP Focal Plane Array," POEM Annual Research Review of Photonics, November 4, 1998, Princeton. NJ.
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14. R.Kabra, V. Patel, J. Lowrance, V. Mastrocola, **D. Misra**, "Ultra High Frame Rate Burst Image Sensor," NJCOE Poster Presentation, Princeton University, April 3, 1998.
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16. S.Ganesh and **D. Misra**, "A simple technique for anisotropic dry etching and release of polysilicon cantilever beams," Extended Abstracts (Abstract # 1167), 191st Meeting of the Electrochemical Society, May 4-9, 1997.
17. R.Kabra, V. Patel, J. Lowrance, V. Mastrocola, **D. Misra**, "Ultra High Frame Rate Burst Image Sensor," NJCOE Poster Presentation, Princeton University, March 20, 1997.
18. K.Linga, C.S. Wang. **D. Misra**, "High performance InGaAs/InP Focal Plane Arrays," NJCOE Poster Presentation, Princeton University, March 20, 1997.
19. T. Golota, Y. Cai, T. Fukaya, K. Linga, S. Ziavras, and **D. Misra**, VHDL Modeling of the BLITZEN Massively Parrel Processing, MARLUG 1996, Spring Conference, May 24, 1996.
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23. P.K. Swain, **D. Misra**, Y. Qui, and P.E. Thompson, Effect of Dry Etching and Subsequent Annealing of Si/SiGe/Si Heterostructure, 188th Meeting of the Electrochemical Society, 1995, Vol. 95-2, Abstract No. 1036.
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26. W. Zhong, **D. Misra**, H. Amin, J. Gaudani, and M. Patel, Electrical studies on SF₆ and O₂ plasma etched Si_{1-x}Ge_x/Si p₊-n heterojunction, 184th Meeting of the Electrochemical Society, 1993, Vol. 93-2, Abstract No. 268.
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28. W. Zhong, H. Amin, J. Gaudani, and **D. Misra**, Damage to Si_{1-x}Ge_x strained layers due to reactive ion etching, The Microelectronic Processing '93, SPIE Symposium Monterey, California, Septmber 27 - 29, 1993.
29. O.W. Purbo, **D. Misra** and C.R. Selvakumar, "Reactive Ion Etching of SOI (ZMR and SIMOX) Silicon in CF₄ + O₂ and SF₆ + O₂ Plasmas," 181th Meeting of the Electrochemical Society, 1992, Vol. 92-1, Abstract No. 193, pp. 323-324.
30. L. Simhadri, and **D. Misra**, Verilog Model for VLSI Implementation of Mathematical Morphology Operations, Open Verilog International UG Meeting, Santa Clara, CA, March 24-25, 1992.
31. B. Wang and **D. Misra**, "A Novel 3-Dimensional Magnetic Field Sensor Array in Merged BiCMOS Technology," Late News Paper, 1992 IEEE Solid-State Sensor and Actuator Workshop, Hilton Head Island, SC, June 21-25, 1992.
32. **D. Misra**, O.W. Purbo, and C.R. Selvakumar, "Reactive Ion Etching of SOI Silicon," Proceedings of the Symposium of the Advanced Technology Center for Surface Engineered Materials (ATC/SEM), Piscataway, NJ, Nov. 25, 1991.
33. **D. Misra**, and Alkesh Shah, "A Microengineered Beam Diaphragm Structure for the High Performance Pressure Sensor," Proceedings of the Symposium of the Advanced Technology Center for Surface Engineered Materials (ATC/SEM), Piscataway, NJ, May 13, 1991.
34. **D. Misra** and W.N. Carr, "Microengineered Sensors: A Review," Proceedings of the Electro/International (IEEE) Conference, New York, NY, April 16-18, 1991.

35. V. Patel, M. Patel, S. Ayyagari, **D. Misra**, W.F. Kosonocky, and B. Singh, M. Leahy, "Application of Thermal Imaging for Monitoring Wafer Temperature and End-Point Detection In Plasma Etching," SRC TECHCON '90, San Jose, CA, October 16-18, 1990.
36. **D. Misra**, Reactive Ion Etching (CF₄ + O₂ Plasma) Induced Deep Levels In MOS Devices," Presented at the 37th National Symposium of American Vacuum Society, Toronto, Canada, October 8-12, 1990.
37. V. Patel, M. Patel, S. Ayyagari, **D. Misra**, W.F. Kosonocky, and B. Singh, M. Leahy, "Wafer Monitoring by Infrared Camera During Plasma Etching: Analysis and Experimental Results," Presented at the New Jersey SEMATECH Center of Excellence for Plasma Etching - Annual Review, Princeton, NJ, August 7, 1990.
38. **D. Misra** and B. Pathak, "Design and Processing of Micromechanical Structures of Silicide Films," Proceedings of the Symposium of the Advanced Technology Center for Surface Engineered Materials (ATC/SEM), Hoboken, NJ, May 16, 1990.
39. **D. Misra**, "Modulus of Elasticity Measurement of Micromechanical Tungsten Silicide Cantilever Beams," (Poster Presentation), Consortium for Surface Processing, Rutgers University, June 8, 1989.
40. B. Pathak and **D. Misra**, "Modulus of Elasticity Measurement of Micromechanical Tungsten Silicide Cantilever Beams," Presented at the 36th National Symposium of American Vacuum Society, Boston, MA, October 23-29, 1989.
41. **D. Misra** and E.L. Heasell, "Annealing Behavior of Reactive Ion Etching Induced Deep Levels," 175th Meeting of the Electrochemical Society, 1989, Vol. 89-1, Abstract No. 168.
42. **D. Misra** and E.L. Heasell, "Side wall etching anisotropy due to CF₄ + O₂ RIE for the fabrication of V-groove emitter transistors," 172nd Meeting of the Electrochemical Society, 1987, Vol. 87-2, Abstract No. RNP - 1829.

VII.h. INVITED LECTURE SERIES, WORKSHOPS, AND SEMINARS

1. **D. Misra**, Micro-Fabricated Microconcentrator for Volatile Organic Compound Sensors, University of Toledo Nanotechnology Research Center. October 2, 2001.
2. **D. Misra**, Process-Induced Damage to Deep-Submicrometer CMOS Transistors, **ASM International**, NJ Chapter Meeting, January, 26, 1999.
3. D. Misra, Electron Transit Time Estimation in Photodiodes for Ultra High Frame Rate (UHFR) Burst Image Sensors, November 4, 1998. POEM Annual Research Review of Photonics, Princeton. NJ.
4. **D. Misra**, "Recent Trends in VLSI Design," August 17, 1998, **Software Technology Park Seminar**, at Kalinga Institute of Industrial Technology, Bhubaneswar, India.
5. **D. Misra**, "Polarity Dependent Plasma Charging Damage in sub-um MOSFETs," July 10, 1998, Center for Advanced Research in Electronics Seminar at Indian Institute of Technology, New Delhi, India.

6. **D. Misra**, "Process Induced Damage (Plasma Damage) To CMOS Electronic Chips" November 4, 1997, **Sigma Xi Seminar** at NJIT.
7. **D. Misra**, A 3-Dimensional Magnetic Sensor and Its Applications, University of Aizu, Aizu-Wakamashu, Japan, March 20, 1995.
8. **D. Misra**, Processing of Strained SiGe Materials, **ASM International**, NJ Chapter, NJ, January 24, 1995.
9. **D. Misra**, Processing of Strained SiGe Materials, University of Aizu, Aizu-Wakamashu, Japan, March 20, 1995.
10. **D. Misra**, Effect of Dry Etching to Si_{1-x}Ge_x Devices, Naval Research Laboratory, Washington, DC, June 25, 1993.
11. **D. Misra**, "Physics of IC Design and Technology," Institute of Physics, Bhubaneswar, India, June 14, 1991.
12. **D. Misra**, "Basic VLSI Design" and "Wafer Monitoring by Infrared Camera During Plasma Etching," Central Research Laboratory of Bharat Electronics Ltd, Bangalore, India, June 4-5, 1991.
13. **D. Misra**, "VIMDE - A Vertically Integrated Multi-Chip-Module Design environment," AT&T Engineering Expo'91, Princeton, NJ, March 5, 1991.
14. **D. Misra**, "Introduction to VLSI Design" IEEE Seminar Series, NJIT IEEE Students' Chapter, November, 1990.
15. **D. Misra**, "Signal Processing for Integrated Sensors," Presented at NJIT Microelectronics Seminar Series and Sigma Xi Lectures Fall 90, Newark, NJ, October 3, 1990.
16. **D. Misra**, "Integrated Magnetic Field Sensor," Presented at NJIT Day, SIEMENS Corporated Research Inc., Princeton, NJ, October 1989.
17. **D. Misra**, "Tungsten Silicide as Micromechanical Material," NATO Advanced Study Institute, Boca Raton, FL, July 17-28, 1989.
18. **D. Misra**, "A study of RIE-induced surface damage in VLSI applications," Microelectronics Seminar Series - Fall 86, Sponsored by Alberta Microelectronics Center and Department of Electrical Engineering, University of Alberta, Edmonton, Canada, October 1986.

VIII. RESEARCH GRANTS AND CONTRACTS

Principal Investigator (PI) or Co-PI

1. D. Misra, PI, Research in MEMS Using Bonded Wafers, **Sarnoff Corporation**, \$4,800.00, June 1, 2001 to December 2002.
2. D. Misra, Co-PI, New Jersey Center for Optoelectronics, **New Jersey Commission on Science and Technology**, \$75,000.00 (NJIT), March 1, 2001 to February 28, 2002 (With H. Grebel).

3. D. Misra, PI, A Micro-concentrator Interface for Real-time VOCs Sensors, **Center for Airborne Organics, An EPA Research Center at MIT**, with Prof. S. Mitra from Chem Eng. \$59,355.00, July 1, 2000 to December 31, 2001 (Amount allotted: Half of the total amount).
4. D. Misra, Co-PI, New Jersey Center for Optoelectronics, **New Jersey Commission on Science and Technology**, \$75,000.00 (NJIT share), March 1, 2000 to February 28, 2001 (with Prof. Grebel & Amount allotted: \$22,372).
5. D. Misra, Co-PI, Acquisition of Instrumentation for Deep Reactive Ion Etching of Bonded Ultra-Thin Silicon Wafers, **National Science Foundation**, \$467,380.00, July 15, 1998 to June 30, 1999 (With Prof.s Farmer and Mitra).
6. D. Misra, PI, Research Experience for Undergraduates (REU) Supplement Grant for Device And Materials Processing, **National Science Foundation**, \$10,000.00, January 1, 1999 to December 31, 2000.
7. D. Misra, PI, Acquisition of Specialized Instrumentation for Research & Development of Materials, Devices and Processes, **National Science Foundation**, \$55,000.00, July 15, 1998 to June 30, 1999.
8. D. Misra, Co-PI, New Jersey Center for Optoelectronics, **New Jersey Commission on Science and Technology**, \$85,000.00 (NJIT share), March 1, 1998 to February 28, 1999 (with Prof. Grebel & Amount allotted: \$22,000).
9. D. Misra, PI, Fabrication of Students' VLSI design projects tiny-chips through MOSIS, **National Science Foundation**, an educational supplemental grant of \$1,785, October 1997 to April 30, 1998.
10. D. Misra, PI, Investigation of Gate Oxides Grown on Light Deuterium Implanted Silicon Substrate, **Microelectronics Research Center**, NJIT, \$10,000, March 1, 1998 to June 30, 1999.
11. D. Misra, PI, Air-gap Capacitance to Improve Interconnect Delay, **Microelectronics Research Center**, NJIT, \$10,000, March 1, 1998 to June 30, 1999.
12. D. Misra, PI, "Two Part Nonvolatile Random Access Memory Using Conducting Polymer," **Infinite Computer Technologies (Air Force Office of Scientific Research , STTR Program)**, \$19,152.00, January 1, 1997 to December 31, 1997.
13. D. Misra, PI, "Two Part Nonvolatile Random Access Memory Using Indium," **Rubicon Inc. (National Science Foundation, SBIR Program)**, \$19,885.00, June 1, 1997 to November 30, 1997.
14. D. Misra, PI, "Silicon Photodetectors for Radiation Monitoring," **Radiation Monitoring Devices, Inc.**, \$19,000.00, Sept. 1, 1996 to Jan. 31, 1997.
15. D. Misra, PI, "Research for Advanced CMOS Process," **Sarnoff Corporation**, \$24,000.00, December 1996 to May 1997.
16. D. Misra, PI, "Design and Fabrication of Test Structures to Study the Reliability of Semiconductor Packaging," (Graduate Student Support & Training in Clean room) **Amkor Electronics Inc.**, \$74,000, July 1, 1996 to March 31, 1997.

17. D. Misra, PI, Equipment Grant, "Upgrade to 6" Wafer Processing," **Amkor Electronics Inc.**, \$15,000 (cash award), January 1997.
18. D. Misra. PI, "DLTS Measurement System," **Lucent Technologies (Allentown, PA)** Equipment donation, Equivalent cost \$10,000.00, May 1997.
19. D. Misra, PI, Research Experience for Undergraduates, **National Science Foundation**, a supplemental grant of \$10,000, Jan. 1, 1995 to Dec. 31, 1995
20. D. Misra, PI, Damage Elimination using an in-situ Contactless Sensor and Real Time Process Monitor During Plasma Etching in Microelectronic Manufacturing, **Center for Manufacturing Systems**, \$20,000, July 1, 1995 to June 30, 1996.
21. D. Misra, PI, Study of Defects and Process Induced Damage in Si_{1-x}Ge_x Materials, **National Science Foundation**, \$141,000.00, September, 1, 1992 to June 30, 1996.
22. D. Misra, PI, Study of Dry Etching Induced Damage in Silicon Dioxide, **SEMATECH Center of Excellence in NJ**, \$15,000, Aug. 1, 93 to Nov 30, 1993.
23. D. Misra, Co-PI, Very-High-Frame-Rate Solid-State Sensor, **New Jersey Commission on Science and Technology**, \$75,000, W.F. Kosonocky PI, July 1, 1993 to June, 30, 1994 (Amount allotted: \$30,000).
24. D. Misra, Co-PI, Design, Simulation and Prototype Fabrication of a Digital Compression Chip, **Digital Compression Technology, Inc.** \$130,000, Jan 4, 1993 to Dec 31, 1993. (Amount allotted: \$36,000).
25. D. Misra, PI, Use of MOSIS for fabrication of VLSI chips, **National Science Foundation**, an educational supplemental grant of \$4,750, October, 1991 to August 1992.
26. D. Misra, PI, Pre-Small Business Innovation Research Program, **Consortium For Surface Processing (ATC/SEM)**, \$5,000, October 1, 1991 - November 30, 1992.
27. D. Misra, PI, VLSI Design and Signal Processing Laboratory, **Sun Microsystems Inc.** \$12,295, June 1, 1992, Equipment.
28. D. Misra, PI, RIE Processed Micromechanical Systems (Cantilevers) Using Silicides, **Consortium For Surface Processing (ATC/SEM)**, \$27,600, June 1, 1989 - May 31, 1990.
29. D. Misra, PI, Use of MOSIS for fabrication of VLSI chips for Small Projects, **National Science Foundation**, an educational supplemental grant of \$5,500, October, 1990 to August 1991.
30. D. Misra, PI, Circuit Design, Analysis And Testing of A Novel CMOS Magnetic Field Sensor With A Temperature Compensation Scheme, **SIEMENS Corporate Research, Inc.** \$10,000, (June 1, 1989 - May 31, 1990).
31. D. Misra, PI, VIMDE - A Vertically Integrated Multi-Chip-Module Design Environment, **AT&T Foundation**, \$22,000, May 31, 1990.

32. D. Misra, PI, Electrical Breakdown Phenomena in Micromechanical Structures, **Consortium For Surface Processing (ATC/SEM)**, \$14,295, June 1, 1991 - May 31, 1992.
33. D. Misra, PI, VLSI Design Softwares, Autologic etc, **Mentor Graphics Corporation**, \$370,000.00, January 1992.
34. D. Misra, Co-PI, Wafer Monitoring During Plasma Etching by IR Camera, **SEMATECH Center of Excellence for Plasma Etching, Semiconductor Research Corporation**, \$30,000, with Prof. W.F. Kosonocky CP, July 1, 1989 - June 30, 1990 (Amount allotted: \$10,000).
35. D. Misra, Co-PI, Trade-Off Study and Design of a Foveating Image Sensor For High Speed data Capture, **Rutgers University CAIP Center** \$15,000, with Prof. W.F. Kosonocky, CP, July 1, 1988 - June 30, 1989 (Amount allotted: \$8,000).

VIII.a. PROPOSALS PENDING

- D.Misra, PI, Interface Hardening with Deuterium Implantation, **National Science Foundation**, \$390,133, October, 1, 2001.
- D. Misra, PI, Conducting Nanotubes for Smart Interconnect, **Semiconductor Research Corporation**, \$40,000, Sept 7, 2001.

VIII.b. UNFUNDED PROPOSALS

- D.Misra, PI, Interface Hardening with Deuterium Implantation, **National Science Foundation**, \$372,271, October, 1, 2000.
- D. Misra, ITR/EWF: Third International Conference on Information Technology, Bhubaneswar, India, December 21-23, 2000, **National Science Foundation**, \$7,000, February 1, 2000.
- D. Misra, PI, Investigation of Gate Oxides Grown on Deuterium Implanted Silicon Substrates, **National Science Foundation**, \$340,121, October, 1, 1999.
- D. Misra, PI, Process Induced Damage to VLSI Devices, **National Science Foundation**, \$337,665, October 1, 1999.
- D. Misra and S. Mitra, Co-PIs, Microconcentrator Interface for Chemical Sensors, **National Science Foundation**, \$389,155, June 4, 1999.
- D. Misra, PI, Plasma Charging Damage to VLSI Devices, **National Science Foundation**, \$308,320, October 24, 1997.
- D. Misra, PI, Acquisition of Instrumentation for Research and Development of Materials and Device Characterization, **Army Research Office, Office of Naval Research and Air Force Office of Scientific Research, (DURIP program)**, \$135,638, August 18, 1997.
- D. Misra, PI, Plasma Charging Damage to VLSI Devices, **New Jersey Commission on Science and Technology (TTP with Lucent Technologies)**, \$94,748, April 21, 1997.
- D. Misra, PI, Integration of MEMS and CMOS on Bonded Ultra-thin Silicon Wafer for Distributed Design and Fabrication Through Agile Networking, **National Science Foundation**, \$1,264,446, August 1996.
- D. Misra, Co-PI, Vertical Integration of Generalized Adaptive Neural Filters, **National Science Foundation**, (with N. Ansari and E.S.H. Hou), \$196,496, October 28, 1996.
- D. Misra, Co-PI, Low Light Level Solid State Sensors, SBIR proposal with Alphasat to **Dept of Defense**, \$100,000, July 1996.

- D. Misra, PI, Study of Deep Level Defects and Their Effects on InGaAs/InAsP Photodiodes, **New Jersey Commission on Science and Technology** (Innovative Partnership Program), \$76,088, February 1995.
- D. Misra, PI, Study of Deep Level Defects and Their Effects on InGaAs/InAsP Photodiodes, **National Science Foundation**, \$99,367, January 1995.
- D. Misra, PI, Damage Elimination using and in-situ Contactless Sensor and Real Time Process Monitoring During Plasma Etching in Microelectronic Manufacturing, **National Science Foundation**, \$195,992, September 1994.
- D. Misra, PI, Damage Elimination using and in-situ Contactless Sensor and Real Time Process Monitoring During Plasma Etching in Microelectronic Manufacturing, **Air Force Office of Scientific Research** (MURI), \$1,795,492, July 1994.

IX. PROFESSIONAL ACTIVITIES:

Electrochemical Society (ECS)

- Member of Electrochemical Society
- Serving in the **Executive Committee** of the **Dielectric Science and Technology Division** of the Society.
- Awards Committee Member, Solid State Science & Technology Award, Electrochemical Society, May 2000.
- Chair, Awards Committee, Thomas D. Callinan Award, Electrochemical Society, May 2000-Present.
- Chair, Membership Committee of Dielectric and Science Division of Electrochemical Society in May 1998 to May 2001.
- Providing Travel Grants and Awarded Memberships to Students all over the world to present a paper in all the ECS meetings since October 1998.

International Symposiums at ECS

- Co-organizer, International Symposium on *Silicon Nitride and Silicon Dioxide Thin Insulating Films – VI* at the 199th Meeting of Electrochemical Society at Washington, DC March 25-29, 2001.
- D. Misra: Session Chair, International Symposium on *Silicon Nitride and Silicon Dioxide Thin Insulating Films – VI* at the 199th Meeting of Electrochemical Society at Washington, DC March 25-29, 2001.
- Co-organizer, International Symposium on Microfabricated Systems And MEMS-V at the 198th Meeting of Electrochemical Society at Phoenix, Arizona October 22-27, 2000.
- D. Misra: Session Chair, International Symposium on Microfabricated Systems and MEMS V, 198th Meeting of Electrochemical Society, Phoenix, Arizona, October 22-27, 2000.
- Co-organizer, International Symposium on Plasma Etching Processes For Sub-Quarter Micron Devices at the 196th Meeting of Electrochemical Society and 1999 Joint International Meeting at Honolulu, Hawaii, October 17-22, 1999. Chaired a Session in the Symposium.
- Co-organizer, International Symposium Interconnects And Contact Metallization For ULSI at the 196th Meeting of Electrochemical Society and 1999 Joint International Meeting at Honolulu, Hawaii, October 17-22, 1999. Chaired a Session in the Symposium.
- Co-organizer, Student Poster Session at the 196th Meeting of Electrochemical Society and 1999 Joint International Meeting at Honolulu, Hawaii, October 17-22, 1999. Chaired the Session in the Symposium.

- Co-organizer, International Symposium on Fifth International Symposium On Silicon Nitride And Silicon Dioxide Thin Insulating Films, Processes and Reliability at the 195th Meeting of Electrochemical Society at Seattle, WA, May 1999. Chaired a Session in the Symposium.
- Organizer, Student Poster Session at the 195th Meeting of Electrochemical Society at Seattle, WA, May 1999. Chaired a Session in the Symposium.
- Co-organizer, International Symposium on Interconnect and Contact Metallization: Materials, Processes and Reliability at the 194th Meeting of Electrochemical Society at Boston, MA, November 1998. Chaired a Session in the Symposium.
- Co-organizer, Fifth International Symposium on Quantum Confinement: Nanostructures at the 194th Meeting of Electrochemical Society at Boston, MA, November 1998. Chaired a Session in the Symposium.
- Co-organizer, International Symposium on Microstructures and Microfabricated Systems IV at the 194th Meeting of Electrochemical Society at Boston, MA, November 1998. Chaired a Session in the Symposium.
- Organizer, Student Poster Session at the 194th Meeting of Electrochemical Society at Boston, MA, November 1998. Chaired a Session in the Symposium.
- Co-organizer, International Symposium on Plasma Processing at the 193rd Meeting of Electrochem Soc at San Diego, CA, May 1998. Chaired a Session in the Symposium.
- Organizer, Student Poster Session at the 193rd Meeting of Electrochemical Society at San Diego, CA, May 1998. Chaired a Session in the Symposium.

Institute of Electrical and Electronics Engineers (IEEE)

- Associate Editor, IEEE Circuits and Device Magazine.
- Senior Member of the IEEE
- D. Misra: Editorial Board Meeting, IEEE Circuits and Devices Magazine, Orlando, FL, Nov. 18, 2000.
- D. Misra: Editorial Board Meeting, IEEE Circuits and Devices Magazine, San Francisco, CA, June 23, 2001.
- D. Misra, Treasurer, IEEE North Jersey Section, Jan. – Dec. 2001.
- 2000 (elected) Member at Large of the North Jersey Section of the IEEE.
- Presently serving as the Associate Chair of Electron Device Society and Circuit and Systems division of the North Jersey Section of IEEE.
- Represented North Jersey Section of IEEE since 1997 the National Meeting of the Electron Device Society at IEDM.
- Organizing seminars at NJIT campus for IEEE.
- A constant reviewer of articles for International Journals such as IEEE Transaction on Electron Devices, IEEE Electron Device Letters.

International Conference on Information Technology

- D. Misra: Session Chair, VLSI Technology Session, VLSI Design 2001, 14th International Conference on VLSI Design, January 5, 2001.
- D. Misra: Session Chair, Session for Keynote Papers, International Conference on Information Technology, Bhubaneswar, India, Dec. 21-23, 2000.
- Served as the **Program Chair** of International Conference on Information Technology, CIT'2000, in Bhubaneswar, India, December 21-23, 2000.

- Served as the **Tutorial Chair** of International Conference on Information Technology, CIT'99, in Bhubaneswar, India, December 20-22, 1999.
- Served in the **Technical Program Committee** of International Conference on Information Technology, CIT'98, in Bhubaneswar, India, December 21-23, 1998.
- Submitted a proposal to NSF to support CIT'2000.

Reviewing Activities

- Regular Reviewer of articles for International Journals:
 IEEE Transaction on Electron Devices
 IEEE Electron Device Letters
 IEEE/ECS Electrochemical and Solid-State Letters
 IEEE Transaction on Circuit and Systems
 Journal of the Electrochemical Society
 Journal of Physics D: Applied Physics
 Journal of Micromechanics and Microengineering
 Material Science in Semiconductor Processing
 Semiconductor Science & Technology
 Grant Proposals for National Science Foundation.
- Awarded Membership of The Institute of Physics, London, 2000 for Reviewing Activities.
- Served as a Panel Member in Enabling Technology Division (ECS) of NSF in June 1998 to review 24 proposals.
- Served as a Panel Member in Enabling Technology Division (ECS) of NSF in May 2001 to review 8 individual MRI proposals and 34 proposals in the panel.

University Service

- Provided an outstanding service with leadership as the Acting Director of Microelectronics Research Center in 1996-97 Academic Year.
- Provided an outstanding service as a Mentor for University Research Experience program for Undergraduates in Equal Opportunity Program, New Jersey State Minority Academic Career Program, McNair Fellow Program (99-00) for last several years (since 1995-96).

University Committees

- Served, and currently serving in the University Research Committee
- Serving in the Graduate Studies Committee for Best Thesis
- Served in the Academic Computing Committee
- Served as the Library Committee

Departmental Committees

- Director, MS Electrical Engineering Program.
- Served in the Chairperson Search Committee (elected)
- Currently serving in (i) Committee of Committees (elected), (ii) Doctoral Committee, (iii) Financial Aid Committee.
- Served as the Computer Engineering Faculty Search Committee for two academic years in 1997-98 and 1998-99.
- Served as the Chair of the departmental A&V committee.

- Served as the Assistant Director of the Electronic Imaging Center at NJIT and established the VLSI/CAD facility for the Center.

PUBLIC SERVICE

- Participated as a Panel Member at the One day Workshop on Rebuilding Orissa (India) after Killer Cyclone on Saturday, February 5, 2000, University of Maryland, College Park, MD, USA
- An active volunteer member at the “Sustainable Economic and Educational Developmental Society (SEEDS) [<http://www.seedsnet.org>]. SEEDS has been active to promote educational and economic progress and development for the common folks particularly in Orissa, but in the developing world in general. SEEDS in principle, also would take stand against social evils and injustices whenever possible. SEEDS best hope that these, in turn, would indirectly bring about and foster the other important ingredient – political consciousness and empowerment-- among the people.
- Serving as a fund raiser and volunteer for the Orissa Cyclone Relief Program
- Served as Vice President of Orissa Society of Americas’ New York Chapter.
- Served as an advisor to Association of Indian Students at NJIT.
- Served as an organizer for the 25th National Convention of Orissa Society of Americas in 1994.
- Member SPIE, Sigma Xi.

X. SIGNIFICANT CONTRIBUTION To Sub- μ m Semiconductor Device Reliability & Fabrication

This section outlines my contribution to sub-micrometer semiconductor device reliability due to advanced fabrication principles. Various new processes induce damage/defects in traditionally reliable devices. My contribution focuses in understanding the process-induced damage mechanisms in semiconductor devices and define alternate or additional fabrication techniques to prevent the damage/defect formation thereby improve device reliability. Following are the details of the projects describing the research activities and results.

1. For the 1st time we have demonstrated that incorporation of deuterium at the silicon-silicon dioxide interface using ion implantation before gate oxide growth is an effective means to improve the oxide quality and may be a viable alternative to many hours of annealing through a middle-of-line or backend process. Deuterium implantation brings about a clear enhancement in gate oxide quality by improving the oxide leakage current and capacitance voltage characteristics. A reduction in density of interface traps D_{it} as obtained from the conductance measurements for the deuterium-implanted devices suggests that deuterium implantation contributes to the passivation of the P_b centers at the interface.
2. Plasma damage immunity of gate oxide grown on very low dose N+ implanted silicon is found to be improved comparing to regular gate oxide of similar thickness ($\sim 5\text{nm}$).
3. It was found that MOSFET noise increase and hot carrier life-time degradation due to plasma damage is strongly dependent on the damage polarity (depending on the direction of current flow during damage). Transistor source and drain junctions do contribute to the plasma damage during metal etching.
4. When samples went through annealing after phosphorus being implanted into strained SiGe layer at room temperature band gap of SiGe increases and misfit strain decreases. Deep defect levels

that were observed due to P-implantation, which can be explained by considering presence of permanent dislocation loops causing strain relaxation.

5. Plasma etching does modify the coherently strained Si/SiGe/Si heterostructures. Electrically active defects were observed when deep level transient spectroscopy was employed to investigate the plasma damage. These defects change energy when annealed at different temperatures in a particular way indicating that point defects are formed due to plasma exposure and these point defects condensing into dislocation loops, which eventually shrink and disappear as the annealing temperature is increased. We verified this behavior electrically and physically (TEM).
6. Change in valence band discontinuity is noticed in plasma etched and subsequently annealed coherently strained SiGe films due to strain relaxation. C-V method is turned out to be a simple, fast and efficient approach to estimate any band gap modifications due to process-induced damage.
7. Designed and experimentally verified a 3-dimensional BiCMOS Magnetic Field Sensor. Cross-sensitivity was a major problem in 3-D magnetic sensors. In our design cross-sensitivity was completely eliminated.