

# Enhanced SiO<sub>2</sub> Reliability on Deuterium-Implanted Silicon

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**Abstract**—Stress-induced leakage current and time-dependent dielectric breakdown were investigated to examine the reliability of gate oxides grown on hydrogen- and deuterium-implanted silicon substrates. An order of magnitude improvement in charge-to-breakdown was observed for the deuterium-implanted devices as compared with the hydrogen-implanted ones. Such reliability improvement may be explained by the reduction of defects in the SiO<sub>2</sub> and Si/SiO<sub>2</sub> interface, such as Si dangling bonds, weak Si-Si bonds, and strained Si-O bonds due to the retention of implanted deuterium at the interface and in the bulk oxide as confirmed by secondary ion mass spectroscopy.

**Index Terms**—Constant voltage stress, dangling bond passivation, deuterium implantation, hydrogen implantation, isotope effect, oxide breakdown, SILC.

## I. INTRODUCTION

THE BREAKDOWN characteristics of ultrathin SiO<sub>2</sub> film that serves as gate dielectric in silicon MOSFET is one of the important issues for the miniaturization of ultralarge-scale integration (ULSI) devices. Deuterium incorporation compared with that of hydrogen at the Si/SiO<sub>2</sub> interface is known to improve the device reliability characteristics [1], [2] because deuterium desorption is substantially reduced as compared with hydrogen desorption due to isotope effect. Suppressed stress-induced leakage current (SILC) was observed under Fowler–Nordheim (F–N) injection when oxide was formed by deuterium pyrogenic oxidation [3]. Recently, various methods [4], [5] were used to incorporate deuterium at the Si/SiO<sub>2</sub> interface, including annealing [6]–[8].

Deuterium incorporation through implantation in middle-of-line process [9], [10] has minimal impact. On the other hand, deuterium implantation before gate oxide growth can be optimized to precisely control the incorporation of deuterium atoms [11], [12]. The use of implantation before the growth of gate oxide can effectively retain deuterium ions at the interface and in the bulk of the oxide. In addition, deuterium implantation can sustain larger thermal budget as compared with deuterium annealing. Due to the presence of sidewall spacers, deuterium diffusion can have a localized effect, such as higher concentration at the drain and source end of the channel if deuterium annealing is used. Deuterium implantation, on the other

hand, can provide a spatially uniform distribution of deuterium throughout the channel.

Inasmuch as the implantation is carried out before the growth of the gate oxide, it is expected that this process does not affect the integrity of the gate oxide. However, the reliability of this oxide is still unknown. In this paper, we present the SILC and breakdown characteristics of oxide grown on hydrogen- and deuterium-implanted silicon substrates. Suppression of the trap creation and SILC was observed under F–N stressing condition due to retention of deuterium at the Si/SiO<sub>2</sub> interface and bulk SiO<sub>2</sub> as determined by SIMS analysis.

## II. EXPERIMENTAL

Deuterium and hydrogen were implanted into a 5-in p-type Si wafer with a resistivity of 0.8–1.2 Ω · cm through a 20-nm-thick sacrificial oxide with an implantation energy of 20 keV with a dose of  $1 \times 10^{14}$  atoms/cm<sup>2</sup>. The energy and dose optimization results are published elsewhere [11]. The wafer without any implantation was used as control. Following the removal of the sacrificial oxide, dry oxidation was used to grow 6.5 nm of gate oxide at 800 °C for 30 min with a flow rate of 750-sccm N<sub>2</sub> and 500-sccm O<sub>2</sub>. Al of 3000 Å was immediately deposited to form MOS capacitors. The oxide thickness was measured using an ellipsometer on 13 sites, and ±3-Å variation across the wafer was found. The oxide thickness for the hydrogen-implanted samples was ~10% higher as compared with the deuterium-implanted devices. This was also compared with the thickness estimated from the electrical measurements [capacitance–voltage (C–V) measurements], which yielded similar results. After back metallization, a postmetal annealing was carried out at 400 °C for 20 min. The oxide was evaluated by measuring the prestress and poststress characteristics after applying a constant voltage stress (CVS) of 9.2 MV/cm on capacitors with 100-μm diameter. HP 4156A semiconductor parameter analyzer and 4284 LCR meter were used for all measurements.

## III. RESULTS AND DISCUSSIONS

Fig. 1 shows the  $J-E_{OX}$  characteristics before and after the MOS capacitors were subjected to a low stress level at a CVS (gate negative) with a field of 9.2 MV/cm for 500 s. A higher poststress leakage current was observed for the hydrogen-implanted devices as compared with the deuterium-implanted ones. All hydrogen-implanted devices showed similar results. The SILC for the hydrogen case in the entire sweeping voltages indicates a large increase of oxide traps, leading to a soft breakdown-like characteristics.

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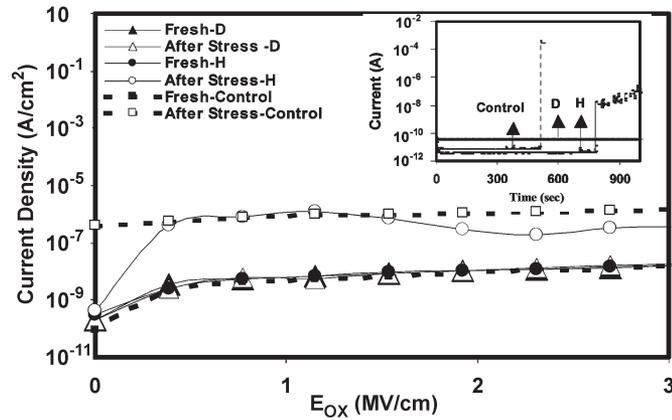


Fig. 1.  $J$ - $E_{OX}$  curves of the deuterium- and hydrogen-implanted devices before and after a CVS of  $-6$  V for 500 s. An increase in the leakage current was observed for the hydrogen samples (circles) as compared with the deuterium samples (triangles). The leakage current of the control sample (squares) has also been monitored after a CVS of  $-6$  V for 400 s. The inset shows the gate current versus the stress time plot for the control, hydrogen-implanted, and deuterium-implanted samples.

It is well known that under the CVS conditions, the injected electrons from the cathode gain kinetic energy from the oxide field and, upon reaching the anode, break the Si-H, SiOH, and strained Si-O bonds. The released hydrogen/holes, while traveling toward the cathode, create oxide traps [13]. SILC is attributed to the generated bulk traps that contribute to trap-assisted tunneling [14]. The traps created in the bulk of the oxide by the released hydrogen from the interface during stress therefore contributed to an increase in the poststress leakage current in the hydrogen-implanted devices. The suppressed SILC for the deuterium implantation case, on the other hand, demonstrates an isotope effect, as it is more difficult to break the Si-D bonds as compared with the Si-H bonds at the interface [15], contributing to less trap creation within the bulk oxide. The leakage current for the control sample (no implantation) was also monitored, as shown in Fig. 1. It is observed that the poststressed leakage current of the control sample increases as compared with the hydrogen and deuterium samples at 0 V.

The observed current versus time during the stress is shown in the inset of Fig. 1. Hydrogen-implanted devices show a fluctuation in the gate current, which also indicates a soft breakdown behavior, whereas the breakdown of the deuterium-implanted devices extended beyond 1000 s without any such fluctuations. For the control samples, oxide breakdown was observed at around 500 s. The higher leakage current observed for the deuterium-implanted devices is due to the lower oxide thickness obtained during oxidation as compared with the hydrogen-implanted case [16]. It should be noted that higher desorption rate for hydrogen, which is  $1.6\times$  that of deuterium [17], leads to a lower oxide growth rate in the deuterium-implanted case as the diffused hydrogen/deuterium takes part in the oxidation process. Lee *et al.* observed a similar effect during the oxide growth conducted after deuterium prebake [5].

The flat-band voltage shift  $\Delta V_{FB}$  before and after stress is observed in the ( $C$ - $V$ ) measurement, as shown in Fig. 2. The shift in the poststressed ( $C$ - $V$ ) curves toward the positive gate voltage direction is attributed to the creation of net negatively charged centers in the bulk oxide due to electron trapping

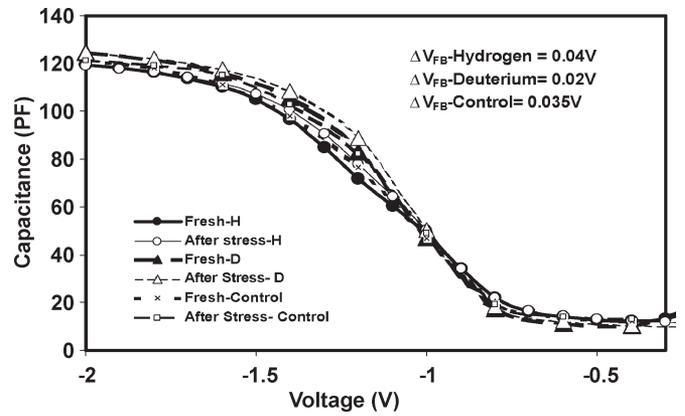


Fig. 2. High-frequency ( $C$ - $V$ ) curves (1 MHz) for the hydrogen (circles), deuterium (triangles), and control samples (squares) before and after stress of  $-6$  V for 200 s, which show a larger flat-band voltage shift  $\Delta V_{FB}$  for the hydrogen case.

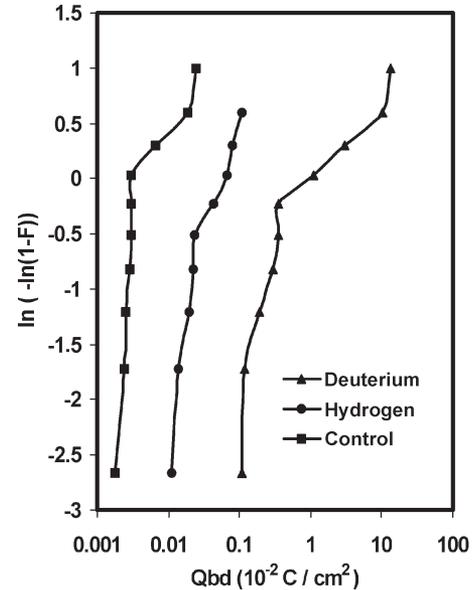


Fig. 3. Weibull plots for charge-to-breakdown showing the comparison between the control (no implantation), hydrogen-implanted, and deuterium-implanted devices at a stress level of  $-7$  V.

[18]. However, a reduced  $\Delta V_{FB}$  of 20 mV for the deuterium-implanted samples indicate a suppressed electron trap creation in the oxide. The reduced electron trap concentration in the gate oxide further supports the lower SILC observed for the deuterium-implanted devices. The lower value of capacitance in the accumulation region for the hydrogen-implanted devices is attributed to a higher oxide thickness as compared with the deuterium-implanted case.

Fig. 3 illustrates the cumulative failure versus the charge-to-breakdown  $Q_{BD}$  for control, hydrogen-implanted, and deuterium-implanted samples under CVS with a voltage of 7 V (gate negative). It is clearly seen that the devices with deuterium implantation exhibits a significantly higher  $Q_{BD}$ , the difference being an order of magnitude greater (considering at the 63% failure level) in comparison with the hydrogen and control devices. Given the limited number of devices tested, the interpretation of the breakdown distribution becomes difficult. However, if we take into consideration the

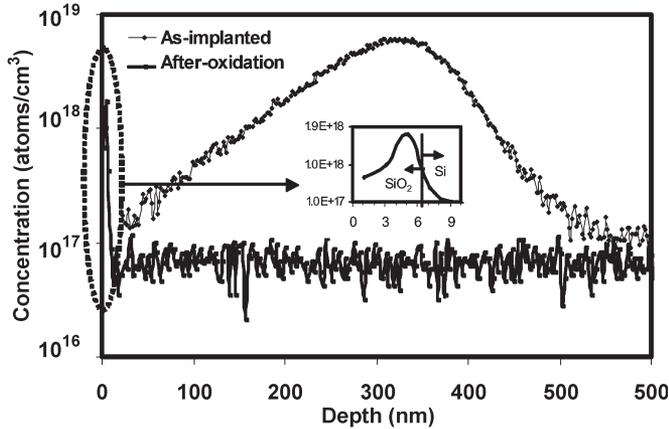


Fig. 4. SIMS concentration profile for deuterium shows a peak concentration of  $6 \times 10^{18}/\text{cm}^3$  for 20 keV with a dose of  $1 \times 10^{14}/\text{cm}^2$  at 325 nm immediately after deuterium implantation. The inset shows a peak deuterium concentration of  $1.7 \times 10^{18}/\text{cm}^3$  after gate oxidation showing a peak within the oxide 1.5 nm from the Si/SiO<sub>2</sub> interface and an interface deuterium concentration of  $7.8 \times 10^{17}/\text{cm}^3$ .

error bars for each measurement, a single Weibull slope can be extracted. The breakdown distribution therefore clearly indicates that the overall  $Q_{BD}$  is significantly greater for the deuterium-implanted devices due to the presence of deuterium. Furthermore, deuterium-implanted devices show an enhanced reliability for higher electric fields for the same voltage level, the thickness of the deuterium-implanted devices being smaller as compared with the hydrogen-implanted and control samples.

The larger charge-to-breakdown of the deuterium-implanted devices is attributed as due to less electron trap creation, as it is known that the electron traps created in the gate oxides during F–N injection are an important precursor leading to oxide breakdown [19]. Suppression of trap creation is clearly evident due to the presence of deuterium in the oxide and at the interface.

Secondary ion mass spectroscopy (SIMS) confirms the presence of deuterium, as shown in Fig. 4. Retention of deuterium is clearly evident after gate oxidation (inset). SIMS profiles show a peak concentration of  $6 \times 10^{18}/\text{cm}^3$  at a depth of 325 nm immediately after the deuterium implantation. After gate oxide growth, the concentration of deuterium reduces to the background level in the bulk silicon, whereas it peaks within the oxide near the Si/SiO<sub>2</sub> interface at a depth of 5 nm with a concentration of  $1.7 \times 10^{18}/\text{cm}^3$ . At the interface deuterium, concentration is found to be  $7.8 \times 10^{17}/\text{cm}^3$ , which is much larger than the ideal concentration of the dangling bonds at the Si/SiO<sub>2</sub> interface. The change in concentration and peak shift indicate that the implanted ions diffuse toward the surface due to the chemical potential difference between SiO<sub>2</sub> and Si [12]. Inasmuch as deuterium has a lower activation energy for diffusion in SiO<sub>2</sub> as compared with silicon [20], deuterium atoms pile up in the oxide near the interface during oxidation.

Fig. 5 shows the extracted interface state density  $D_{it}$  for both hydrogen and deuterium devices evaluated using the conductance technique [21] immediately after the oxide growth before any applied stress. An identical passivation was observed for both hydrogen- and deuterium-implanted devices with a trap density of  $6.94 \times 10^{10} \text{ eV}^{-1} \cdot \text{cm}^{-2}$  at the energy level of 0.35 eV in the Si band gap. Dangling bonds at the interface  $P_{b0}$

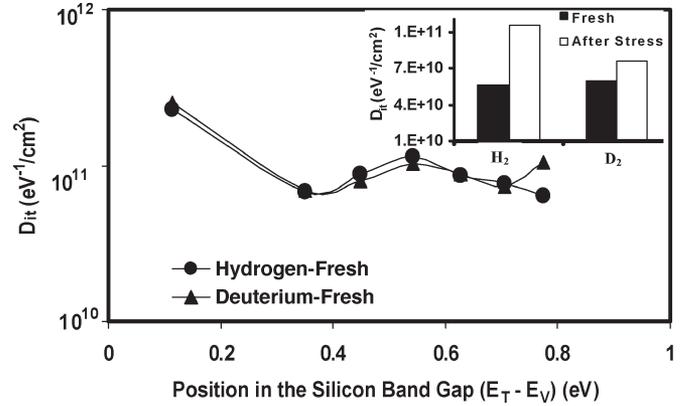


Fig. 5.  $D_{it}$  distribution for deuterium- and hydrogen-implanted devices before stress shows an identical passivation of the interface. The inset shows a fivefold increase in the value of  $D_{it}$  for the hydrogen case as compared with the deuterium case after a  $-6\text{-V}$  CVS for 200 s.

are known to be one of the major contributors for the interface state density [22] and have their  $(0 \rightarrow 1)$  electron transition approximately at 0.3 eV and  $(1 \rightarrow 2)$  transition at 0.85 eV above the valance band edge [23]. In our case, the passivation of the dangling bonds brings about a reduction in the density of  $P_{b0}$  centers at 0.35 eV, suggesting a clear passivation of interface states for both the hydrogen- and deuterium-implanted devices. However, when the devices were subjected to a CVS for 100 s,  $D_{it}$  was found to increase by  $5\times$  in case of the hydrogen-implanted case as compared with the deuterium case, as shown in the inset of Fig. 5.  $D_{it}$  generation due to hydrogen release at the Si/SiO<sub>2</sub> interface was further confirmed by the poststress interface trap generation where deuterium implantation showed significant improvement.

We have therefore observed from the preceding measurements that deuterium atoms incorporated by implantation diffuse to the Si/SiO<sub>2</sub> interface, react with the interface dangling bonds, weak Si–Si bonds, and strained Si–O [24] bonds, and are also incorporated in the bulk SiO<sub>2</sub> as evidenced by the postoxidation SIMS concentration profile. During oxidation, the diffused deuterium atoms that are introduced in the bulk SiO<sub>2</sub> structure possibly contribute to the construction of the SiO<sub>2</sub> film being incorporated in the SiO<sub>2</sub> network [3]. It has been reported that the strength of the Si–OD bonds formed during oxidation is larger than that of the Si–D bonds, which passivates the interface defects [16]. Gerardi *et al.* reported that the stability of the Si–H bond increases when the silicon atoms form bonds with the larger electronegative oxygen atoms [25]. Furthermore, thermal desorption spectroscopy data suggest that the activation energy of desorption is 7% higher when deuterium participated in the oxidation process as compared with the deuterium annealing [26].

The presence of deuterium at the interface and in the bulk oxide therefore suppresses deuterium release, which triggers defect generation [13] at the interface and in the bulk region under F–N stress. Therefore, the deuterium atoms incorporated into both the Si/SiO<sub>2</sub> interface and the bulk SiO<sub>2</sub> by implantation play an important role in the suppression of the electron trap creation under F–N stress, which yields a suppressed SILC,  $D_{it}$ ,  $\Delta V_{FB}$ , and higher  $Q_{BD}$  as deuterium has a lower desorption rate due to the resonance between the Si–D bond

bending mode and the transverse optical phonon of the bulk silicon [15].

Inasmuch as the optimized condition for effective deuterium passivation for a 65-Å oxide has been obtained for a 20-keV energy and a  $1 \times 10^{14}/\text{cm}^2$  dose of implantation [12], use of similar conditions for a thinner oxide may not lead to the desired passivation effect due to variation in thermal budget. For oxide scaling, i.e., thinner oxides, the energy and dose of implantation need to be selected appropriately for optimum results. Lower energy of implantation can be used to obtain effective interface and oxide passivation in thinner oxide as the peak concentration depth decreases [27], which will lead to the interface during the oxide growth.

#### IV. CONCLUSION

We have demonstrated a reliability improvement of gate oxide grown on deuterium-implanted silicon substrate under CVS. The SILC and breakdown measurements show that the deuterium-implanted oxides resulted in an order of magnitude improvement as compared with the hydrogen-implanted ones. Results also indicate that implantation can be used as an alternative technique to incorporate deuterium atoms at the Si/SiO<sub>2</sub> interface as there is a strong evidence of reduced trap creation induced by the release of hydrogen species and due to the nature of the chemical bonding of the atoms inside the oxide and at the interface.

#### REFERENCES

- [1] J. W. Lyding, K. Hess, and I. C. Kizilyalli, "Reduction of hot electron degradation in metal oxide semiconductor transistors by deuterium processing," *Appl. Phys. Lett.*, vol. 68, no. 18, pp. 2526–2528, Apr. 1996.
- [2] K. Hess, I. C. Kizilyalli *et al.*, "Giant isotope effect in hot electron degradation of metal oxide silicon devices," *IEEE Trans. Electron Devices*, vol. 45, no. 2, pp. 406–416, Feb. 1998.
- [3] H. Y. Mitani, H. Satake, H. Itoh, and A. Toriumi, "Suppression of stress induced leakage current after Fowler–Nordheim stressing by deuterium pyrolytic oxidation and deuterated poly-Si deposition," in *IEDM Tech. Dig.*, 2002, vol. 49, p. 1192.
- [4] H. Kim and H. Hwang, "High-quality ultrathin gate oxide prepared by oxidation in D<sub>2</sub>O," *Appl. Phys. Lett.*, vol. 74, no. 5, pp. 709–710, Feb. 1999.
- [5] M. H. Lee, C. H. Lin, and C. W. Liu, "Novel methods to incorporate deuterium in MOS structures," *IEEE Electron Device Lett.*, vol. 22, no. 11, pp. 519–521, Nov. 2001.
- [6] H. C. Mogul, L. Cong, R. M. Wallace, P. J. Chen, T. A. Rost, and K. Harvey, "Electrical and physical characterization of deuterium sinter on submicron devices," *Appl. Phys. Lett.*, vol. 72, no. 14, pp. 1721–1723, Apr. 1998.
- [7] I. J. R. Baumvol, E. P. Gusev, F. C. Stedile, F. L. Freire, M. L. Green, and D. Brasen, "On the behavior of deuterium in ultrathin SiO<sub>2</sub> films upon thermal annealing," *Appl. Phys. Lett.*, vol. 72, no. 4, pp. 450–452, Jan. 1998.
- [8] P. J. Chen and R. M. Wallace, "Deuterium transport through device structures," *J. Appl. Phys.*, vol. 86, no. 4, p. 2237, 1999.
- [9] T. A. Rost and K. C. Harvey, "Method for improving performance and reliability of MOS technologies and data retention characteristics of flash memory cells," U.S. Patent 6 221 705, Apr. 24, 2001.
- [10] K. C. Harvey, "Method to enhance deuterium anneal/implant to reduce channel-hot carrier degradation," U.S. Patent 6 017 806, Jan. 25, 2000.
- [11] T. Kundu and D. Misra, "Si-SiO<sub>2</sub> interface passivation using hydrogen and deuterium implantation," *Electrochem. Solid-State Lett.*, vol. 8, no. 2, pp. G35–G37, 2005.
- [12] H. Park and C. R. Helms, "The effect of annealing treatment on the distribution of deuterium in silicon and in silicon/silicon oxide systems," *J. Electrochem. Soc.*, vol. 139, no. 7, p. 2042, 1992.
- [13] D. J. Maria and J. W. Stasiak, "Trap creation in silicon dioxide produced by hot electrons," *J. Appl. Phys.*, vol. 65, no. 6, pp. 2342–2356, Mar. 1989.
- [14] R. Moazzami and C. Hu, "Stress induced current in thin silicon dioxide films," in *IEDM Tech. Dig.*, 1992, p. 139.

- [15] R. Biswas, Y.-P. Li, and B. C. Pan, "Enhanced stability of deuterium in silicon," *Appl. Phys. Lett.*, vol. 72, no. 26, pp. 3500–3502, Jun. 1998.
- [16] Y. Mitani, H. Satake, H. Itoh, and A. Toriumi, "A study of the effect of deuterium on stress induced leakage current," *Jap. J. Appl. Phys.*, vol. 39, no. 6B, pp. L564–L566, Jun. 2000.
- [17] K. Sinniah, M. G. Sherman, B. Lisa, W. Henry, J. T. Yates, and K. C. Janda, "Hydrogen desorption from monohydride phase on Si (100)," *J. Chem. Phys.*, vol. 92, no. 9, p. 5700, 1990.
- [18] E. Harari, "Dielectric breakdown in electrically stressed thin films of thermal SiO<sub>2</sub>," *J. Appl. Phys.*, vol. 49, no. 4, pp. 2478–2489, Apr. 1978.
- [19] D. J. Dumin, S. K. Mopuri, S. Vachinatham, R. S. Scott, R. Subramaniam, and T. G. Lewis, "High field related thin oxide wearout and breakdown," *IEEE Trans. Electron Devices*, vol. 42, no. 4, pp. 760–772, Apr. 1995.
- [20] R. Rodriguez, E. Miranda, R. Pau, J. Sune, M. Nafria, and X. Aymerich, "Monitoring the degradation that causes the breakdown of ultrathin (< 5 nm) SiO<sub>2</sub> gate dielectrics," *IEEE Electron Device Lett.*, vol. 21, no. 5, pp. 251–253, May 2000.
- [21] S. M. Meyers, "Interaction of deuterium gas with dry SiO<sub>2</sub> on Si: An ion beam study," *J. Appl. Phys.*, vol. 61, no. 12, pp. 5428–5437, Jun. 1987.
- [22] M. J. Uren, K. M. Brunson, J. H. Stathis, and E. Cartier, "Potential fluctuations due to Pb centers at the Si/SiO<sub>2</sub> interface," *Microelectron. Eng.*, vol. 36, no. 1–4, pp. 219–222, Jun. 1997.
- [23] E. H. Poindexter, P. J. Caplan, B. E. Deal, and R. R. Razouk, "Interface states and electron spin resonance in thermally oxidized (111) and (100) silicon wafers," *J. Appl. Phys.*, vol. 52, no. 2, pp. 879–884, Feb. 1981.
- [24] T. Y. Luo, M. Laughery, G. A. Brown, H. N. Al-Shareef, V. H. C. Watt, A. Karamcheti, M. D. Jackson, and H. R. Huff, "Effect of H<sub>2</sub> content on reliability of ultrathin *in-situ* steam generated (ISSG) SiO<sub>2</sub>," *IEEE Electron Device Lett.*, vol. 21, no. 9, pp. 430–432, Sep. 2000.
- [25] G. J. Gerardi, E. H. Poindexter, and P. J. Caplan, "Electrical activity of interfacial paramagnetic defects in thermal (100) Si/SiO<sub>2</sub>," *Appl. Phys. Lett.*, vol. 49, no. 6, pp. 348–350, Aug. 1998.
- [26] C. L. Darling and H. B. Schlegel, "Heats of formation of SiHnO and SiHnO<sub>2</sub> calculated by ab initio molecular orbital methods at the G2 level of theory," *J. Phys. Chem.*, vol. 97, no. 31, pp. 8207–8211, 1993.
- [27] T. Kundu and D. Misra, "Annealing effect on reliability of SiO<sub>2</sub> for deuterium implanted silicon," *Phys. Chem. SiO<sub>2</sub> Si-SiO<sub>2</sub> Interface-V—ECS Trans.*, vol. 1, no. 1, p. 221, 2005.



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