VLSI Design - I
(Computer Aided Physical Design)

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Introduction to Digital VLSI Design

• Historical Prospective
• Design Process, Methodology and Hierarchy
  • VLSI Technology Trends
  • Problems of VLSI Design
  • Nanotechnology
  • Impact on VLSI Designers
  • History of VLSI Design
  • Today’s trend

A Brief History

• 1958: First integrated circuit
  – Flip-flop using two transistors
  – Built by Jack Kilby at Texas Instruments
• 2003
  – Intel Pentium 4 processor (55 million transistors)
  – 512 Mbit DRAM (> 0.5 billion transistors)
• 53% compound annual growth rate over 45 years
  – No other technology has grown so fast so long
• Driven by miniaturization of transistors
  – Smaller is cheaper, faster, lower in power!
  – Revolutionary effects on society
Birth of Modern Electronics 1947
AT&T Bell Laboratories – Invention of Point Contact Transistor
William Shockley, Walter Brittain, and John Bardeen
Winners of the 1956 Nobel Prize in Physics

Solid-State Electronics Goes Commercial -- 1950
AT&T Bell Laboratories – Junction Transistor

Microelectronic Revolution -- 1958
The First Integrated Circuit – Jack Kilby, Texas Instruments
1 Transistor and 4 Other Devices on 1 Chip
Winner of the 2000 Nobel Prize
The Planar Process -- 1959
A More Efficient Way to Make Transistors
Fairchild Electronics -- Jean Hoerni and Robert Noyce

First Commercial Planar IC
Fairchild -- One Binary Digital (Bit) Memory Device on a Chip
4 Transistors and 5 Resistors
START OF SMALL SCALE INTEGRATION TECHNOLOGY

A New Form of Transistor -- 1962
Metal-Oxide Semiconductor Field-Effect Transistor
Radio Corporation of America (RCA) Sarnoff Laboratories
First Linear IC -- 1964
The μA 702 OPAMP – Fairchild

First General-Purpose Microprocessor -- 1974
8-Bit Intel 8080, Intel Corporation – 4,500 Transistors

First IC Created with Computer-Aided Design -- 1967
μMOSAIC – Fairchild
First 1,024 Bit Memory Chip -- 1970
Intel Corporation DRAM

First 256-Bit Static RAM -- 1970
The Fairchild 4100

First EPROM -- 1971
The INTEL 1702
**Birth of the Microprocessor -- 1971**
The Intel 4004 – 2,300 Transistors
THE FIRST COMPUTER ON A SINGLE CHIP
BEGINNING OF LARGE SCALE INTEGRATION TECHNOLOGY

**Driver of the Late 1970’s**
**Minicomputer Revolution -- 1975**
Advanced Micro Devices 2901 BIT-SLICE MICROPROCESSOR
WELL INTO THE MEDIUM SCALE INTEGRATION ERA

**First 65,536 Bit Dynamic Memory Chip -- 1977**
IBM Corporation
One of the Most Powerful 16-Bit Microprocessors -- 1979
The Motorola 68000
WELL INTO THE LARGE SCALE INTEGRATION ERA

First 294,912 Bit Dynamic RAM Memory -- 1981
IBM Corporation

A Very Early 32-Bit Microprocessor -- 1981
The HP Focus Chip, Hewlett-Packard Co. – 450,000 Transistors
THE VERY LARGE SCALE INTEGRATED CIRCUIT ERA BEGINS
**VLSI Technology Trends**

- Source: International Technology Roadmap for Semiconductors – Semiconductor Industry Association
- NSF, NIST, Depts. of Commerce, Defense, & Energy, Semiconductor Research Corporation, International SEMATECH
- Assumptions:
  - Moore’s Law continues to hold
  - DRAM bit count goes up 4 times every 3 yrs. to 2010
  - Si CMOS -- > 75 % of world’s semiconductors

**Moore’s Law**

- 1965: Gordon Moore plotted transistor on each chip
  - Fit straight line on semilog scale
  - Transistor counts have doubled every 26 months

<table>
<thead>
<tr>
<th>Integration Levels</th>
<th>Transistor Count</th>
</tr>
</thead>
<tbody>
<tr>
<td>SSI: 10 gates</td>
<td>1,000,000</td>
</tr>
<tr>
<td>MSI: 1000 gates</td>
<td>10,000,000</td>
</tr>
<tr>
<td>LSI: 10,000 gates</td>
<td>100,000,000</td>
</tr>
<tr>
<td>VLSI: &gt; 10k gates</td>
<td>1,000,000,000</td>
</tr>
</tbody>
</table>

**Moore’s Law in Action**

- Intel 386: 400 transistors
- Intel 486: 800 transistors
- Intel Pentium: 80 transistors
- IBM Microprocessor: 8,000 transistors
- Intel Microprocessor: 64,000 transistors
- Hitachi Microprocessor: 1 million
- IBM PowerPC: 32 million
- MOS MOS 4100: 64k transistors
- Intel Pentium Pro: 64 million
- Intel Pentium II: 200 million
- Intel Pentium III: 200 million
- Intel Pentium IV: 280 million
- AMD Athlon: 280 million
- Intel Pentium M: 440 million
- Intel Pentium D: 590 million
- Intel Core 2 Duo: 1 billion
- AMD Opteron: 1 billion
- IBM PowerPC: 1.5 billion
- Intel Itanium: 2 billion
- Intel Xeon: 2 billion
- AMD Opteron: 3 billion
- Intel Itanium 2: 5 billion
- Intel Xeon: 5 billion
- AMD Opteron: 10 billion
- Intel Itanium 3: 10 billion
- Intel Xeon: 10 billion
- AMD Opteron: 20 billion
- Intel Itanium 4: 20 billion
- Intel Xeon: 20 billion
- AMD Opteron: 40 billion
- Intel Itanium 5: 40 billion
- Intel Xeon: 40 billion
- AMD Opteron: 80 billion
- Intel Itanium 6: 80 billion
- Intel Xeon: 80 billion
- AMD Opteron: 160 billion
- Intel Itanium 7: 160 billion
- Intel Xeon: 160 billion
- AMD Opteron: 320 billion
- Intel Itanium 8: 320 billion
- Intel Xeon: 320 billion
- AMD Opteron: 640 billion
- Intel Itanium 9: 640 billion
- Intel Xeon: 640 billion
- AMD Opteron: 1 trillion
- Intel Itanium 10: 1 trillion
- Intel Xeon: 1 trillion
- AMD Opteron: 2 trillion
- Intel Itanium 11: 2 trillion
- Intel Xeon: 2 trillion
- AMD Opteron: 4 trillion
- Intel Itanium 12: 4 trillion
- Intel Xeon: 4 trillion
- AMD Opteron: 8 trillion
- Intel Itanium 13: 8 trillion
- Intel Xeon: 8 trillion
- AMD Opteron: 16 trillion
- Intel Itanium 14: 16 trillion
- Intel Xeon: 16 trillion
- AMD Opteron: 32 trillion
- Intel Itanium 15: 32 trillion
- Intel Xeon: 32 trillion
- AMD Opteron: 64 trillion
- Intel Itanium 16: 64 trillion
- Intel Xeon: 64 trillion
- AMD Opteron: 128 trillion
- Intel Itanium 17: 128 trillion
- Intel Xeon: 128 trillion
- AMD Opteron: 256 trillion
- Intel Itanium 18: 256 trillion
- Intel Xeon: 256 trillion
- AMD Opteron: 512 trillion
- Intel Itanium 19: 512 trillion
- Intel Xeon: 512 trillion
- AMD Opteron: 1 trillion
- Intel Itanium 20: 1 trillion
- Intel Xeon: 1 trillion
- AMD Opteron: 2 trillion
- Intel Itanium 21: 2 trillion
- Intel Xeon: 2 trillion
- AMD Opteron: 4 trillion
- Intel Itanium 22: 4 trillion
- Intel Xeon: 4 trillion
- AMD Opteron: 8 trillion
- Intel Itanium 23: 8 trillion
- Intel Xeon: 8 trillion
- AMD Opteron: 16 trillion
- Intel Itanium 24: 16 trillion
- Intel Xeon: 16 trillion
- AMD Opteron: 32 trillion
- Intel Itanium 25: 32 trillion
- Intel Xeon: 32 trillion
- AMD Opteron: 64 trillion
- Intel Itanium 26: 64 trillion
- Intel Xeon: 64 trillion
- AMD Opteron: 128 trillion
- Intel Itanium 27: 128 trillion
- Intel Xeon: 128 trillion
- AMD Opteron: 256 trillion
- Intel Itanium 28: 256 trillion
- Intel Xeon: 256 trillion
- AMD Opteron: 512 trillion
- Intel Itanium 29: 512 trillion
- Intel Xeon: 512 trillion
- AMD Opteron: 1 trillion
- Intel Itanium 30: 1 trillion
- Intel Xeon: 1 trillion
- AMD Opteron: 2 trillion
- Intel Itanium 31: 2 trillion
- Intel Xeon: 2 trillion
- AMD Opteron: 4 trillion
- Intel Itanium 32: 4 trillion
- Intel Xeon: 4 trillion
- AMD Opteron: 8 trillion
- Intel Itanium 33: 8 trillion
- Intel Xeon: 8 trillion
- AMD Opteron: 16 trillion
- Intel Itanium 34: 16 trillion
- Intel Xeon: 16 trillion
- AMD Opteron: 32 trillion
- Intel Itanium 35: 32 trillion
- Intel Xeon: 32 trillion
- AMD Opteron: 64 trillion
- Intel Itanium 36: 64 trillion
- Intel Xeon: 64 trillion
- AMD Opteron: 128 trillion
- Intel Itanium 37: 128 trillion
- Intel Xeon: 128 trillion
- AMD Opteron: 256 trillion
- Intel Itanium 38: 256 trillion
- Intel Xeon: 256 trillion
- AMD Opteron: 512 trillion
- Intel Itanium 39: 512 trillion
- Intel Xeon: 512 trillion
- AMD Opteron: 1 trillion
Minimum VLSI Feature Size
1995 Projections Vs. Reality

<table>
<thead>
<tr>
<th>Year</th>
<th>DRAM Projection</th>
<th>DRAM What Happened</th>
<th>μProcessor Gate Length</th>
</tr>
</thead>
<tbody>
<tr>
<td>1998</td>
<td>0.25 μm</td>
<td>0.25 μm</td>
<td>0.25 μm</td>
</tr>
<tr>
<td>2001</td>
<td>0.18 μm</td>
<td>0.13 μm</td>
<td>0.065 μm</td>
</tr>
<tr>
<td>2003</td>
<td>0.13 μm</td>
<td>0.09 μm</td>
<td>0.032 μm</td>
</tr>
<tr>
<td>2004</td>
<td>0.10 μm</td>
<td>0.08 μm</td>
<td>0.018 μm</td>
</tr>
<tr>
<td>2005</td>
<td>0.07 μm</td>
<td>0.045 μm</td>
<td>0.009 μm</td>
</tr>
<tr>
<td>2007</td>
<td>0.04 μm</td>
<td>0.022 μm</td>
<td></td>
</tr>
<tr>
<td>2010</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2016</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

2005 International Technology Roadmap for Semiconductors

- Two key conclusions:
  - More aggressive chip scaling than projected earlier
  - Beginning to reach fundamental limits of materials used for the planar Silicon CMOS process
    - Basis of industry for past 30 years
- Industry plans:
  - Accelerate rate of technical progress
  - Will reach fundamental limits of process sooner than expected – between 2006 and 2008

Key Technical Challenges

- Making the mask to transfer layout onto chip
  - Optical lithography will not carry us beyond 2010
    - Alternatives:
      - Extreme ultraviolet lithography
      - Electron projection lithography
- Development of new metrology tools
  - Perform critical measurements of new materials, processes, and devices
- Difficulty to deposit metal into deep and narrow holes etched onto chip to make billions of interconnections
  - Need new interconnection strategy within the chip
    - Optical interconnect
    - Wireless interconnect
**Acceleration of Moore’s Law Continues**

<table>
<thead>
<tr>
<th>Year</th>
<th>DRAM Memory Size</th>
<th>DRAM Cost/Bit</th>
<th>μProcessor Speed</th>
</tr>
</thead>
<tbody>
<tr>
<td>2001</td>
<td>512 M</td>
<td>7.7 μcents</td>
<td>1,684 MHz</td>
</tr>
<tr>
<td>2005</td>
<td>2 G</td>
<td>1.9 μcents</td>
<td>5,173 MHz</td>
</tr>
<tr>
<td>2010</td>
<td>8 G</td>
<td>0.34 μcents</td>
<td>11,511 MHz</td>
</tr>
<tr>
<td>2016</td>
<td>64 G</td>
<td>0.042 μcents</td>
<td>28,751 MHz</td>
</tr>
</tbody>
</table>

**Annual Sales**

- 10¹⁸ transistors manufactured in 2003
  - 100 million for every human on the planet

**Economic Conclusions**

- By 2010:
  - Memory costs 1/20 what it costs today
  - Microprocessors are 10 times faster
- By 2016:
  - Memory cost less than 1/100 today’s prices
  - Microprocessors are 15 times faster
- Industry conclusions:
  - Need increased support for University research
  - Got 8% increase in NSF appropriations
- Industry funding agencies:
  - National Nanotechnology Initiative
  - Networking and Information Technology Research Initiative
  - Defense Dept’s. Government Industry Cooperative University Research Program
**Surprise – Scaling Faster than Ever!**

- History of 30% per-year per-function cost reduction
- 0.7 feature scaling from generation to next
- 1995 – expected Moore’s law to end in 2010 with 0.1 \( \mu m \) feature size – looks like it will continue until we hit 0.01 \( \mu m \)!
- Chip cost kept increasing, but customer cost/benefit per function kept dropping
- Multi-chip modules (MCMs) – took over from printed circuit boards (PCBs) in many applications
- Systems-on-a-chip (SoCs) – single chip entire system with sensor, wireless receiver/transmitter, processor, digital signal processor (DSP), and memory
  - Starting to take over from MCM’s

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**Clock Speed**

- Many other factors grow exponentially
  - Ex: clock frequency, processor performance

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**Consequences of Extremely Rapid Shrinking of VLSI**

- Complete change of all computer-aided design (CAD) tools
  - Need new deep sub-micron transistor models – Spice Level 3 MOSFET model no longer correct
- Design & Test of VLSI – Severe Challenge
- Low-Power VLSI Design – even more severe challenge
- Hardly any improvement in battery technology over time
  - Billion transistor chips around the corner
- New era of wireless sensors-on-Silicon has arrived
  - Solid-State & VLSI joint project
**Technical Problems of VLSI**

- **Low-Power Design**
  - Silicon CMOS transistors now leak current heavily, even when not switching
  - May force change in a few years from Si CMOS to Silicon-on-Insulator technology
- In two years, the testing cost will exceed the chip making cost and the chip packaging cost
  - In spite of cost of fabrication line rising to $2 billion
  - New digital CMOS faults (i.e., capacitive interconnect coupling)
  - New interest in built-in self-testing (make the design test itself)
- Inductance – now a major problem for chip leads and pins

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**Low-Power Design and Batteries**

- At present, NiCd batteries provide 120 Watt Hrs / Kg
  - Improvements come extremely slowly

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**Power Dissipation**

- [Graph showing power dissipation over years for high-performance processors and hand-held electronics]
Design for Low Power

- Most critical and difficult part of VLSI design at present
- On large projects, each designer gets a power budget
- To meet it:
  - Use only complementary static CMOS logic gates or pass transistor logic
  - Dynamic gates MAY be an option for 0.1 μm processes
  - Reduce dynamic power consumption by reducing supply voltage, switched capacitance, & clock frequency
  - Use minimum-sized devices & manual layout
- Low-power – 1.5 to 3 V supplies
- Use a variable clock rate to reduce power

Low-Power Design

- Off-power of chips increases 10 times each time we shrink to a new feature size (some say 20 times)
  - Power dissipation for high-performance processors will exceed package limits by 25 times in 15 years
- MOSFET Transistor Leakage
  - Need to control gate leakage
  - Need to control sub-threshold leakage
  - Switch to very thin high-κ oxynitride dielectric for gate oxide around 2005
  - Switch to metal transistor gate from polysilicon gate

Transistor Leakages

- $I_1$: Reverse-Bias Current
- $I_2$: Weak Inversion
- $I_3$: Drain-Induced Barrier-Lowering
- $I_4$: Gate-Induced Drain Leakage
- $I_5$: Punchthrough
- $I_6$: Narrow-Width Effect
- $I_7$: Gate Oxide Tunneling
- $I_8$: Hot-Carrier Injection
Low-Power Design

- Interim solutions:
  - Use multiple transistor thresholds ($V_{th}$) on one chip
  - Use multiple oxide thicknesses ($t_{ox}$) on one chip
  - Use multiple power supplies ($V_{DD}$) on one chip
    - Very slow $V_{DD}$ scaling – hard technical problem
- ULSI Power Management
  - Switch to lower clock $f$ when less computing needed
  - Selectively power down unused parts of chip
  - Redesign DSP and μprocessor data path to use less energy
- Power supply & signal noise sensitivity increasing
  - Operating voltage decreases 20% for each feature size shrink

Silicon-On-Insulator MOSFETs

- Need to be integrated onto the same chip as traditional CMOS devices – could save much power

Fig. 2 Dynamic power, which accounts for most of the power dissipated in CMOS ICs, has two Major components: crowbar current and load current. Crowbar power is dissipated when the transistor's inputs are changing from low to high or high to low because the p-channel and the n-channel devices are both on in their linear region at the same instant, creating a low-resistance path to ground.
Fig. 4 Clock gating is highly effective at reducing dynamic power, because it prevents the unnecessary clocking of storage elements. In conventional schemes [top left], the register is clocked all the time, whether or not new data awaits. If the register must hold the old data, its output is fed back into the data input through a multiplexer whose enable line controls whether the register clocks in new data or recycles existing data.

With a gated clock [bottom left], the signal that had controlled the enable line now controls the gate. The lower the average local clock frequency, the less power is spent on driving the register’s clock input. Thus, the two circuits function identically, but use of the gated clock saves power.

Clocks can be gated locally [bottom left] or else at a more global level [right] for even greater power reductions.

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When voltages are lowered, the performance of an IC can be maintained if the slower transistor switching is offset by parallelism and pipelining. Granted, this remedy increases IC area. The simple datapath [top left] performs an addition and a comparison. Pipelining [top right] and parallelism [bottom left] compensate for the loss in throughput due to voltage reduction. The use of parallelism and pipelining to maintain performance at lower voltages was developed by Anantha Chandrakasan and Robert Brodersen at the University of California.

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### 1. Effects of architecture-based voltage scaling

<table>
<thead>
<tr>
<th>Architecture</th>
<th>Voltage, V</th>
<th>Area (normalized)</th>
<th>Power (normalized)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Simple</td>
<td>3.0</td>
<td>1.0</td>
<td>1.00</td>
</tr>
<tr>
<td>Parallelized</td>
<td>2.5</td>
<td>1.3</td>
<td>0.35</td>
</tr>
<tr>
<td>Parallel</td>
<td>2.0</td>
<td>3.4</td>
<td>0.26</td>
</tr>
<tr>
<td>Parallelized and parallel</td>
<td>2.0</td>
<td>0.7</td>
<td>0.20</td>
</tr>
</tbody>
</table>
**Advanced Power Reduction Now Needed**

- Power reduction techniques:
  1. Redesign network routing algorithms to reduce power
  2. Redesign compilers and operating systems
  3. Change application software
  4. Change processor architecture
  5. Synthesize data path to reduce power
  6. Change controller state assignment
  7. Resynthesize logic to reduce power
  8. Redesign RF communications front-end to save power
  9. Resize all transistors to balance path delays and take advantage of inertial logic gate delays
  10. Use dual V process (high V for slow paths, low V for fast paths)
  11. Switch to Silicon-on-Insulator technology

**Nanotechnology**

- Nanotechnology has arrived (chip features less than 0.1 μm or 100 nm)
  - No cost-effective way to make such tiny patterns
  - High energy ultra-violet light, narrow spectrum X-rays, electron-beam lithography being explored
  - Used with Micro-Electro-Mechanical Machines (MEMS) devices on chip
    - Mechanical sensors (accelerometers) – automobile air-bag sensor
  - Sensors are now on the Silicon
    - Photonic sensors and interconnects
    - DNA sensors
    - Biochemical sensors
    - Chemical sensors
    - Surface Acoustic Wave filters (Radio Frequency transmission/reception)

**Impact on Designers**

- Reduced supply voltage: 5 V → 3.3 V → 2.5 V
- 2-input NAND gate delay used to be 1-2 ns – is now 160 ps
- Density – transistor count on chip went from 8 million to 50 million (heading towards 1 billion)
- Systems-on-a-Chip are reality
  - Learn Analog VLSI Design
  - Learn to design sensors
  - Learn to design RF receiver transmitters
  - Learn to design DRAM and SRAM on your chip
- Core-based design is now the mainstream
**System-on-a-Chip (SoC)**

- A single chip replaces the whole PCB (Printed Circuit Board)
- Different chips on PCB are now building blocks (cores) of SoC chip
- Advantages:
  - On-chip interconnects are many times faster than off-chip wires
  - Get a compact system with the same functionality
  - Reduces pin overhead
    - Saves much power
    - Reduces noise in the mixed-signal/analog circuits
- Liabilities:
  - Bed-of-nails (decomposition) system testing is not possible
  - Most of the cores are surrounded by many other cores
    - Results in very poor controllability and observability
    - Need electronic test hardware to access these blocks during testing

**Example System-on-a-Chip**

**System-in-a-Package (SIP)**

- SoC technology – a great success, EXCEPT for radio receiver/transmitters
  - Can sustain mixed analog/digital hardware together on one chip, provided that:
    - Analog hardware is in the voice band
    - Digital clocks & their harmonics are carefully chosen to avoid polluting key parts of the spectrum with noise
  - Key result: Still unable to integrate radio frequency (RF) hardware into SoC
    - Substrate coupling between digital and analog parts causes digital clock noise to deplete the signal-to-noise ratio of RF part
    - RF tuners still require precision inductors, but on-chip inductors are expensive and inadequate
- Interim solution: Combine separate digital & analog chips and passive components into a single package
**Today’s Trend**

- Moore’s Law continues to hold
- Major technical obstacles to continuing Moore’s Law at present are:
  - Lithography
  - Low-Power Design
  - VLSI Cost-Effective Testing
  - Design complexity of 1 billion transistor single chip
- VLSI Designers are increasingly asked to do analog chip layout and sensors on silicon

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**Top-Down Design Process**

- System Level Specification
- System Partition & Design Creation
- Functional Verification
- Logic Synthesis
- Logic Simulation & Optimization
- Timing Analysis
- Layout Design and Verification
- Circuit Simulation
- Mask Making & Wafer Fabrication
- Test Synthesis & Test Generation
- Design Rule

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**Abstraction Hierarchy**

Abstraction Hierarchy – a set of interrelated representation levels that allow a system to be represented in varying amounts of detail. Helps designer maintain perspective.