The VLSI Transistor

- MOSFET History and Properties
- C-Switch and MOS Inverter
- MOS NAND and NOR Gates
- MOS Compound Logic
- MOS MUX and D Flip-Flop
- MOS Physical Realizations
- Behavioral, Structural & Physical domains
- Summary

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Material from: Principles of CMOS VLSI Design
By Neil E. Weste and Kamran Eshraghian
&
CMOS VLSI Design By Weste and Harris

Transistor and Integrated Circuit History

- MOSFET idea:
  - J. Lillenfeld 1925
  - O. Heil 1935
- Experiments in early Field-Effect Transistor (FET) failed due to material problems
  - Led to invention of Bipolar transistor at Bell Telephone Laboratories in 1947 by Shockley, Brittain, and Bardeen
  - 1956 Nobel Prize in Physics
CMOS MOSFET Inventions

- Key Patents:
  - Frank Wanlass – Fairchild 1963 – CMOS Logic Gates
- Two types of MOS transistors

Silicon Lattice

- Transistors are built on a silicon substrate
- Silicon is a Group IV material
- Forms crystal lattice with bonds to four neighbors

Dopants

- Silicon is a semiconductor
- Pure silicon has no free carriers and conducts poorly
- Adding dopants increases the conductivity
- Group V: extra electron (n-type)
- Group III: missing electron, called hole (p-type)
**p-n Junctions**

- A junction between p-type and n-type semiconductor forms a diode.
- Current flows only in one direction.

```
    p-type   n-type
    anode    cathode
```

**nMOS Transistor**

- Four terminals: gate, source, drain, body
- Gate – oxide – body stack looks like a capacitor
  - Gate and body are conductors
  - SiO₂ (oxide) is a very good insulator
  - Called metal – oxide – semiconductor (MOS) capacitor
  - Even though gate is no longer made of metal

```
Gate
Source
Drain
bulk Si
SiO₂
Polysilicon
```

**nMOS Operation**

- Body is commonly tied to ground (0 V)
- When the gate is at a low voltage:
  - P-type body is at low voltage
  - Source-body and drain-body diodes are OFF
  - No current flows, transistor is OFF
**nMOS Operation Cont.**

- When the gate is at a high voltage:
  - Positive charge on gate of MOS capacitor
  - Negative charge attracted to body
  - Inverts a channel under gate to n-type
  - Now current can flow through n-type silicon from source through channel to drain, transistor is ON

**pMOS Transistor**

- Similar, but doping and voltages reversed
  - Body tied to high voltage (V_{DD})
  - Gate low: transistor ON
  - Gate high: transistor OFF
  - Bubble indicates inverted behavior

**Power Supply Voltage**

- GND = 0 V
- In 1980's, V_{DD} = 5V
- V_{DD} has decreased in modern processes
  - High V_{DD} would damage modern tiny transistors
  - Lower V_{DD} saves power
- V_{DD} = 3.3, 2.5, 1.8, 1.5, 1.2, 1.0, ...
**MOSFET Properties**

- Arrow conventions – $p \rightarrow n$
- $p$ type slower (lower hole mobility)
- Assignment of SOURCE & DRAIN names depends on current flow
- Power signals:
  - '1' – 1.5 to 15 V, ($V_{DD}$)
  - '0' – 0 V, ($V_{SS}$ or GROUND)
- Signal strength – how much current can it sink or source
  - Important for switch-level simulators

**Transistors as Switches**

- We can view MOS transistors as electrically controlled switches
- Voltage at gate controls path from source to drain

**CMOS Inverter**

<table>
<thead>
<tr>
<th>A</th>
<th>Y</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
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</tbody>
</table>

A diagram of CMOS inverter is shown.
CMOS NAND Gate

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>Y</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
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</tbody>
</table>

A = 0, B = 0, Y = 1 (OFF)
A = 0, B = 1, Y = 0 (OFF)
A = 1, B = 0, Y = 0 (ON)
A = 1, B = 1, Y = 1 (ON)
**CMOS NAND Gate**

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>Y</th>
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<tbody>
<tr>
<td>0</td>
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</table>

- **A = 1**
  - **B = 0**
    - **Y = 1** (ON)
    - **Y = 0** (OFF)

- **A = 1**
  - **B = 1**
    - **Y = 0** (ON)
    - **Y = 1** (ON)

**CMOS NOR Gate**

- **A = 1**
  - **B = 0**
    - **Y = 1** (OFF)
    - **Y = 0** (OFF)

- **A = 1**
  - **B = 1**
    - **Y = 0** (ON)
    - **Y = 1** (ON)
NOR Gate Karnaugh Map

<table>
<thead>
<tr>
<th>OUTPUT</th>
<th>A INPUT</th>
<th>B INPUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
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<td>1</td>
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</table>

<table>
<thead>
<tr>
<th>TABLE 1.8 2-input CMOS NOR Gate Truth Table</th>
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</thead>
<tbody>
<tr>
<td>OUTPUT</td>
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<tr>
<td>--------</td>
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<td>0</td>
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CMOS NOR Gate

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<th>A</th>
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<th>Y</th>
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<tbody>
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<td>1</td>
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</table>

3-input NAND Gate
- Y pulls low if ALL inputs are 1
- Y pulls high if ANY input is 0
### 3-input NAND Gate

- Y pulls low if ALL inputs are 1
- Y pulls high if ANY input is 0

![3-input NAND Gate Diagram](image)

### CMOS Fabrication

- CMOS transistors are fabricated on silicon wafer
- Lithography process similar to printing press
- On each step, different materials are deposited or etched
- Easiest to understand by viewing both top and cross-section of wafer in a simplified manufacturing process

### Inverter Cross-section

- Typically use p-type substrate for nMOS transistors
- Requires n-well for body of pMOS transistors

![Inverter Cross-section Diagram](image)
**Well and Substrate Taps**

- Substrate must be tied to GND and n-well to \( V_{DD} \)
- Metal to lightly-doped semiconductor forms poor connection called Shottky Diode
- Use heavily doped well and substrate contacts / taps

![Diagram of Well and Substrate Taps]

**Inverter Mask Set**

- Transistors and wires are defined by masks
- Cross-section taken along dashed line

![Diagram of Inverter Mask Set]

**Detailed Mask Views**

- Six masks
  - n-well
  - Polysilicon
  - n+ diffusion
  - p+ diffusion
  - Contact
  - Metal
Fabrication Steps

- Start with blank wafer
- Build inverter from the bottom up
- First step will be to form the n-well
  - Cover wafer with protective layer of SiO₂ (oxide)
  - Remove layer where n-well should be built
  - Implant or diffuse n dopants into exposed wafer
  - Strip off SiO₂

Oxidation

- Grow SiO₂ on top of Si wafer
  - 900 – 1200°C with H₂O or O₂ in oxidation furnace

Photoresist

- Spin on photoresist
  - Photoresist is a light-sensitive organic polymer
  - Softens where exposed to light
**Lithography**

- Expose photoresist through n-well mask
- Strip off exposed photoresist

![Diagram of lithography process]

**Etch**

- Etch oxide with hydrofluoric acid (HF)
  - *Seeps through skin and eats bone; nasty stuff!!*
  - Only attacks oxide where resist has been exposed

![Diagram of etch process]

**Strip Photoresist**

- Strip off remaining photoresist
  - *Use mixture of acids called piranah etch*
  - Necessary so resist doesn’t melt in next step

![Diagram of strip photoresist process]
**n-well**

- n-well is formed with diffusion or ion implantation
- **Diffusion**
  - Place wafer in furnace with arsenic gas
  - Heat until As atoms diffuse into exposed Si
- **Ion Implantation**
  - Blast wafer with beam of As ions
  - Ions blocked by SiO₂, only enter exposed Si

**Strip Oxide**

- Strip off the remaining oxide using HF
- Back to bare wafer with n-well
- Subsequent steps involve similar series of steps

**Polysilicon**

- Deposit very thin layer of gate oxide
  - < 20 Å (6-7 atomic layers)
- Chemical Vapor Deposition (CVD) of silicon layer
  - Place wafer in furnace with Silane gas (SiH₄)
  - Forms many small crystals called polysilicon
  - Heavily doped to be good conductor
**Polysilicon Patterning**

- Use same lithography process to pattern polysilicon

**Self-Aligned Process**

- Use oxide and masking to expose where n⁺ dopants should be diffused or implanted
- N-diffusion forms nMOS source, drain, and n-well contact

**N-diffusion**

- Pattern oxide and form n⁺ regions
- *Self-aligned process* where gate blocks diffusion
- Polysilicon is better than metal for self-aligned gates because it doesn't melt during later processing
N-diffusion cont.

- Historically dopants were diffused
- Usually ion implantation today
- But regions are still called diffusion

N-diffusion cont.

- Strip off oxide to complete patterning step

P-Diffusion

- Similar set of steps form p+ diffusion regions for pMOS source and drain and substrate contact
**Contacts**

- Now we need to wire together the devices
- Cover chip with thick field oxide
- Etch oxide where contact cuts are needed

**Metalization**

- Sputter on aluminum over whole wafer
- Pattern to remove excess metal, leaving wires

**Layout**

- Chips are specified with set of masks
- Minimum dimensions of masks determine transistor size (and hence speed, cost, and power)
- Feature size \( f = \) distance between source and drain
  - Set by minimum width of polysilicon
- Feature size improves 30% every 3 years or so
- Normalize for feature size when describing design rules
- Express rules in terms of \( \lambda = f/2 \)
  - E.g. \( \lambda = 0.3 \mu m \) in 0.6 \( \mu m \) process
**Simplified Design Rules**

- Conservative rules to get you started

**Inverter Layout**

- Transistor dimensions specified as Width / Length
  - Minimum size is \( \frac{4 \lambda}{2} \), sometimes called 1 unit
  - In \( I = 0.6 \mu m \) process, this is 1.2 \( \mu m \) wide, 0.6 \( \mu m \) long

**nMOS and pMOS Switches**
**C-Switch Device**
- Key enabler of personal computer technology
- More efficient for logic realization than logic gates
- Double-rail logic required
- If only '0' ('1') needs to be passed, delete $p$ ($n$) device

**Series / Parallel Switches**

**Sketch a stick diagram for a 4-input NOR gate**
CMOS Compound Logic Gate
- Unique to CMOS – not available in TLL or ECL

CMOS Compound Gate Truth Table
- Compound logic gate function: 
  \[ F = (A + B + C) \cdot D \]

CMOS Multiplexer
CMOS Level-Sensitive D Latch

Positive Edge-Triggered D Flip-Flop

Physical Transistor Symbols
**Digital Design Domains**
- Behavioral, Structural, and Physical

**Hardware Abstraction Levels**
- Architecture & Behavioral
- Register Transfer – Verilog/VHDL
- Logic
- Switch Level
- Circuit (Transistors)
- Layout & Test Patterns
- Fabrication Line

**Behavioral Adder Example**
- Hardware Description Language supports concurrency, time, word size, bit vectors
- Boolean equations:
  \[
  s = A \cdot B \cdot C + A \cdot B \cdot C + A \cdot C \cdot B + A \cdot B \cdot C \\
  \text{co} = A \cdot B + A \cdot C + B \cdot C \\
  \]
- Verilog description of Carry Out (CO) function:
  ```verilog
  module carry (co, a, b, c);
  output co;
  input a, b, c;
  assign
  co = (a & b) | (a & c) | (b & c);
  endmodule
  ```
**Boolean Behavioral Description**

- Truth table for CO function and Verilog code:

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>C</th>
<th>CO</th>
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```verilog
module carry (co, a, b, c);
  output co;
  input a, b, c;
  wire #10 co = (a & b) | (a & c) | (b & c);
endmodule
```

**Verilog Speed Specification**

```verilog
module adder (s, c4, cl, s, b);
  input [3:0] a, b;
  input cl;
  output [3:0] a;
  output c4;
  wire [2:0] co;
  add a0 (co[0], s[0], a[0], b[0], cl);
  add a1 (co[1], s[1], a[1], b[1], co[0]);
  add a2 (co[2], s[2], a[2], b[2], co[1]);
  add a3 (c[4], s[3], a[3], b[3], co[2]);
endmodule
```

**Structural Adder Description**

- Expressed in Verilog in terms of 1-bit adders:
One-Bit Adder in Verilog

- Structural description presents hardware as connection of known parts:

```verilog
module add (co, a, b, c);
  input a, b, c;
  output co;
  sum a1 (a, b, c);
  carry cl (co, a, b, c);
endmodule
```

```verilog
module carry (co, a, b, c);
  input a, b;
  output co;
  wire g1 (a, b);
  wire g2 (b, c);
  wire g4 (co, y);
endmodule
```

Transistor Structural Description

- For CO module of adder, expressed in Verilog
- Transistors: Type (n or p) Name Drain Source Gate

```verilog
module carry (co, a, b, c);
  input a, b;
  output co;
  wire (1, 12, 13, 14, co);
  nmos g1 (11, a, a);
  nmos g2 (11, b, b);
  nmos g3 (11, co, a);
  nmos g4 (12, a, b);
  nmos g5 (13, a, c);
  pmos g6 (13, b, d);
  pmos g7 (14, c, e);
  pmos g8 (14, b, d);
  nmos g9 (co, vdd, co);
  nmos g10 (co, veg, co);
endmodule
```

Structural Decomposition
Spice Description of Adder Circuit

Physical Representation of Adder

View of Physical Representation
**Design Flow for CMOS Design**

- Specification
- Behavioral Design
- Structural Design
- Physical Design

**Summary**

- CMOS has displaced all of the other logic families
  - Much less power consumption
  - With aggressive transistor scaling, approaches the speed of the fastest traditional Bipolar logic families
  - Massive transistor density compared with Bipolar
  - Suitable for analog circuit implementation
- All nFETs can share the same substrate
- All pFETs can share the same substrate
- May ultimately be displaced if leakage power problem is not solved