# MOS Transistor Theory

- MOSFET Symbols
- Current Characteristics of MOSFET
- Calculation of $V_t$ and Important 2nd-Order Effects
- Small-Signal MOSFET Model
- Summary

Material from: *CMOS VLSI Design* By Weste and Harris

*& Principles of CMOS VLSI Design*

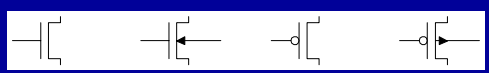
By Neil E. Weste and Kamran Eshraghian

Durga Misra
ECE Dept., NJIT, Newark, NJ



# MOS Symbols and Characteristics

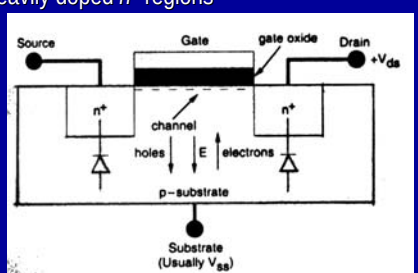
- MOS – majority carrier device
- Carriers: $e^-$ in *n*MOS, holes in *p*MOS
- $V_t$ – channel threshold voltage (cuts off for voltages < $V_t$)
- Transistor gate, source, drain all have capacitance
  - $I = C\,(\Delta V/\Delta t) \Rightarrow \Delta t = (C/I)\,\Delta V$
  - *Capacitance and current determine speed*
- Derive current-voltage (I-V) relationships





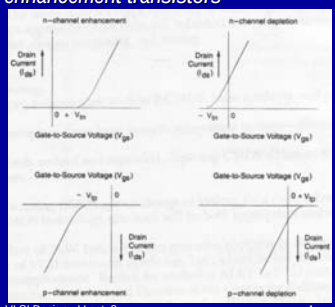
# nMOS Enhancement Transistor

- Moderately doped *p* type Si substrate
- 2 Heavily doped $n^+$ regions



## *I vs. V Plots*

- *Enhancement* and *depletion* transistors
  - *CMOS – uses only enhancement transistors*
  - *nMOS – uses both*





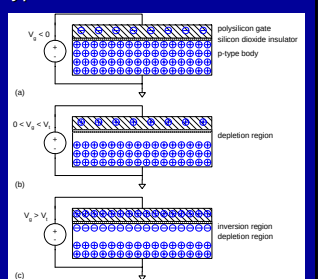

## *Materials and Dopants*

- $SiO_2$ – low loss, high dielectric strength
  - *High gate fields are possible*
- *n* type impurities: P, As, Sb
- *p* type impurities: B, Al, Ga, In

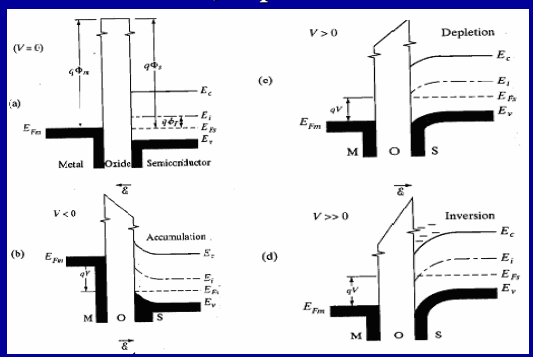


## *Accumulation, Depletion & Inversion*

- Surface of underlying *p* type Si said to be inverted
- Gate and body form MOS capacitor
- Operating modes
  - *Accumulation*
  - *Depletion*
  - *Inversion*



## Accumulation, Depletion & Inversion






## Bipolar vs. MOS Transistors

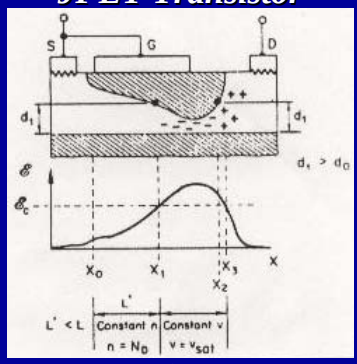
- Bipolar – *p-n* junction – metallurgical
- MOS
  - *Inversion layer / substrate junction field-induced*
  - *Voltage-controlled switch, conducts when* $V_{gs} \geq V_t$
  - $e^-$ *swept along channel when* $V_{ds} > 0$ *by horizontal component of* $\vec{E}$
  - *Pinch-off* – conduction by $e^-$ drift mechanism caused by positive drain voltage
  - Pinched-off channel voltage: $V_{gs} - V_t$ (saturated)
  - Reverse-biased *p-n* junction insulates from the substrate



## JFET vs. FET Transistors

- *Junction FET* (JFET) – channel is deep in semiconductor
- MOSFET – For given $V_{ds}$ & $V_{gs}$, $I_{ds}$ controlled by:
  - *Distance between source & drain* $L$
  - *Channel width* $W$
  - $V_t$
  - *Gate oxide thickness* $t_{ox}$
  - $\varepsilon$ *gate oxide*
  - *Carrier mobility* $\mu$

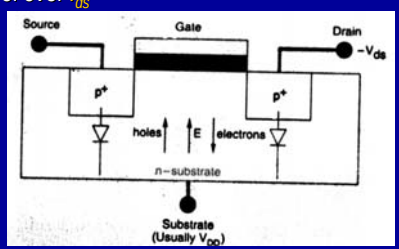
## JFET Transistor





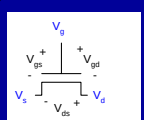

## Punchthrough and pMOSFET

- Avalanche breakdown for very high $V_{ds}$ – gate has no control over $I_{ds}$





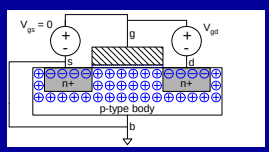

## Terminal Voltages




- Mode of operation depends on $V_g$, $V_d$, $V_s$
  - $V_{gs} = V_g - V_s$
  - $V_{gd} = V_g - V_d$
  - $V_{ds} = V_d - V_s = V_{gs} - V_{gd}$
- Source and drain are symmetric diffusion terminals
  - *By convention, source is terminal at lower voltage*
  - *Hence $V_{ds} \geq 0$*
- nMOS body is grounded. First assume source is 0 too.
- Three regions of operation
  - Cutoff
  - Linear
  - Saturation

# nMOS Cutoff

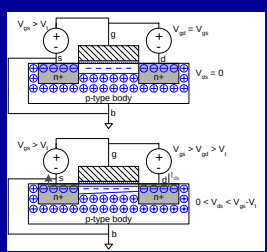
- No channel
- $I_{ds} = 0$
- $V_{gs} < V_t$






# nMOS Linear

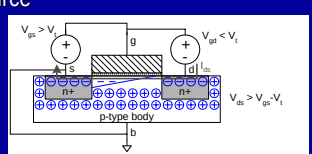
- Channel forms
- Current flows from d to s
  - $e^-$ *from s to d*
- $I_{ds}$ increases with $V_{ds}$
- Similar to linear resistor






# nMOS Saturation

- Channel pinches off
- $I_{ds}$ independent of $V_{ds}$
- We say current saturates
- Similar to current source



## $V_t$ Dependencies

- Gate material
- Gate insulation material
- Gate insulator thickness
- Channel doping
- Impurities at Si – $SiO_2$ interface
- $V_{sb}$ – voltage from source to substrate
- $|V_t| \propto 1/T$
  - *-4 mV /ºC High substrate doping*
  - *-2 mV/ºC Low substrate doping*

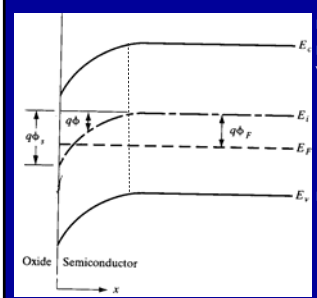


## Non Deep-Submicron Threshold Equations

- $V_t = \underbrace{V_{t\text{-}mos}}_{\text{Ideal } V_t \text{ of Ideal MOS Capacitor}} + \underbrace{V_{fb}}_{\text{Flat-band voltage – point at which energy levels go flat}}$
- $V_{t\text{-}mos} = 2\,\phi_b + \frac{Q_b}{C_{ox}}$
- $\phi_b = \frac{kT}{q} \ln\left(\frac{N_A}{n_i}\right)$, bulk potential difference between Fermi level of doped & intrinsic Si
- $C_{ox}$ = oxide capacitance
- $Q_b$ = bulk charge = $\sqrt{2\,\varepsilon_{Si}\,q\,N_A\,2\,\phi_b}$
- $n_i = 1.45 \times 10^{10}$ cm$^{-3}$ at 300 ºK



## Threshold Equations (cont'd)




- $E_i$ as reference energy level
- Conditions due to different $\phi_s$ values
  - $\phi_s$ =0, Flatband Condition
  - $\phi_s$ <0, Accumulation
  - $\phi_s$ >0, Depletion
  - $\phi_s$ >0 & $\phi_s > \phi_F$ , Inversion
- Condition for strong inversion

## Threshold Equations (cont'd)

- $k$ = Boltzmann's constant = $1.380 \times 10^{-23}$ J/°K
- $q$ = $1.602 \times 10^{-19}$ C ($1\ e^-$ charge)
- $kT/q$ = 0.02586 V. at 300 °K (thermal voltage)
- $\varepsilon_{Si} = 1.06 \times 10^{-12}$ F/cm
- Intrinsic Fermi level – midway between conduction & valence bands
- $p$ Fermi level – closer to valence band
- $n$ Fermi level – closer to conduction band
- $V_{fb} = \phi_{ms} - \frac{Q_{fc}}{C_{ox}}$
- $Q_{fc}$ = fixed charge due to imperfections in Si – $SiO_2$ interface and due to doping



## Threshold Equations (cont'd)

- $\phi_{ms} = \phi_{gate} - \phi_{Si}$ – work function difference between gate material & Si substrate
- $\phi_{ms} = -\left(\frac{E_g}{2} + \phi_b\right) = -0.9$ V ($N_A = 1 \times 10^{16}$ cm$^{-3}$)
- $E_g$ = band gap energy of Si
  $= (1.16 - 0.704 \times 10^{-3} \frac{T^2}{T + 1108})^5$
- $\phi_{ms} \approx$ -0.2 V ($N_A = 1 \times 10^{16}$ cm$^{-3}$)



## Adjustments to $V_t$

- Change $V_t$ by:
  - *Changing substrate doping $N_A$*
  - *Changing $C_{ox}$ (use a different insulator) (usual method)*
  - *Changing surface state charge $Q_{fc}$ (usual method)*
  - *Changing $T$* (temperature)
- Often use a layer of Silicon nitride $Si_3N_4$ $\varepsilon_{Si3N4} = 7.5$ on top of $SiO_2$
  - *Dual dielectric process – gives combined $\varepsilon_{relative} = 6$*
  - *Electrically equivalent to thinner layer of $SiO_2$, leads to higher $C_{ox}$*
- MOS transistors self-isolating if regions between devices cannot be inverted by normal circuit voltages
- High-K

## Example

1. Calculate the native threshold voltage for an n-transistor at 300°K for a process with a Si substrate with $N_A = 1.80 \times 10^{16}$, a $SiO_2$ gate oxide with thickness 200 Å. (Assume $\phi_{ms} = -0.9V$, $Q_{fc} = 0$.)

$$\phi_b = .02586\, ln\left(\frac{1.8\times10^{16}}{1.45\times10^{10}}\right)$$

$$= .36 \text{ volts}$$

with $C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$

$$= \frac{3.9 \times 8.85 \times 10^{-14}}{0.2 \times 10^{-5}}$$

$$= 1.726 \times 10^{-7} \, Farads/cm^2$$

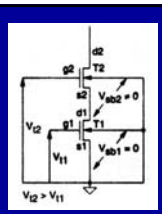
$$V_t = \phi_{ms} + \frac{\sqrt{2\epsilon_{Si} q N_A 2\phi_b}}{C_{ox}} + 2\phi_b$$

$$= -0.9 + .384 + .72$$

$$= 0.16 \text{ volts}$$



## Body Effect




- Series devices – $V_{sb}$ increases as we proceed along series chain
  - *Result: Channel-substrate depletion layer width increases*
  - *Result – Increased density of trapped carriers in depletion layer*
  - *For charge neutrality to hold, channel charge must decrease*
  - *Result: $V_{sb}$ adds to channel-substrate junction potential, gate-channel voltage drop increases, effectively get a higher $V_t$*

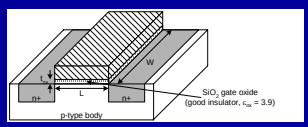


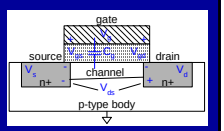
## I-V Characteristics

- In Linear region, $I_{ds}$ depends on
  - *How much charge is in the channel?*
  - *How fast is the charge moving?*

# Channel Charge

- MOS structure looks like parallel plate capacitor while operating in inversion
  - *Gate – oxide – channel*
- $Q_{channel}$ =






# Channel Charge

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- $Q_{channel}$ = CV
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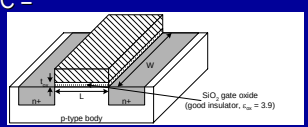


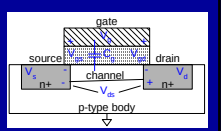




# Channel Charge

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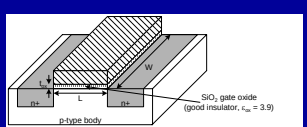
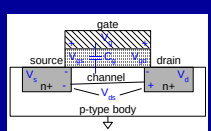
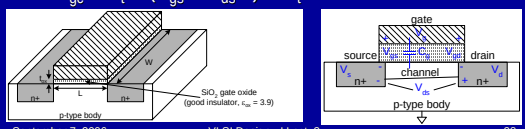
  - *Gate – oxide – channel*
- $Q_{channel}$ = CV
- C = $C_g = \varepsilon_{ox}WL/t_{ox} = C_{ox}WL$ $\quad C_{ox} = \varepsilon_{ox} / t_{ox}$
- V =



## Channel Charge

- MOS structure looks like parallel plate capacitor while operating in inversion
  - *Gate – oxide – channel*
- $Q_{channel} = CV$
- $C = C_g = \varepsilon_{ox}WL/t_{ox} = C_{ox}WL$ Where $C_{ox} = \varepsilon_{ox} / t_{ox}$ F/cm$^2$
- $V = V_{gc} – V_t = (V_{gs} – V_{ds}/2) – V_t$ ➡









## Carrier velocity

- Charge is carried by e-
- Carrier velocity *v* proportional to lateral E-field between source and drain
- *v* =



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- $E = V_{ds}/L$
- Time for carrier to cross channel:
  - t =



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- Time for carrier to cross channel:
  - $t = L / v$



## nMOS Linear I-V

- Now we know
  - *How much charge* $Q_{channel}$ *is in the channel*
  - *How much time* t *each carrier takes to cross*

$I_{ds} =$

## nMOS Linear I-V

- Now we know
  - *How much charge $Q_{channel}$ is in the channel*
  - *How much time* t *each carrier takes to cross*

$$I_{ds} = \frac{Q_{\text{channel}}}{t}$$
$$=$$



## nMOS Linear I-V

- Now we know
  - *How much charge $Q_{channel}$ is in the channel*
  - *How much time* t *each carrier takes to cross*

$$I_{ds} = \frac{Q_{\text{channel}}}{t}$$
$$= \mu C_{\text{ox}} \frac{W}{L}\left(V_{gs} - V_t - V_{ds}/2\right)V_{ds}$$
$$= \beta\left(V_{gs} - V_t - V_{ds}/2\right)V_{ds}$$

$$\beta = \mu C_{\text{ox}} \frac{W}{L}$$



## nMOS Saturation I-V

- If $V_{gd} < V_t$, channel pinches off near drain
  - *When $V_{ds} > V_{dsat} = V_{gs} - V_t$*
- Now drain voltage no longer increases current

$$I_{ds} =$$

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$$I_{ds} = \beta\left(V_{gs} - V_t - V_{dsat}/2\right)V_{dsat}$$



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- Now drain voltage no longer increases current

$$I_{ds} = \beta\left(V_{gs} - V_t - V_{dsat}/2\right)V_{dsat}$$
$$= \frac{\beta}{2}\left(V_{gs} - V_t\right)^2$$



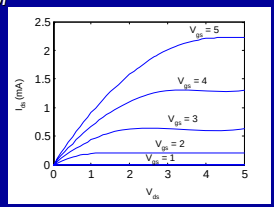
## nMOS I-V Summary

- *Shockley* 1st order transistor models

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t \quad \text{cutoff} \\ \beta\left(V_{gs} - V_t - V_{ds}/2\right)V_{ds} & V_{ds} < V_{dsat} \quad \text{linear} \\ \frac{\beta}{2}\left(V_{gs} - V_t\right)^2 & V_{ds} > V_{dsat} \quad \text{saturation} \end{cases}$$

## Example
## V-I Characteristics for MOSFETs

- We will be using a 0.6 μm process
  - *From AMI Semiconductor*
  - *$t_{ox}$ = 100 Å*
  - *$\mu$ = 350 cm²/V*s*
  - *$V_t$ = 0.7 V*
- Plot $I_{ds}$ vs. $V_{ds}$
  - *$V_{gs}$ = 0, 1, 2, 3, 4, 5*
  - *Use W/L = 4/2 λ*

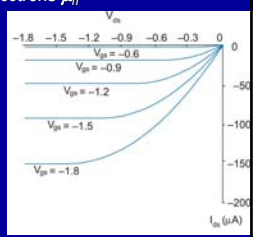



$$\beta = \mu C_{ox}\frac{W}{L} = (350)\left(\frac{3.9 \bullet 8.85 \cdot 10^{-14}}{100 \cdot 10^{-8}}\right)\left(\frac{W}{L}\right) = 120\frac{W}{L}\mu A/V^2$$



## pMOS I-V

- All dopings and voltages are inverted for pMOS
- Mobility $\mu_p$ is determined by holes
  - *Typically 2-3x lower than that of electrons $\mu_n$*
  - *120 cm²/V*s in AMI 0.6 μm process*
- Thus pMOS must be wider to provide same current
  - *In this class, assume $\mu_n / \mu_p = 2$*






## MOS Device Equations

- Ideal Shockley Equations:

1. $I_{ds} = 0$, $V_{gs} - V_t \leq 0$ (cut-off or sub-threshold)
2. $I_{ds} = \beta[(V_{gs} - V_t)V_{ds} - \frac{V_{ds}^2}{2}]$, $0 < V_{ds} < V_{gs} - V_t$ (non-saturation, linear, or triode)
3. $I_{ds} = \frac{\beta}{2}(V_{gs} - V_t)^2$, $0 < V_{gs} - V_t < V_{ds}$ (saturation)

- $\beta$ = MOS transistor gain = $\frac{\mu\varepsilon}{t_{ox}}\left(\frac{W}{L}\right)$ (process; geometry)
- $\mu$ = carrier mobility
- $W$ = Channel Width
- $L$ = Channel length

## MOS Equations (continued)

- $K_p$ = process-dependent gain factor = $\frac{\mu\varepsilon}{t_{ox}} = \mu C_{ox}$

| | $\mu_{nbulk}$ | $\mu_{pbulk}$ | $\mu_{nsurface}$ | |
|---|---|---|---|---|
| Si | 1350 | 450 | 500 | Units of $cm^2$ / (V sec) |
| Ge | 3600 | | | |
| GaAs | 5000 | | | |

- $\varepsilon_{SiO2} = 4\ \varepsilon_0 = 4 \times 8.854 \times 10^{-14}$ F/cm
- $t_{ox} \leq 200$ Å
- For a 1 μm process:
  - *Typical $\beta_n$ = 88.5 W/L μA/V²*
  - *Typical $\beta_p$ = 31.9 W/L μA/V²*



## Spice/Spectre Models for MOSFETs

- LEVEL 1 – Shockley equation + some 2nd-order effects
- LEVEL 2 – Based on device physics
- LEVEL 3 – Semi-empirical – match equations to real circuits based on parameters
- BSIM3 v3 3.1 – Berkeley empirical deep sub-micron model
  - *Use this one – all other models give incorrect results*
    - Predict too high a $V_t$
    - Exaggerate the body effect
    - Incorrectly calculate leakage currents (drain induced barrier lowering)
- $K_P$ – major Spice/Spectre parameter
  - *10 to 100 μA/V², varies 10-20 % in manufacturing process*



## Second-Order Effects – Cannot Be Ignored

## Threshold Voltage Body Effect

- $V_{t0}$ – Threshold voltage when $V_{sb} = 0$
- $V_t = V_{fb} + 2\,\phi_b + \frac{\sqrt{2\,\varepsilon_{Si}\,q\,N_A(2\,\phi_b + |V_{sb}|)}}{C_{ox}}$

$= V_{t0} + \gamma[\sqrt{(2\,\phi_b + |V_{sb}|)} - \sqrt{2\,\phi_b}\,]$

$0.4 \le \gamma \le 1.2$

$\gamma = \frac{t_{ox}}{\varepsilon_{ox}}\sqrt{2\,q\,\varepsilon_{Si}\,N_A} = \frac{1}{C_{ox}}\sqrt{2\,q\,\varepsilon_{Si}\,N_A}$

Equivalent SPICE parameters: GAMMA, VT0

NSUB is $N_A$, PHI is $\phi_s = 2\,\phi_b$ (surface potential at onset of strong inversion)



## Threshold Voltage Body Effect

- $V_{t0}$ – Threshold voltage when $V_{sb} = 0$
- $V_t = V_{fb} + 2\,\phi_b + \frac{\sqrt{2\,\varepsilon_{Si}\,q\,N_A(2\,\phi_b + |V_{sb}|)}}{C_{ox}}$

$= V_{t0} + \gamma[\sqrt{(2\,\phi_b + |V_{sb}|)} - \sqrt{2\,\phi_b}\,]$

$0.4 \le \gamma \le 1.2$

$\gamma = \frac{t_{ox}}{\varepsilon_{ox}}\sqrt{2\,q\,\varepsilon_{Si}\,N_A} = \frac{1}{C_{ox}}\sqrt{2\,q\,\varepsilon_{Si}\,N_A}$

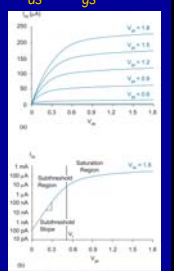
Equivalent SPICE parameters: GAMMA, VT0

NSUB is $N_A$, PHI is $\phi_s = 2\,\phi_b$ (surface potential at onset of strong inversion)



## Subthreshold Region Conduction

- $I_{ds} \approx 0$, but increases exponentially with $V_{ds}$ & $V_{gs}$
- Affects dynamic storage memory cells
- Use BSIM to model



## Channel Length Modulation

- Channel length changes for short channels as $V_{ds}$ changes
- Must now be modeled
- Effective channel length: $L_{eff} = L - L_{short}$
- $L_{short} = \sqrt{\frac{2\ \varepsilon_{Si}}{q\ N_A}\ (V_{ds} - (V_{gs} - V_t))}$

Shorter length increases $W/L$ ratio, increases $\beta$ as $V_d$ increases

Gives a finite output impedance, not a pure current source

More accurate model (which we must use):

$I_{ds} = \frac{K_P\ W}{2\ L}\ (V_{gs} - V_t)^2\ (1 + \lambda\ |\ V_{ds}\ |)$

$\lambda$ = channel length modulation factor (Spice parameter LAMBDA)

Use SPICE LEVEL I to model



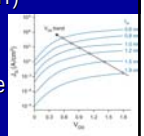
## Mobility Variation

- $\mu$ = $\frac{\text{average carrier drift velocity } (v)}{\text{Electric Field } E}$
- Decreases with increasing doping and with increasing $T$
- $\mu$ is Spice parameter U0
- Use BSIM to model



## Fowler-Nordheim Tunneling

- For very thin gate oxides,
- Current flows from gate to source or gate to drain by $e^-$ tunneling through $SiO_2$
- Exploit in *High Electron Mobility Transistor* (HEMT)
- $I_{FN} = C_1\ W\ L\ E_{ox}^2\ e^{\frac{-E_0}{E_{ox}}}$
- $E_{ox} = \frac{V_{gs}}{t_{ox}}$, Electric field across gate oxide
- $E_0$, $C_1$ are constants
- Limits oxide thickness as processes are scaled – used in making EPROMS



## Drain Punchthrough

- Drain depletion region extends to source at high voltages
  - *Lose gate control of transistor*
  - *Used in pin I/O (pad) circuits to make Zener diodes*
  - *Forces voltages to be scaled down as device sizes are scaled down*



## Impact Ionization – Hot $e^{--}$

- For submicron gate lengths << 1 μm, a major problem
- $e^{--}$ get so much energy that they impact the drain, and dislodge holes, which are swept toward the grounded substrate
- Creates a substrate current
- $e^{--}$ may penetrate the gate oxide and cause gate current
- Degrades $V_t$, subthreshold current, $\beta$
- Causes circuit failure
  - *Poor DRAM refresh times, noise in mixed analog-digital circuits, latchup*
- Hot holes are too slow to cause trouble



## Solutions to Impact Ionization

- Solve with lightly-doped drains
- Drop $V_{DD}$ to 3 V. or lower
- $I_{substrate} = I_{ds}\, C1\, (V_{ds} - V_{dsat})^{C2}$
- $C1 = 2.24 \times 10^{-5} - 0.1 \times 10^{-5}\, V_{ds}$
- $C2 = 6.4$
- $V_{dsat} = \dfrac{V_{tm}\, L_{eff}\, E_{sat}}{V_{tm} + L_{eff}\, E_{sat}}$
- $V_{tm} = V_{gs} - V_{tn} - 0.13\, V_{bs} - 0.25\, V_{gs}$
- $E_{sat} = 1.10 \times 10^{7} + 0.25 \times 10^{7}\, V_{gs}$

## Spice Modeling Parameters

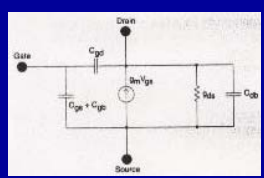
| Parameter | nMOS | pMOS | Units | Description |
|---|---|---|---|---|
| VTO | 0.7 | 0.7 | volt | Threshold voltage |
| KP | $8 \times 10^{-5}$ | $2.5 \times 10^{-5}$ | $A/V^2$ | Transconductance coefficient |
| GAMMA | .4 | .5 | $V^{0.5}$ | Bulk threshold parameter |
| PHI | .37 | .36 | volt | Surface potential at strong inversion |
| LAMBDA | .01 | .01 | $volt^{-1}$ | Channel length modulation parameter |
| LD | $0.1 \times 10^{-6}$ | $0.1 \times 10^{-6}$ | meter | Lateral diffusion |
| TOX | $2 \times 10^{-8}$ | $2 \times 10^{-8}$ | meter | Oxide thickness |
| NSUB | $2 \times 10^{16}$ | $4 \times 10^{16}$ | $1/cm^3$ | Substrate doping density |

- Also must use process parameters in LEVEL III model to calculate VT0, KP, GAMMA, PHI, and LAMBDA
- See Section 2.11 in book.



## Small Signal AC MOSFET Model

- Linear transistor region operation only
- $g_{ds} = \beta [ (V_{gs} - V_t) - 2 V_{ds} ]$
  $= \lim_{V_{ds} \to 0} g_{ds} \approx \beta (V_{gs} - V_t)$
- $R_{channel\ (linear)} = \dfrac{1}{\beta (V_{gs} - V_t)}$
- Model as a resistor






## Saturation Small Signal Model

- In saturation, behaves like a current source
- $\dfrac{d I_{ds}}{d V_{ds}} = \dfrac{d [ \frac{\beta}{2} (V_{gs} - V_t)^2 ]}{d V_{ds}} = 0$
- But channel length modulation gives this a slope
- $g_m = \left. \dfrac{d I_{ds}}{d V_{ds}} \right|_{V_{ds} = \text{constant}}$
- $g_{m\ (linear)} = \beta V_{ds}$
- $g_{m\ (sat)} = \beta (V_{gs} - V_t)$

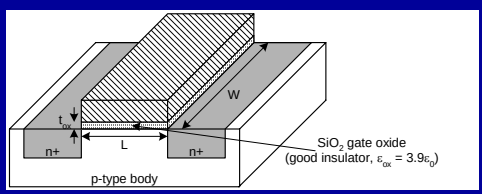
## Capacitance

- Any two conductors separated by an insulator have capacitance
- Gate to channel capacitor is very important
  - *Creates channel charge necessary for operation*
- Source and drain have capacitance to body
  - *Across reverse-biased diodes*
  - *Called diffusion capacitance because it is associated with source/drain diffusion*



## Gate Capacitance

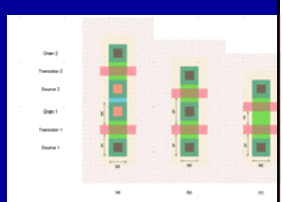
- Approximate channel as connected to source
- $C_{gs} = \varepsilon_{ox}WL/t_{ox} = C_{ox}WL = C_{permicron}W$
- $C_{permicron}$ is typically about 2 fF/μm

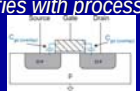





## Diffusion Capacitance

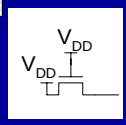
- $C_{sb}$, $C_{db}$
- Undesirable, called *parasitic* capacitance
- Capacitance depends on area and perimeter
  - *Use small diffusion nodes*
  - *Comparable to $C_g$ for contacted diff*
  - *½ $C_g$ for uncontacted*
  - *Varies with process*





## Pass Transistors

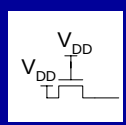
- We have assumed source is grounded
- What if source > 0?
  - *e.g. pass transistor passing $V_{DD}$*





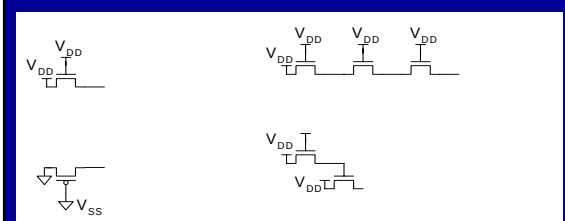

## Pass Transistors

- We have assumed source is grounded
- What if source > 0?
  - *e.g. pass transistor passing $V_{DD}$*
- $V_g = V_{DD}$
  - *If $V_s > V_{DD}-V_t$, $V_{gs} < V_t$*
  - *Hence transistor would turn itself off*
- nMOS pass transistors pull no higher than $V_{DD}-V_{tn}$
  - *Called a degraded "1"*
  - *Approach degraded value slowly (low $I_{ds}$)*
- pMOS pass transistors pull no lower than $V_{tp}$

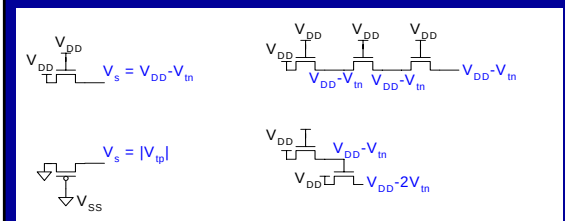





## Pass Transistor Ckts



## Pass Transistor Ckts






## Effective Resistance

- Shockley models have limited value
  - *Not accurate enough for modern transistors*
  - *Too complicated for much hand analysis*
- Simplification: treat transistor as resistor
  - *Replace $I_{ds}(V_{ds}, V_{gs})$ with effective resistance R*
    - $I_{ds} = V_{ds}/R$
  - *R averaged across switching of digital gate*
- Too inaccurate to predict current at any given time
  - *But good enough to predict RC delay*



## Summary

- Current Characteristics of MOSFET
- Calculation of $V_t$ and Important 2nd-Order Effects
- Small-Signal MOSFET Model
- Models in this lecture
  - *For pedagogical purposes only*
  - *Obsolete for deep-submicron technology*
  - *Real transistor parameter differences:*
    - Much higher transistor current leakage
    - Body effect less significant than predicted
    - $V_t$ is lower than predicted
- More accurate models covered later

$V_c = (V_s + V_d)/2 = V_s + V_{ds}/2$

$V_{gc} = V_g - V_c = V_g - V_s - V_{ds}/2 = (V_{gs} - V_{ds}/2)$