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Low-Frequency (1/*f*) Noise Performance of n- and p-MOSFETs with Poly-Si/Hf-Based Gate Dielectrics

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The low-frequency (LF) noise performance of n- and p-channel metal-oxide-semiconductor field-effect transistors (MOSFETs) with different Hf-based gate oxides, deposited by metallorganic chemical vapor deposition (MOCVD) on the same interfacial oxide layer and using polysilicon (poly-Si) as a gate material has been investigated. Independent of the gate oxide, the LF noise spectra of n- and p-MOSFETs are predominantly of the $1/f^{\gamma}$ type, with the frequency exponent γ close to 1. For nMOSFETs, the noise spectral density of HfO_2 devices is two orders of magnitude higher than for SiON or $Hf_xSi_{1-x}ON$ (silicates), where $0 < x < 100\%$, most likely due to trapping by defects in the high-*k* layer. For the silicates with different *x*, no significant differences are noticed for n- and p-MOSFETs. It is shown that the noise characteristics behave as can be expected for a number fluctuations mechanism. The extracted volume and surface trap densities are significantly higher for pure HfO_2 than for the $Hf_xSi_{1-x}ON$ devices. In the latter case, trap densities comparable with the values for the SiON reference transistors are obtained. Hooge's parameter α_H, as an alternative figure of merit, shows that the devices with MOCVD HfO_2 gate dielectric have the noisiest performance, while $Hf_xSi_{1-x}ON$ MOSFETs yield the lowest α_H, even better than for SiON.
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As downscaling of complementary metal oxide semiconductor (CMOS) technologies faces a number of well-known problems, Hf-based high-*k* materials are expected to replace ultrathin SiO_2.[1-4] Based on the present available materials, HfO_2 and $Hf_xSi_{1-x}ON$ ($0 < x < 100$) are the most promising candidates for future CMOS technology (45 nm) nodes. However, the implementation of high-*k* materials is confronted with some serious challenges, most of them related to the inferior material quality, i.e., a high density of traps.[1-4] Because carrier trapping and detrapping within a few nm from the silicon interface governs the fluctuations in the channel current,[5,6] it is likely that the low-frequency (LF) noise is an important issue to be considered for analog applications of devices with high-*k* gates.[7-9]

Alternatively, noise investigations have the potential to be used as a reliability tool, as LF noise is a strongly technology-sensitive parameter.[9,10] In other words, it may also yield information on the defectiveness of the gate stack, when the current fluctuations are caused by trapping-detrapping events. Recently, a comprehensive investigation on the influence of various processing parameters, such as the deposition technique, HfO_2 thickness, and the SiO_2 interfacial layer on 1/*f* noise of n-MOSFETs (metal-oxide-semiconductor field-effect transistors) with polysilicon gate, has been undertaken.[11-14] Devices with a thinner interfacial layer and a thicker HfO_2 layer are found to have higher 1/*f*-like noise, while higher trap values have been noticed for metallorganic chemical vapor deposition (MOCVD) processed devices than for atomic-layer deposition (ALD) counterparts.

In the case of SiO_2 n-MOSFETs, the dominant 1/*f* noise mechanism is shown to be carrier density fluctuations with correlated mobility fluctuations.[15,16] For high-*k* transistors, it has been observed that in most cases the same 1/*f* noise mechanism applies,[7,8,11,17] corresponding, however, to a significantly higher density of oxide traps. In addition, Horikawa et al. have concluded that on top of that, the relaxation-induced noise (RIN) also partly contributes to low-frequency noise.[8] Recently, it was observed for 1.6 nm effective oxide thickness (EOT) $Hf_xSi_{1-x}ON$ n-MOSFETs that the trap density was lower than for HfO_2 but still significantly larger than for SiO_2 MOSFETs.[17] It has also been reported that two decades higher noise is observed for $x = 50\%$ compared with 30%,[18] which was associated with higher trapping in the high-*k* layer.

This paper extends previous noise studies on poly-Si/HfO_2 n-MOSFETs[11] to their p-channel counterparts and to $Hf_xSi_{1-x}ON$ gate dielectrics (also called Hf silicates, in general), on an identical interfacial layer (IL) oxide. Three different silicate ratios, namely 23/77, 47/53, and 65/35, are studied apart from pure HfO_2, and the dielectrics have overall an EOT $\sim$ 1.5 nm. It is seen that the resulting N_t for MOCVD HfO_2, estimated from the input-referred noise spectral density S_{vg}, is relatively high. Moreover, at high gate voltages, the noise characteristics suffer from parasitic series resistance, particularly for HfO_2 devices. The different dielectric compositions perform almost the same and are comparable in noise performance with the reference SiON devices, which indicates that MOCVD $Hf_xSi_{1-x}ON$ is more favorable than pure HfO_2 for analog applications.

Experimental

n- and p-channel MOSFETs of dimensions $W/L = 10/1$ (μm), with SiON (1.5 nm), pure HfO_2, and with various SiO_2/HfO_2 ratios [three different values of *x* of $Hf_xSi_{1-x}ON$, as 23/77, 47/53, and 65/35], were fabricated using a conventional CMOS process flow. A 0.8 nm thin interfacial chemical oxide layer (IMEC clean) was employed on top of which either HfO_2 or $Hf_xSi_{1-x}ON$ with various Hf contents, ranging from 23, 47, to 65%, was deposited by MOCVD. Polysilicon (poly-Si) was used as gate electrode material. The physical thicknesses of the various high-*k* dielectrics for both n- and p-MOSFET devices were chosen such that the final EOT of all devices studied were 1.5 ± 0.2 nm. These devices were post-deposition annealed in NH_3 at 800°C for 60 s, followed by a forming gas anneal at 520°C for 20 min.

On-wafer noise measurements were performed in linear operation at a constant drain voltage $|V_{ds}| = 0.05$ V for gate voltages $|V_{gs}|$ of 0.5–2 V in steps of 50 mV using BTA9812 hardware and NoisePro software from Cadence. A channel length of 1 μm was chosen, to reduce device-to-device scatter in the noise magnitude.

Results

Figure 1a and b shows the LF noise spectra of n- and p-MOSFETs at a $|V_{ds}|$ of 0.05 V and a gate voltage overdrive of $|V_{gs} - V_t|$ of 0.1 V for various high-*k* gate dielectrics with SiON as

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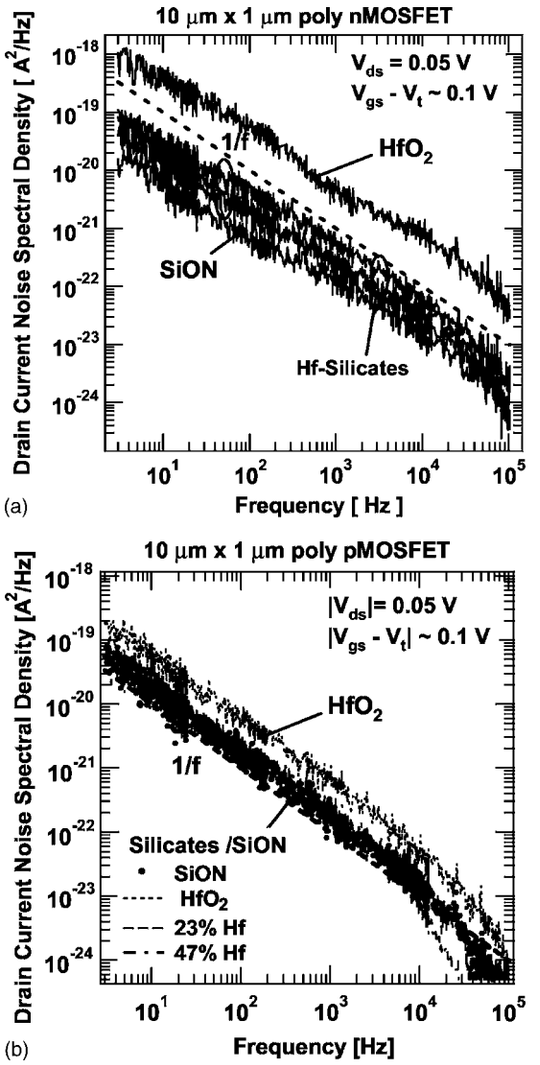

Figure 1. Low-frequency noise spectra at $|V_{ds}| = 0.05$ V and $|V_{gs} - V_t| \sim 0.1$ V for 10 μm × 1 μm n-MOSFETs (a) and p-MOSFETs (b) with various high-*k* oxides. The % of the Hf content was varied from 23 to 100%. SiON is used as a reference oxide for comparison purposes.

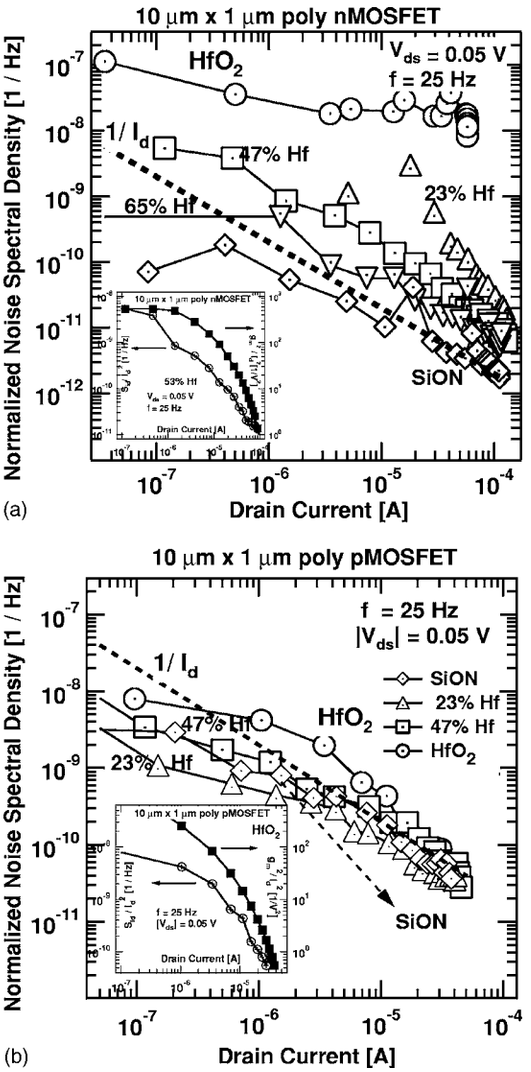

Figure 2. Normalized drain current spectral density S_{id}/I_d^2 vs drain current I_d for 10 × 1 μm n-MOSFETs (a) and p-MOSFETs (b) for various Hf silicates at $|V_{ds}| = 0.05$ V and $f = 25$ Hz. (Inset) Normalized drain current spectral density S_{id}/I_d^2 and g_m^2/I_d^2 vs drain current I_d for 10 × 1 μm n-MOSFETs (a) and p-MOSFETs (b) for 53% Hf dielectric at $|V_{ds}| = 0.05$ V and $f = 25$ Hz.

a reference and various $Hf_xSi_{1-x}ON$ (silicate) ratios. Independent of the used gate oxide, predominantly $1/f^{\gamma}$-like spectra are obtained with a frequency exponent in the range 0.9–1.05. As seen in Fig. 1a, the noise spectral density S_{id} of HfO_2 devices is two orders of magnitude higher than for SiON and $Hf_xSi_{1-x}ON$, in agreement with previous reports.[11,17] This is due to the significant trap density in the HfO_2 dielectric. Moreover, for such transistors S_{id} remains more or less constant at higher drain currents I_d, pointing to a $1/f$ noise dominated by the parasitic series resistance.[19,20] In Fig. 1b, no significant differences in the spectra are noticed among the different Hf/Si ratios, indicating lower bulk defectivity when compared to pure HfO_2.

The corresponding normalized current noise spectral density S_{id}/I_d^2 against the drain current I_d is represented in Fig. 2a and b for n-and p-MOSFETs, respectively. The normalized values are approximately two orders of magnitude higher for the HfO_2 devices (Fig. 2a) when compared with their SiON and $Hf_xSi_{1-x}ON$ counterparts, while the difference is comparatively lower for p-MOSFETs. For the various silicate ratios, similar S_{id}/I_d^2 values are observed for both the n- and p-MOSFETs. As can be noted in Fig. 2a, a leveling off in weak inversion and a roll-off with $1/I_d^k$, where $k \sim 1$, occurs in strong inversion.

It is also observed that S_{id} at $f = 25$ Hz and for all Hf/Si ratios varies according to I_d^x for $1 < x < 2$, whereby x lowers for increasing I_d. An I_d^2 dependence was noticed at low drain currents, suggesting a $1/f$ noise origin related to trapping/detrapping of charges near the interface (number fluctuations).[15,16]

From the variation in the normalized drain current noise spectral density S_{id}/I_d^2 with drain current, represented in Fig. 2a (inset) and b (inset) for n- and p-MOSFETs, it can be deduced that there is a good agreement with the g_m^2/I_d^2 ratio. This again suggests that the $1/f$ noise in the studied transistors can be described in the frame of the correlated number fluctuations theory,[16] based on carrier trapping/detrapping in the gate dielectric.

As represented in Fig. 3a and b, the gate-referred voltage noise spectral density $[\sqrt{S_{vg}} = \sqrt{(S_{id}/g_m^2)}]$ at $f = 25$ Hz shows a pronounced dependence on the gate voltage overdrive $|V_{gs} - V_t|$ for both n- and p-MOSFETs. As can be observed in Fig. 3a, for

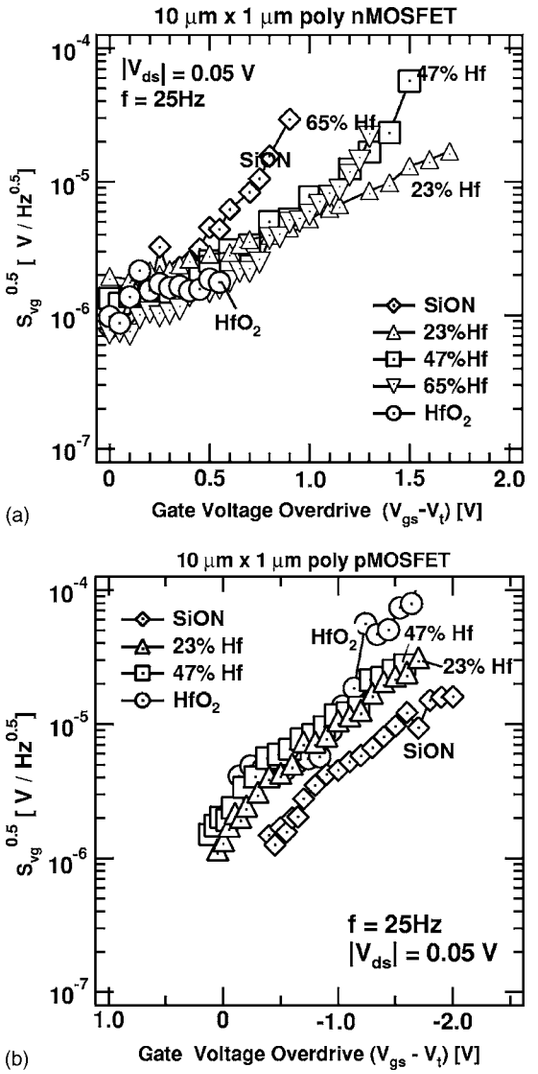

Figure 3. Input-referred voltage noise spectral density $\sqrt{S_{vg}}$ vs gate voltage overdrive $|V_{gs} - V_t|$ at $|V_{ds}| = 0.05$ V, $f = 25$ Hz for 10×1 μm n-MOSFETs (a) and p-MOSFETs (b) for various Hf silicates.

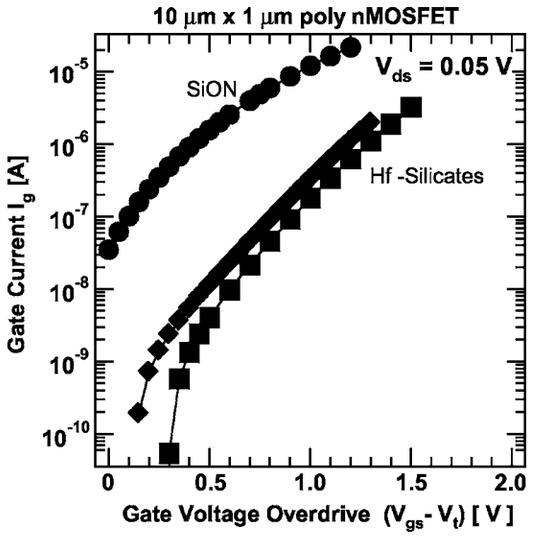

Figure 4. Gate current I_g vs gate voltage overdrive $(V_{gs} - V_t)$ at $|V_{ds}| = 0.05$ V for 10 μm × 1 μm n-MOSFETs for SiON and various Hf silicates.

n-MOSFETs, $\sqrt{S_{vg}}$ shows a tendency to level off to a value corresponding to the flatband voltage noise spectral density S_{vFB} for lower gate voltage overdrives $|V_{gs} - V_t|$. However, for both n- and p-MOSFETs with $Hf_xSi_{1-x}ON$ gate dielectric, $\sqrt{S_{vg}}$ increases with higher gate voltage overdrive $|V_{gs} - V_t|$. Also, the slope of the curves varies with increasing gate voltage overdrive $|V_{gs} - V_t|$ for the various Hf/Si ratios. This $|V_{gs} - V_t|$ dependence may be due to the profiles of the trap concentration with distance from the interface and/or with energy in the gate oxide bandgap.[21] However, in the case of the SiON devices, also the fluctuations in the higher gate current as shown in Fig. 4 can enhance significantly S_{vg}.[22,23]

Discussion

In summary, it can be concluded that the LF noise of polygate n- and p-MOSFETs with $Hf_xSi_{1-x}ON$ gate dielectric is rather independent of the composition x, in the range studied here. Moreover, the spectra have a $1/f$-like character, while the noise characteristics behave in agreement with a trapping origin. However, one would normally expect that the noise increases for increasing x, following the increased trap density.[18] The fact that no clear dependence on x is observed here could point either to the fact that the relevant traps in our silicate stacks do not depend on x or that the dominant fluctuation mechanism is not related to trapping. To put this even more in perspective, assuming a pure tunneling model for the trapping, the tunneling depth z can be calculated from

$$\frac{1}{2\pi f} = \tau_0 \exp(\alpha_t z) \qquad [1]$$

with τ_0 the tunneling time constant at the Si-SiO_2 interface and α_t the tunneling parameter, given by[15]

$$\alpha_t = \sqrt{[(2m^*_{e(h)}\phi_b)/\hbar^2]} \qquad [2]$$

where $\hbar$ is Planck's constant divided by 2π. The tunneling parameter α_t is estimated semi-empirically from the expected values of the effective tunneling mass of the electron (m^*_e) in the dielectric[21] and hole (m^*_h) in the Si[24] and the potential barriers for electron and hole emission at the silicon-oxide interface (ϕ_b), which varies with composition x. The effective masses in HfO_2 are estimated to be $0.18m_0$ for an electron and $0.15m_0$ for a hole and the barrier height for holes is assumed to vary linearly from 4.4 to 3.4 eV from the SiO_2 to HfO_2 system, while it varies from 3.5 to 1.5 eV for electrons.

The calculation result is shown in Fig. 5 for electrons, versus x and corresponding with a frequency of 25 Hz. As indicated, the tunneling parameter reduces to half of its value when HfO_2 replaces pure SiO_2, mainly due to the effect of a reduced electron mass, as indicated in the second x axis. This means that electrons could tunnel through the physical gate oxide thickness, contributing to the gate leakage current rather than to the noise. This is not the case for the noise at higher frequencies, corresponding to a shallower tunneling depth.

In order to verify whether the noise at low frequencies (large tunneling depths) is due to trapping or to some other mechanism, $f \times S_{id}$ has been investigated as a function of frequency. The result is shown in Fig. 6a for various gate voltage overdrive $(V_{gs}\text{-}V_t)$ voltages for a 65% silicate n-MOSFET, while Fig. 6b shows the $f \times S_{id}$ spectra for all the silicate ratios studied at $|V_{gs} - V_t| \sim 0.1$ V for p-MOSFETs. In both cases, a rather continuous dependence on the frequency is observed, which is constant for the p-MOSFETs and increasing with frequency (or reducing with depth from the interface) for the n-channel counterparts. Based on this and

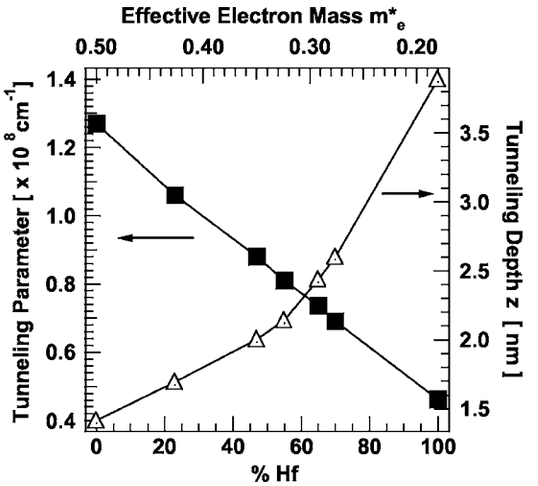

Figure 5. Estimation of tunneling parameter (left *y* axis) for Hf-based gate oxides (bottom *x* axis) based on the empirical data (Ref. 14) of effective tunneling mass of the electron (top *x* axis) and the barrier height at the SiO_2-$Hf_xSi_{1-x}ON$ interface. The calculated tunneling depth is plotted along right *y* axis.

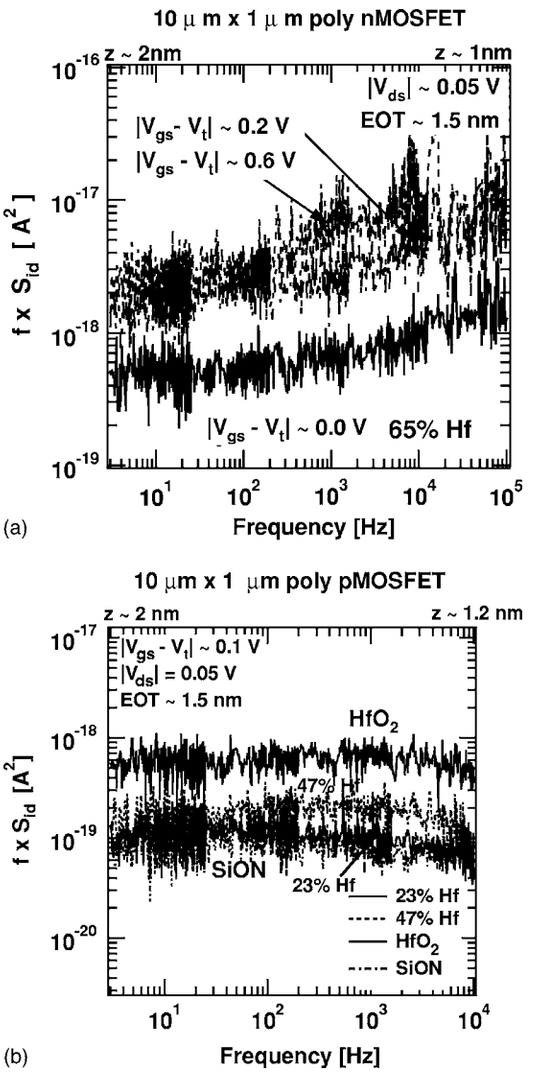

Figure 6. $f \times S_{id}$ spectra vs frequency f at $|V_{ds}| = 0.05$ V, $|V_{gs}\text{-}V_t| \sim 0.1$ V for 10×1 μm n-MOSFETs (a) and p-MOSFETs (b) for various Hf-silicate dielectric.

on the behavior of the noise characteristics in Fig. 2 and 3, we believe that the noise at $f = 25$ Hz can in the first instance be interpreted in terms of trapping.

In the case of p-MOSFETs with metal gates, more scattering-related events occur in which case it supports the mobility fluctuations.[25] Von Haartman et al.[26] observed a similar behavior and concluded that the noise origin was due to mobility fluctuations in p-MOSFETs for a SiGe-based system. But in the case of poly-gates with p-MOSFETs, more trapping-related events are found to be the origin for noise. These differences may be closely related to the concentration of oxygen vacancy-related defects, which we have explained in our forthcoming paper.[27] A similar conclusion was reached by another group,[17] although the question is not self-evident as explained before.

Having established the trapping origin of the $1/f$ noise, an effective volume trap density N_t can be estimated from the values of S_{vg}, using the formula,[15,16]

$$S_{vfb} = q^2 kTN_t/(WLC_{inv}^2 \alpha_t f) \quad [3]$$

where kT is the thermal energy, q is the electron charge, and C_{inv} is the inversion capacitance per unit area. From Fig. 7a, which shows the volume and surface trap densities along the first *y* and second *y* axis, it follows that for n-MOSFETs, $Hf_xSi_{1-x}ON$ performs better than pure HfO_2 (for $V_{gs} \sim V_t$). Min et al. for $Hf_xSi_{1-x}ON$ have obtained similar values at low gate voltage overdrives.[17] The increase of N_t with V_{gs} could point to a trap profile that increases with increasing energy, although this has to be confirmed by more detailed modeling, including correlated mobility fluctuations. The surface trap densities, calculated from N_t, are estimated using the formula $4kTzN_t$, where z is the tunneling distance of the carrier from the Si/high-κ interface at $f = 1$ Hz. The trap densities range from the highest for HfO_2 ($\sim 3 \times 10^{13}$ cm^{-2}) to $\sim 5 \times 10^{11}$ cm^{-2} for the $Hf_xSi_{1-x}ON$, irrespective of the composition, while for SiON reference devices we find a density $\sim 8 \times 10^{11}$ cm^{-2}. Pure HfO_2 has two orders of magnitude higher density, indicating that the oxide layer is highly defective.

From Fig. 7b, which shows the volume and surface trap densities along first *y* and second *y* axis for p-MOSFETs, the trap values are more or less comparable among various silicate ratios including HfO_2 and SiON oxides. The volume trap densities are found to be $\sim (3 - 6) \times 10^{18}$ cm^{-3} eV^{-1} while the surface trap values are $\sim (6\text{–}8) \times 10^{11}$ cm^{-2}, where the difference among the silicates can be considered negligible if device-to-device variations are taken into account.

The described trap density values are in agreement with the results obtained from other measurement methods, but should only be considered as effective values, considering the approximate values used for the tunneling parameter, represented in Fig. 5.

Effective values referred to here are due to various approximations during the estimation of tunneling parameter, mainly 1. neglection of the interfacial layer, 2. average trap time constant independent of tunneling depth in both high-k and interfacial layer, 3. linearly extrapolated effective masses on composition x, and 4. quantization and other second-order effects due to high vertical field.

Figure 8 shows the normalized S_{vg} values plotted against %Hf. As seen from the figure, the percentage of hafnium content is seen to be weakly dependent on the normalized noise values. The S_{vg} values for all the % silicates are within the device-to-device variation. One other remark is that the lowest noise is for the SiON reference for both n- and p-MOSFETs. Compared to the ITRS specification value

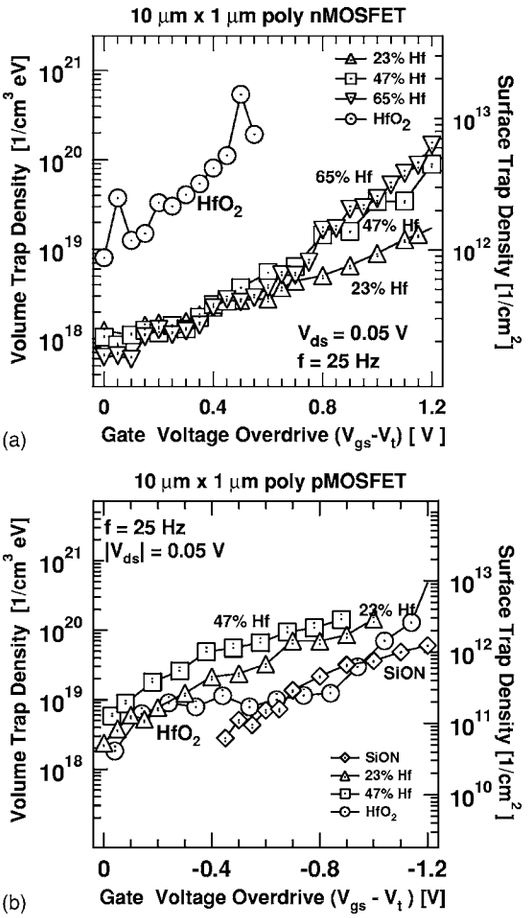

Figure 7. Estimated volume trap density N_t (left y axis) and surface trap density (right y axis) vs gate voltage overdrive $|V_{gs} - V_t|$ at $|V_{ds}| = 0.05$ V for 10×1 μm n-MOSFETs (a) and p-MOSFETs (b) for various Hf-silicate dielectric.

of 200 μV^2/Hz for analog CMOS applications, at least a one-decade higher noise is observed in these high-k devices.[28]

As an alternative figure of merit parameter, Hooge's constant α_H is calculated as NfS_{id}/I_d^2,[29] with N the total number of carriers in the channel, which is calculated from

$$N = WLC_{EOT}(V_{gs} - V_t)/q$$

The resulting α_H is fairly constant or weakly dependent on the gate voltage V_{gs} and is found to be $1 \times 10^{-3} \sim 1 \times 10^{-4}$ for $Hf_xSi_{1-x}ON$ (silicates) and SiON devices and a decade higher for the HfO_2 (Fig. 9). The devices with MOCVD HfO_2 as dielectric material have the noisiest performance, while silicates yield the lowest α_H, even better than the one for SiON. The "noisiness" of the system is also believed to exist in relationship with carrier mobility, affected by different scattering phenomena, which is reflected in the normalized maximum transconductance G_m(max)/CET values as plotted versus %Hf content in Fig. 9.

Conclusions

Summarizing the results, it has been shown that the LF noise spectra of Hf-based dielectrics for both n- and p-MOSFETs are predominantly $1/f^{\gamma}$-like with $\gamma \sim 1$. The flicker noise is approximately two orders of magnitude higher for the HfO_2 devices when compared to their SiON and $Hf_xSi_{1-x}ON$ counterparts. The dependence

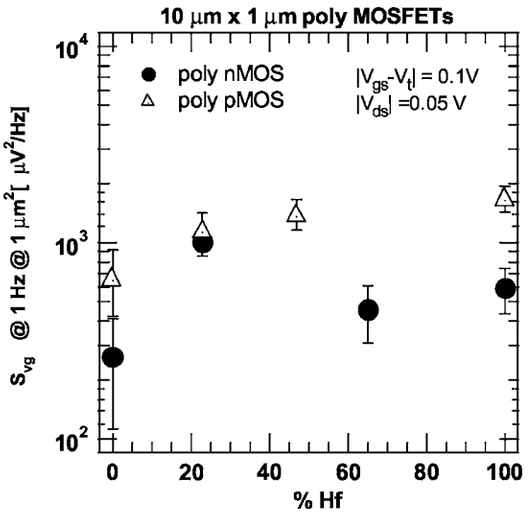

Figure 8. Impact of gate stack composition for n- and p-MOSFETs at $|V_{ds}| = 0.05$ V and $|V_{gs} - V_t| \sim 0.1$ V. The normalized S_{vg} values are used to compare their performance.

of S_{id}/I_d^2 to $1/I_d^x$, for $x \sim 1$, for all Hf/Si ratios of gate oxides, indicates that $1/f$ noise can be described in the frame of the correlated number fluctuations theory for n- and p-MOSFETs. From the values of S_{vg} and N_t, it is derived that the $Hf_xSi_{1-x}ON$ devices perform better than pure HfO_2 and the SiON reference devices for n-MOSFETs, while comparable values are found for all types of p-MOSFETs. S_{vg} values were observed to have a very weak dependence on the %Hf content in both n- and p-MOSFETs and the values were found to be at least an order of magnitude higher when compared to ITRS specifications. The "noisiness" of the system, given by the Hooge parameter as a figure of merit, shows that the devices with an HfO_2 gate dielectric have the noisiest performance, while $Hf_xSi_{1-x}ON$ devices show the lowest α_H, even better than for SiON for n-MOSFETs.

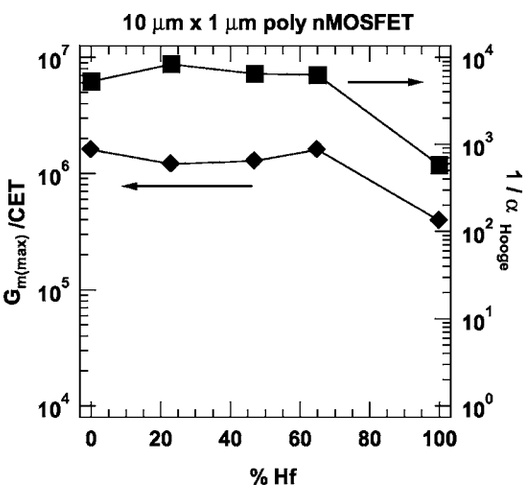

Figure 9. Comparison between $G_{m(max)}$/CET and $1/\alpha_{Hooge}$ at $V_{ds} = 0.05$ V, of n-MOSFETs for various composition of Hf and Si gate dielectric ratios.

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