Effect of Ge Surface Nitridation on the $Ge/HfO_2/Al$ MOS Devices

Reenu Garg, Durga Misra, and Supratik Guha

***Abstract*—In this paper, the effect of Ge surface nitridation on $Ge/HfO_2/Al$ MOS capacitors has been studied. Low-frequency measurements indicated the presence of significant interface states in surface nitrided devices. As temperature decreased from 300 to 140 K, electron trapping increased monotonically in both nitrided and nonnitrided devices, but the interface state density didn't show a major fluctuation in nitrided devices as compared to nonnitrided devices. A constant voltage stress was applied on both samples to test their behavior under stress. Electron trapping was dominant in nonnitrided devices at lower stress voltages. After relaxation, detrapping was observed as devices recovered to their original state. Nitrided devices showed hole trapping after stress, but further device deterioration was observed after relaxation.**

***Index Terms*—Ge bandgap, hysteresis, low temperature, voltage stress.**

I. Introduction

GERMANIUM substrate with high-k gate dielectric films is bringing a new set of challenges in CMOS technologies. The unstable native oxide of Ge was one of the biggest obstruction in a very large-scale integration of CMOS devices in Ge. To obtain a more stable oxide, different gate stacks of Ge oxynitride (GeO_xN_y), using either thermal or plasma anodic nitridation [1], [2] or GeON with low-temperature gate oxide, were used to form Ge MOSFETs [3]. However, these gate stacks are not very scalable. But, high-k dielectrics being deposited directly on Ge [4] seem to be very promising.

Various deposition techniques have been used to deposit HfO_2 films on Ge, such as atomic layer deposition (ALD) [5], CVD [6], thermal evaporation [7], etc. But, devices made by depositing HfO_2 directly on Ge are too leaky or show significant hysteresis. This deterioration in electrical performance is mainly due to the formation of unstable interfacial layer of GeO_2 during the HfO_2 deposition. It has been found that Ge surface treatment prior to gate dielectrics deposition is effective in improving the MOS device quality. Different kinds of surface passivation have been done by forming thin Ge oxynitride [8], [9] by NH_3 annealing [10] or by SiH_4 annealing [11]. Recently, it has been demonstrated that an initial treatment of Ge surface by atomic N beam seems to improve the physical and electrical characteristics of MOS capacitors [12]. However, interface properties of these nitrided Ge MOS devices have not been studied in detail and well understood yet. To examine the effect of surface nitridation on the electrical properties of MOS capacitors, low-temperature characterization has been done. Also, to see the effect of nitridation on the reliability of $Ge/HfO_2/Al$ MOS capacitors, charge-trapping characteristics were investigated using a constant voltage stress at different voltage levels.

Manuscript received July 29, 2005; revised March 25, 2006. This work was supported in part by the National Science Foundation under Award number 0140584.

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Digital Object Identifier 10.1109/TDMR.2006.881457

II. Experimental

Following a standard solvent cleaning and a deionized (DI) water rinse, n-type Ge (100) wafers (0.1 $\Omega \cdot$ cm) were cleaned using a cyclical rinse of H_2O_2, HCl/H_2O, and DI water [13]. Following this, a protective layer of Ge oxide was formed by immersion in a solution of $NH_4OH/H_2O_2/H_2O$. The protective oxide was then removed in an ultrahigh vacuum by thermal adsorption. Following oxide adsorption, the 3.3 nm of HfO_2 films with 0.6 nm of interfacial layer were deposited on the Ge substrate in the system described elsewhere [12]. *In situ* surface-nitridation of the Ge substrates, before HfO_2 deposition, took place at 350 °C−600 °C by exposure to an atomic N beam from a remote RF source at 350 W for 30 s. Samples were then cleaned using standard m-pyrol clean before annealing at 450 °C in a forming gas environment (FGA: N_2/H_2 5%). Al was evaporated by e-beam evaporation. Various sizes of Al gate electrode, ranging from 2×10^{-5} to 2×10^{-3}cm^2, were patterned by photolithography. After depositing aluminum as a backside metal, samples were subjected to a 350 °C forming gas anneal (FGA: N_2/H_2 5%).

Electrical characterization was done using an HP 4145 semiconductor parameter analyzer and an HP 4284A LCR meter. CTI Cryogenics M22 closed loop helium cooled refrigeration system and Palm Beach Cryophysics model 4075 temperature controller were used for low-temperature measurements.

III. Results and Discussion

Fig. 1 shows the capacitance–voltage (C–V) characteristics of nitrided and nonnitrided Ge MOS capacitors at 1 MHz. Significant reduction in hysteresis (0.03 V) of surface nitrided capacitors imply the improvement in device performance after surface nitridation. At high frequency, accumulation capacitance of nitrided devices increased by a factor of three from nonnitrided devices. It implies that surface nitridation enhanced the quality of hafnium oxide deposited as hysteresis was reduced, and/or it helped in restricting the growth of interfacial

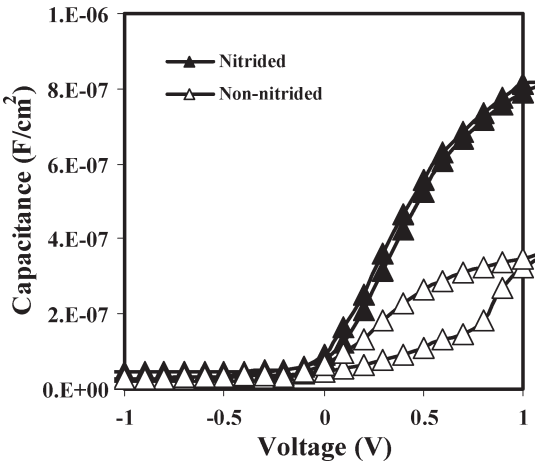


Fig. 1. C–V characteristics of the nitrided and nonnitrided Ge/HfO_2/Al MOS capacitors. The nitrided and nonnitrided devices show hysteresis of 0.03 V and 0.5 V, respectively.

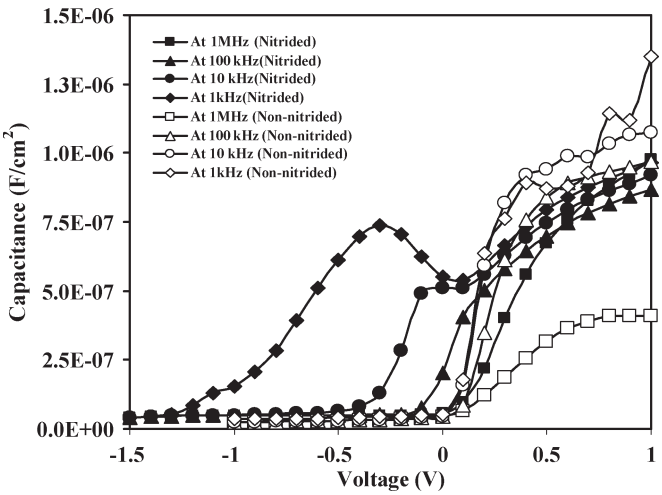


Fig. 2. C–V characteristics of nitrided and nonnitrided Ge/HfO_2/Al MOS capacitors at different frequencies ranging from 1 kHz to 1 MHz.

layer [11]. During high-frequency measurement, therefore, the impact of series resistance makes it difficult to estimate the correct effective oxide thickness (EOT).

To analyze the effect of surface nitridation, C–V characteristics of nitrided versus nonnitrided Ge MOS capacitors were taken at frequencies ranging from 1 MHz to 1 kHz, as shown in Fig. 2. At low frequencies, there is almost no difference in the accumulation capacitance of both devices, which is clearly indicating that surface nitridation didn't affect the interfacial layer but improved the gate oxide. Nitrided samples show a significant dispersion in the inversion region as the frequency is reduced, indicating the presence of slow-interface states. Dimoulas *et al.* [9] had observed a similar dispersion in the inversion region on p-type substrate after Ge surface was treated with O and N beams. No dispersion was observed in the inversion region of nonnitrided devices. It is possible that surface nitridation is creating new slow-interface traps deep in the bandgap that were nonexistent in nonnitrided samples. On the other hand, nonnitrided samples showed dispersion in the accumulation region as a function of frequency that is mainly because of series resistance effect. This behavior is observed

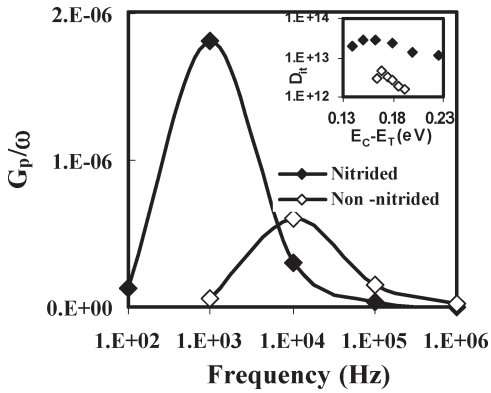


Fig. 3. $G_{\rm p}/\omega$ versus frequency for nitrided and nonnitrided devices. Maximum interface state density $(D_{\rm it})$ is 2.9×10^{13} and 4.55×10^{12} $\rm cm^{-2}eV^{-1}$ for the nitrided and nonnitrided Ge MOS capacitors, respectively. Inset shows the distribution of $D_{\rm it}$ in the bandgap.

when the conductance of gate oxide becomes comparable with the conductance associated with the series resistance of bulk. Absence of this effect in nitrided devices suggests an improvement in the gate dielectric, which was also observed in the hysteresis of these devices (Fig. 1).

To estimate the interface state density $(D_{\rm it})$, $G_{\rm P}/\omega$ was calculated from the measured capacitance and conductance at the gate bias of -1 to 1 V in the frequency range of 1 MHZ to 1 kHz and then plotted as a function of frequency. Energy levels pertaining to gate biases from the depletion to inversion regions (as conductance method is reliable in this region) were calculated from an ideal C–V curve using oxide capacitance from experimental measurements [22]. Maximum $D_{\rm it}$, which is extracted from the peak of $G_{\rm p}/\omega$ versus frequency plot (Fig. 3), is 2.9×10^{13} and 4.55×10^{12} $\rm cm^{-2}eV^{-1}$ in nitrided and nonnitrided devices, respectively. $D_{\rm it}$ in nitrided devices seems to be more widely distributed in Ge bandgap as compared to nonnitrided devices, as shown in the inset of Fig. 3. Also, interface states in nitrided devices are located deeper in the Ge bandgap than in nonnitrided devices. The concentration of the deep interface states in nitrided devices in the bandgap is higher than that of the maximum $D_{\rm it}$ estimated for nonnitrided devices. Thus, the interface states distribution observed using the conductance method in a nitrided case is due to the slow-interface states [23] not present in nonnitrided devices.

Recent studies have shown that HfO_2 has electrically active ionic defects [19] that traps and detraps rapidly, which is based on the Shockley–Read–Hall theory (SRH model) [21]. However, this detrapping process is thermally activated. Hence, detrapping decreases as temperature is lowered; this results in an increase in $\Delta V_{\rm FB}$. Therefore, to further investigate the nature of the traps in gate oxide as well as at interface in nitrided and nonnitrided MOS capacitors, low-temperature conductance and capacitance measurements were taken. Fig. 4 shows the flatband voltage shift $(\Delta V_{\rm FB})$ with respect to room temperature after considering the appropriate flatband temperature correction. A positive increase in $\Delta V_{\rm FB}$ with the reduction in temperature shows electron trapping in both the nitrided and nonnitrided samples. Although almost a linear dependence can be seen in both devices, nitrided devices have a steeper slope in comparison to nonnitrided devices. This suggests that bulk

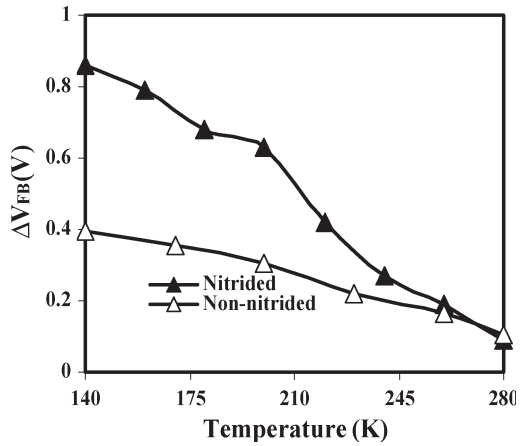


Fig. 4. Shift in the flatband voltage with respect to the room temperature $\Delta V_{\rm FB}$ as a function of the temperature for the nitrided and nonnitrided Ge MOS capacitors.

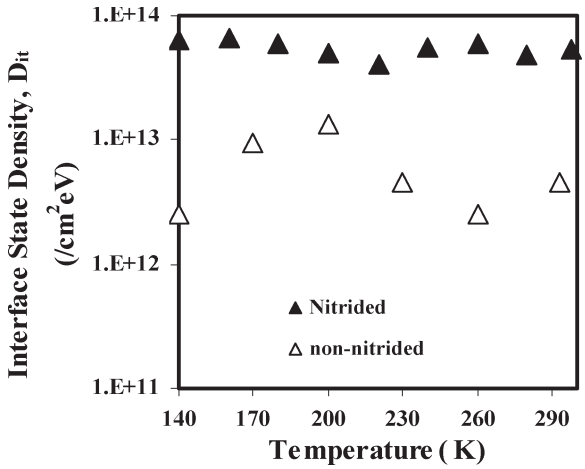


Fig. 5. Interface state density $(D_{\rm it})$ as a function of the temperature for both the nitrided and nonnitrided samples.

trapping in nitrided devices increases rapidly as temperature reduces compared to nonnitrided devices. Nitrogen, therefore, is believed to be contributing to the additional defects in dielectric that are being revealed at low temperature.

In nonnitrided devices, there is a difference of almost one order of magnitude in $D_{\rm it}$ at room temperature and 200 K, as shown in Fig. 5. Since both interface traps and bulk-oxide traps contribute to charge centroid [15], absence of any contribution of interface traps on $\Delta V_{\rm FB}$ implies that bulk-oxide traps are dominant. No considerable variation was observed in interface state density $(D_{\rm it})$ of nitrided devices as a function of temperature. This is in contrast to $\Delta V_{\rm FB}$, where a significant electron trapping was observed as a function of the temperature. It shows that, even though $D_{\rm it}$ is higher in nitrided samples, interface-trap distribution is rather stable with temperature. On the other hand, the interface-trap distribution fluctuates for nonnitrided devices. It is well known that HfO_2 has active intrinsic defects. Diffusion of nitrogen from the interface into the bulk oxide seems to modify the nature of these intrinsic defects in nitrided devices.

As the flatband voltage varies with temperature due to a change in the traps' behavior, trap-activation energies $(E_{\rm T})$

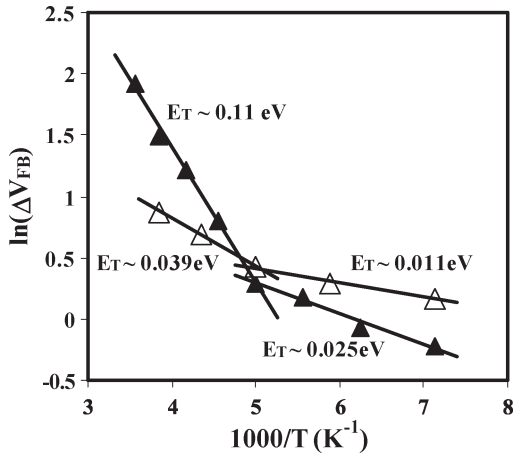


Fig. 6. Ionization energy levels $(E_{\rm T})$ calculated from $\Delta V_{\rm FB}$ with respect to 1000/K. The $E_{\rm T}$ for the nitrided devices is 110 and 25 meV (solid triangles), while for the nonnitrided it's 39 and 11 meV (empty triangles).

TABLE I
PROPERTIES OF NITRIDED VERSUS NON-NITRIDED Ge/HfO_2/Al MOS CAPACITORS

	Nitrided	Non-nitrided
Hysteresis (V)	0.03	0.5
Interface State Density (/cm^{2}eV)	2.9×10^{13}	4.55×10^{12}
Estimated Traps Energy levels (eV)	0.11, 0.025	0.039, 0.011

were estimated for both the nitrided and nonnitrided devices [16]. As shown in Fig. 6, the estimated $E_{\rm T}$s from the slope of the curve for nitrided sample are ~110 and 25 meV, while for nonnitrided samples they are 39 and 11 meV from the Ge conduction band edge. The observed shallow traps in both devices are rather similar except the observed deeper trap energy level in nitrided devices. Presence of this additional trap energy level confirms that the presence of nitrogen is indeed responsible for the new trap levels in the bulk oxide. Table I summarizes the effect of surface nitridation on interface traps as well as on oxide traps.

Charge-trapping characteristics were studied using a constant voltage stress to understand the device behavior, as it can affect the reliability of the devices by altering $V_{\rm FB}$ and the defects in gate oxide. A positive shift in $V_{\rm FB}$, observed in nonnitrided devices, implies electron trapping, as shown in Fig. 7, consistent with the different gate dielectric on a silicon substrate [17], for stress voltages less than -3 V. Interestingly, nitrided devices show a totally opposite trend with the negative shift in $V_{\rm FB}$, implying hole trapping as a function of the stress time. It is probably due to the nature of the defects introduced by surface nitridation in bulk oxide as observed in low-temperature measurements. On the other hand, a possible stress-induced N^+ ion diffusion in the gate dielectric from the interface can explain the trend. To further clarify the mechanism, the devices were subjected to a substrate injection, as shown in Fig. 8. In nitrided devices, it was observed that initially $V_{\rm FB}$ shifts negatively, but at a higher stress level (i.e., at 2.5 and 3 V) as the stress

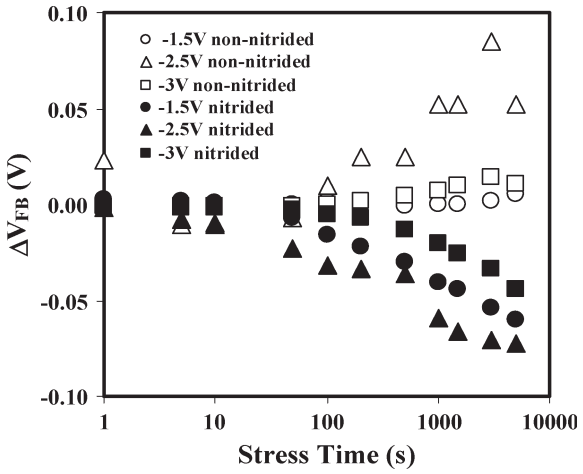


Fig. 7. Shift in the flatband voltage $\Delta V_{\rm FB}$ after a constant voltage stress, under gate injection, and of various time periods for the nitrided and nonnitrided Ge MOS capacitors.

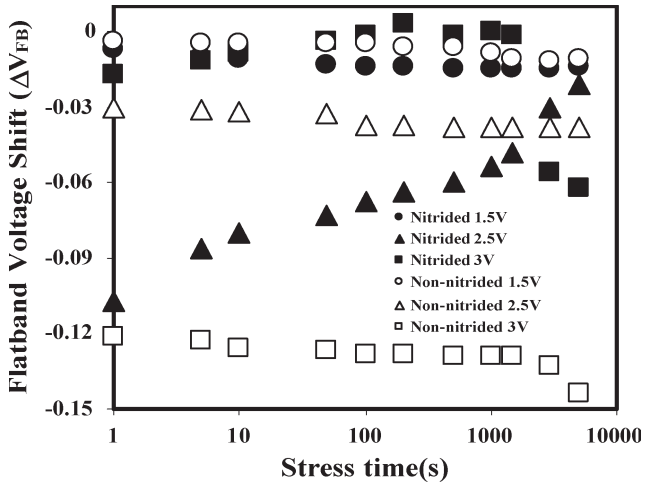


Fig. 8. Shift in the flatband voltage $\Delta V_{\rm FB}$ after a constant voltage stress, under substrate injection, and of various time periods for the nitrided and nonnitrided Ge MOS capacitors.

time increases, it starts shifting positively, thus reducing the shift in $V_{\rm FB}$. While in a nonnitrided case, negative shift keeps on increasing with stress voltage and time. Stress-induced $D_{\rm it}$ for both the nitrided and nonnitrided devices almost remained constant as a function of stress time at all stress levels, as shown in Fig. 9. Therefore, it can be concluded that a possible diffusion of N^+ ions in the dielectric could be the main reason of an opposite flatband voltage shift observed during gate injection. However, a maximum shift in $\Delta V_{\rm FB}$ at -2.5 V, in comparison to -3 V, for both the nitrided and nonnitrided devices implies that two different trapping mechanisms may be taking place at the same time. Although a mixed degradation in HfO_2 has been reported earlier [18], [20], it still requires further analysis to clearly differentiate between these two types of trapping mechanisms.

Fig. 10(a) and (b) shows the transient current characteristics of both the nitrided and nonnitrided devices as a function of the stress time. An almost constant increase in the current with the stress time shows a trap-assisted tunneling taking place in nonnitrided devices. While in nitrided devices, current is almost

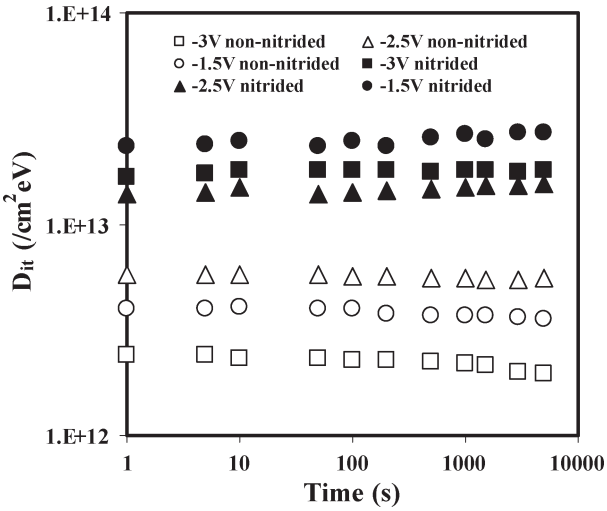
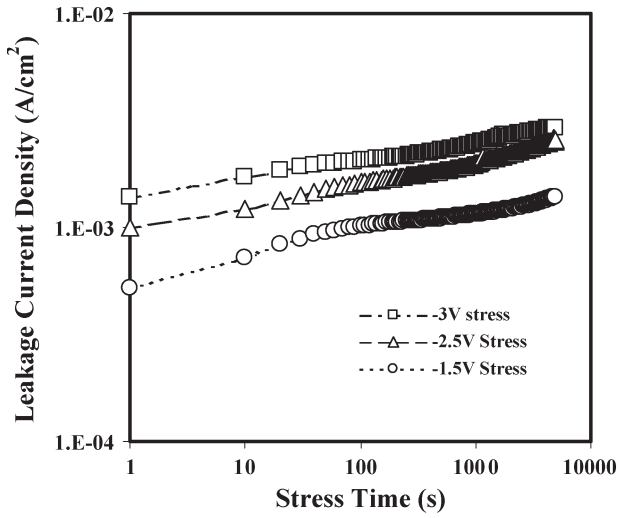
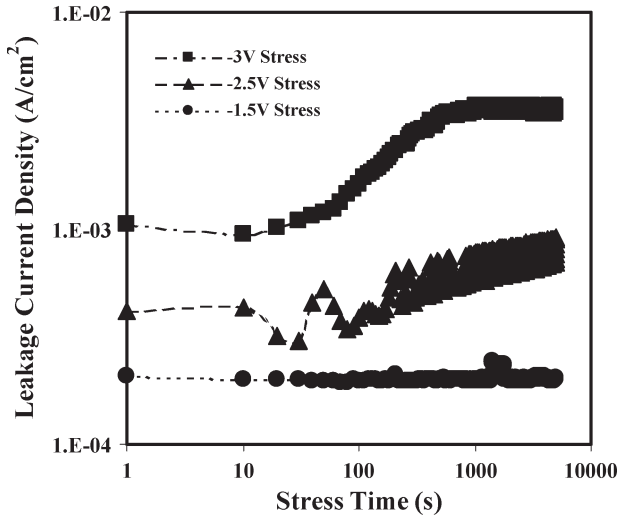


Fig. 9. Interface state density $(D_{\rm it})$ after stress, under gate injection, and of various time periods for the nitrided and nonnitrided Ge MOS capacitors.



(a)



(b)

Fig. 10. (a) Gate current as a function of time for the nonnitrided Ge MOS capacitors for three stress voltage of -1.5, -2.5, and -3 V. (b) Gate current as a function of time for the nitrided Ge MOS capacitors for three stress voltage of -1.5, -2.5, and -3 V.

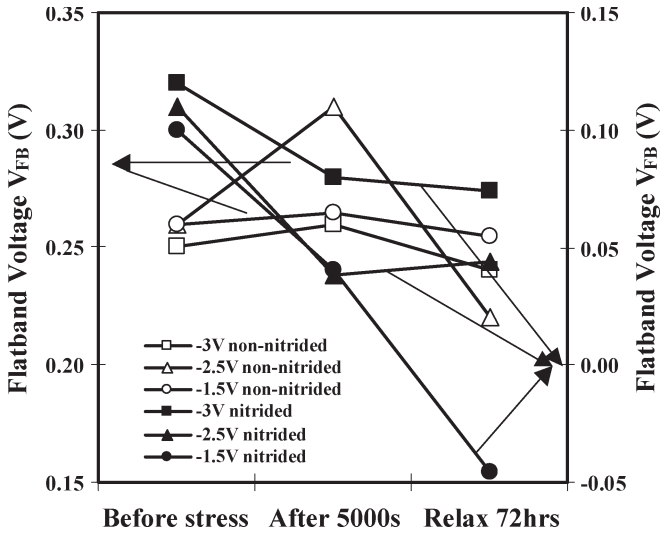


Fig. 11. Flatband voltage before stress, after a 5000-s stress, and after a 72-h relaxation for the nitrided and nonnitrided Ge MOS capacitors.

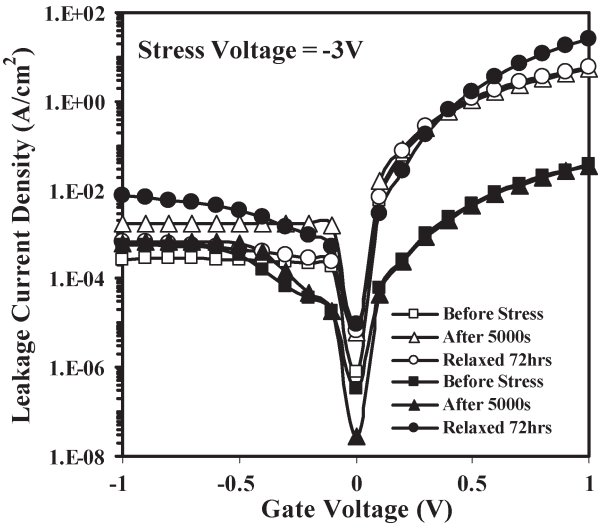


Fig. 12. Leakage-current density before stress, after a 5000-s stress at -3 V, and after a 72-h relaxation for the nitrided and nonnitrided Ge MOS capacitors.

constant at -1.5 V, implying hole trapping, which is also seen in a flatband voltage shift (Fig. 7). At higher voltage levels, an increase in the current as a function of the stress time suggests a trap-assisted tunneling as well. This also confirms the presence of two trapping mechanisms in these devices.

C–V and current–voltage (I–V) measurements were taken after three days, on the stressed devices. Figs. 11 and 12 show the $V_{\rm FB}$ and leakage-current density, respectively, of both the nitrided and nonnitrided devices before stress, after a 5000-s stress, and after a relaxation period of 72 h. Nonnitrided devices show a recovery from the charge-trapping damage after a relaxation period, as the flatband voltage almost comes back to their original value. For the nitrided samples, on the other hand, the flatband voltage remained slightly negative after 72 h at -3- and -2.5-V stress voltages, but at -1.5 V, device deterioration is worse. This further confirms that relaxation was not possible due to the presence of slow traps deep in the bandgap. These traps were possibly intrinsic to the nitrided devices or were created during stress due to nitrogen diffusion, as discussed earlier. Leakage current in nonnitrided devices also showed recovery after the relaxation period. In nitrided devices, an almost no change in the leakage current was observed immediately after the -3-V stress. But after relaxation, it increased up to three orders of magnitude in positive regime. Similar behavior was observed in the leakage-current characteristics of other two stresses voltages (not shown). It suggests that deeper trap levels, which are found from low-frequency and low-temperature measurements, trap the charge carrier immediately after stress, but with time these carriers detrap and create more traps inside the bulk oxide. However, this still needs to be investigated further.

IV. Conclusion

Ge/HfO_2/Al MOS capacitors with nitrided and nonnitrided Ge surfaces have been characterized using low-temperature measurements with temperature ranging from 140 to 300 K. Electron trapping was found to be dominant in both the nitrided and nonnitrided devices, as temperature was decreased from 300 to 140 K. The activation energies of the trap levels responsible for electron trapping in nitrided devices are estimated to be $\sim$110 and $\sim$25 meV, while for the nonnitrided devices are $\sim$39 and $\sim$11 meV. Interface state densities in nonnitrided devices show a variation of one order of magnitude with respect to the temperature, but nitrided device does not show major fluctuations in $D_{\rm it}$. Electron trapping is occurring in nonnitrided devices with stress, but hole trapping is dominant in nitrided devices due to a possible N^+ ion diffusion in the oxide. However, both devices show a mixed degradation at higher stress voltages. Nonnitrided devices seem to recover after relaxation, but a slow deterioration seems to be taking place in nitrided devices with time.

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