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Trapping in deep defects under substrate hot electron stress in TiN/Hf-silicate based gate stacks

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Abstract

Substrate hot electron stress was applied on n^+-ringed n-channel MOS capacitors with TiN/Hf-silicate based gate stacks to study the role of O vacancy induced deep bulk defects in trapping and transport. For the incident carrier energies above the calculated O vacancy formation threshold, applied on MOS devices with the thick high-κ layer, both the flatband voltage shift due to electron trapping at the deep levels and the increase in leakage current during stress follow t^n ($n \approx 0.4$) power law dependence. *Negative-U* transitions to the deep levels are shown to be possibly responsible for the strong correlation observed between the slow transient trapping and the trap-assisted tunneling.
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1. Introduction

Hafnium silicate based high-κ gate dielectrics have been put forth as the leading candidates to replace SiO_2 in sub-nm devices in CMOS technology [1]. Higher thermal stability, better leakage characteristics, improved threshold instability and less mobility degradation compared to HfO_2 [1–4] are the major advantages of Hf-silicate films though it has comparatively low dielectric constant (~8–15) depending on Hf content. Although the CMOS process compatibility of Hf-silicates has been achieved as far as fabrication is concerned [2], its reliability needs to be studied further.

The effect of the location of the electrically active defect level within the bulk high-κ bandgap on the transient trapping in Hf-based gate stacks, which is widely considered to be holding back the successful incorporation of the high-κ devices into CMOS technology, was critically investigated in the recent studies [4–9]. The fast transient trapping mostly occurs at the bulk defects with the energy levels near the high-κ band edges and is found to be quickly reversible under the post-stress low 'non-zero' gate bias conditions [6,9]. On the other hand, the slow transient trapping occurs at deeper levels, specially those lying within Si bandgap range in the context of MOS band diagram, and its lateral distribution is shown to inhibit fast threshold ΔV_T recovery even under the high bias conditions [4–6]. Hence, the trapping at the pre-existing or stress induced deep bulk defects can be reasonably considered to be the ultimate limiting factor for the long-term reliability of Hf-based devices.

Calculations show that O vacancies ($V^{++}/V^{+}/V^{0}$) are primarily responsible for the deep electron trapping in the high-κ oxides [10–14]. Their energy levels and formation energies are also found from calculations. For Hf-based oxides, Torii et al. [13] determined the deep V^0 level from the leakage measurements, and Yamabe et al. [15] found that O vacancies are responsible for electron trapping under the gate injection. However, the diversity in the usage of the deposition techniques, precursors for deposition, processing history, anneal conditions, etc. makes it imperative that the deep defect characteristics be

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studied on the case-by-case basis. Kumar et al. [16] applied substrate hot electron (SHE) stress on HfO_2 films with the incident carrier energies up to 6 eV and found that the defect generation threshold is ~4 eV. But, the defect generation characteristics under the incident carrier energy levels in the calculated O vacancies formation range (>7 eV) [10,12] are yet to studied for Hf-based oxides.

In order to address the above-mentioned reliability issues in TiN/$HfSi_xO_y$ based gate stacks, a number of studies are reported in this work. The deep bulk electron trap levels are experimentally observed in our gate stacks for the first time using low temperature techniques. SHE stress was applied on n^+-ringed n-channel MOS capacitors (nMOS-C) with the incident carrier energies below and above the O vacancy formation threshold. It is shown that flatband voltage shift, ΔV_{FB}, due to the enhanced electron trapping at the stress induced deep bulk defects, follows both t^n ($n \approx 0.4$) and $A \times Q_{inj}^{\beta}$ ($\beta \approx 0.4$) power law dependence for the incident carrier energies above the threshold. Under the same stress conditions, t^n ($n \approx 0.4$) power law fits are also observed for the increase in the leakage current density during stress, $\Delta J_g(t)$, due to the increased trap-assisted tunneling. The *negative-U* behavior of the stress induced defects is shown to be possibly responsible for the simultaneous occurrences of ΔV_{FB} and $\Delta J_g(t)$ during SHE injection with the high substrate bias. Comparison of the trapping characteristics in devices with the thin high-κ layer under the same stress conditions shows that the defects are generated mostly within the bulk high-κ.

2. Experimental

Hafnium silicate ($HfSi_xO_y$ – 20% SiO_2) film and TiN metal gate were deposited by MOCVD technique [3] on both n- and p-type Si substrates after ozone treatment had been performed for the pre-dielectric deposition cleaning, which resulted in ~10 Å of chemical oxide growth at the dielectric and Si substrate interface [4]. Isolation edge and n^+/p^+-ringed MOS capacitors were fabricated using the standard CMOS process flow. Using HRTEM, the physical thickness has been measured to be 4.5 nm including an interfacial layer (IL) of 1 nm [3]. These devices were further subjected to NH_3 PDA at 700 °C for 60 s to improve the leakage performance. The physical characterization details can be found elsewhere [3]. An effective oxide thickness (EOT) of 1.8–2 nm was estimated from the high-frequency *C–V* measurements after the quantum mechanical and temperature corrections [17]. TiN and 2 nm $HfSi_xO_y$ (20% SiO_2) were deposited by ALD method on p-Si to fabricate n^+-ringed nMOS-C and nMOSFET using standard CMOS process flow [18]. IL consists of 1 nm of chemical oxide. PDA was done in NH_3 ambient for 60 s. EOT was found to be around 1.2 nm. SHE stress was applied on n^+-ringed nMOS-C using HP4156B semiconductor parameter analyzer. Capacitance and conductance measurements (*C–V* and *G–V*) at 10 KHz to 1 MHz range were taken periodically during the stress with HP 4284 A LCR meter. CTI Cryogenic M24 refrigerator based closed loop system was used for the low temperature measurements.

3. Results and discussion

3.1. Low temperature measurements

The electrically active ionic defects are found to be mostly responsible for the trapping within the bulk high-κ oxides [1]. For Hf-based gate stacks with the thin IL (<2 nm), simulations show that it is possible to quickly (in the order of 10 ms) charge and discharge deep electron traps by applying moderately high positive and negative bias (~±2 V) respectively [9]. To characterize the defects with the deep levels, specially lying within Si bandgap range, we may use *C–V* measurement at different low temperatures as an effective method. It is possible to fill the deep bulk traps with the majority carriers injected from the substrate and subsequently empty them [19] if the gate bias (V_g) sweep levels from the accumulation to inversion regimes are carefully selected for a capacitor. The temperature dependent response of the majority carrier traps leaves its signature in ΔV_{FB} and, thus, enables the defect characterization. In this work, we are focused on studying the deep electron traps. Hence, *C–V* measurements are taken for capacitors with TiN/$HfSi_xO_y$/IL/n-Si gate stacks at low temperatures within 275–78 K range.

As V_g is swept from the accumulation to the depletion regime the deep bulk traps, with the energy level lying below Fermi level, become filled with electrons injected from the substrate. As V_g is swept from the depletion to inversion regimes, the bulk trap energy levels move above Fermi level and these traps tend to become empty as a result of the detrapping of electrons to Si conduction band, E_c^{Si}. However, this detrapping process is thermally activated. Hence, the detrapping decreases as the temperature is lowered, which results in the increase in ΔV_{FB} as observed in Fig. 1. We did quantum mechanical and temperature corrections while determining V_{FB} at low temperature using the computer program, CVC, developed by Hauser et al. [17]. Two distinct defect levels are observed from Arrhenius plots as shown in the inset of Fig. 1. The activation energies, E_a, of these deep defects are found to be 122 meV and 6 meV. In our earlier work [20], we observed that the peak value of 10 KHz *G–V* plots did not change, but it shifted to the right as temperature was lowered. It suggests that the trapping at the interface states does not significantly increase with low temperatures. Therefore, V_{FB} shifts to the right due to the oxide trapping. This further indicates that the observed ΔV_{FB} is most probably due to the trapping within the bulk. Therefore, the bulk electron (E_T' and E_T'') trap levels are determined with respect to E_c^{Si} in the context of MOS band diagram and are shown in Fig. 2. It may be noted that during each *C–V* measurement at a certain low temperature, V_g was swept from +1.75 V to −1.75 V with a high resolution of

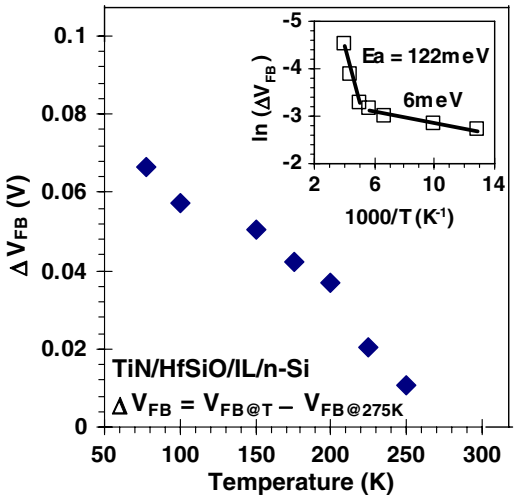

Fig. 1. ΔV_{FB} in 275–78 K temperature range for a capacitors with TiN/3.5 nm $HfSi_xO_y$/IL/n-Si gate stack. (Inset) Arrhenius plot of ln (ΔV_{FB}).

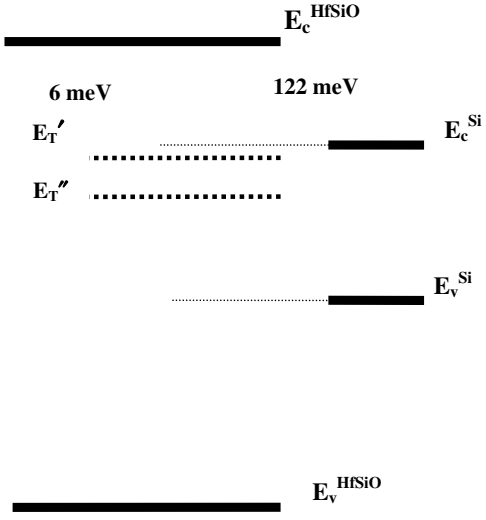

Fig. 2. Deep bulk electron (E_T' and E_T'') trap levels in the context of MOS band diagram for 3.5 nm Hf-silicate/IL.

voltage step (0.05 V) and inter-step delay (10 ms). Hence, the effect of low temperature induced residual trapping is probably negated.

Our objective is to inject electrons into the gate stack and observe its effect on ΔV_{FB}. Voltage across gate stack, $V_{OX} = V_{H-K} + V_{IL}$, where, V_{H-K} and V_{IL} are the potential drops at the high-κ and interfacial layer respectively. In our case, EOT is ~2 nm and physical thickness of Hf-silicate and interfacial layers are 3.5 and 1 nm respectively. Hence, $V_{H-K}/V_{IL} \approx 1$. Furthermore, $V_{H-K} = V_{IL} = V_{OX}/2 = (V_g - V_{FB} - \Psi_s)/2$, where Ψ_s is the surface potential. For p-MOS-C, $V_{FB} \approx 0.4$ V [20], and for $V_g = +1.75$ V, $V_{IL} \approx 0.7$ V. The offset between Hf-silicate and Si conduction bands ≈1.5 eV [21]. Hence, as far as band bending conditions during sweep are concerned, shallow electron trap energy levels lying within ~0.1 eV of Hf-silicate conduction band are not resonant with Si conduction band, which prevents them from being populated [8]. Therefore, the observed activation energies do not correspond to them.

To understand whether the deep defects, responsible for electron trapping, are located within the IL or high-κ layer of TiN/3.5 nm $HfSi_xO_y$/1 nm IL gate stacks, another set of samples with a different high-κ layer thickness and the same IL needs to be used. To this end, we took 100 KHz C–V and G–V measurements of nMOSFETs with TiN/2 nm $HfSi_xO_y$/1 nm IL gate stack at room and low (78 K) temperatures. To initially inject electrons into the gate stack and observe its effect on ΔV_{FB}, V_g was swept from +1.5 V to −1.5 V, i.e., from the inversion to the accumulation regime as shown in Fig. 3. $V_{IL} \approx 0.8$ V for $V_g = +1.5$ V, which allows the deep levels to be filled with electrons during sweep. It may be noted that the minority carrier (electrons) shortage during the substrate injection was avoided as source/drain were grounded. C–V measurements, however, show a negligible change in V_{FB} as temperature is lowered. Moreover, the peak value of G–V shows no change at low temperatures. Hence, trapping at the interface states is also negligible. Very fast detrapping from the bulk defects in 2 nm high-κ layers due to the very short tunneling distances (<2 nm) were reported [18]. If electron trapping in IL had dominated, ΔV_{FB} would have been significantly high positive value (see Fig. 1) irrespective of the high-κlayer thickness. As this is not the case, we may, therefore, argue that electron trapping mostly occurs within the bulk high-κ layer in 3.5 nm Hf-silicate/1 nm IL gate stack.

At low temperatures, especially below 20 K, the dopant atoms activation at the surface was reported to cause dispersion in C–V plots, especially at the flatband region [22]. Charging/discharging of the dopant atoms during C–V measurements results in the observation of the 'dip and peak' in the measured capacitance near flatband at low temperatures [23,24]. We did not observe any such discrepancies as we kept $T \geqslant 77$ K [20]. This further supports

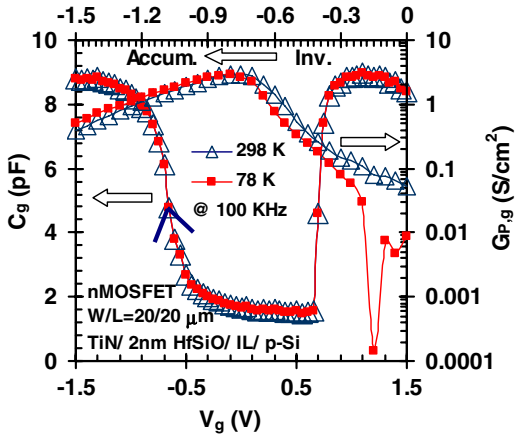

Fig. 3. 100 KHz C–V and G–V for 2 nm Hf-silicate/IL at 298 K and 78 K.

that the low temperature induced dispersion in C–V is most likely due to the trapping within the bulk high-κ.

As stated earlier, O vacancies ($V^{++}/V^{+}/V^{0}$) are the prime candidates for electron trapping at the deep levels within the high-κ dielectrics, which were shown to be O deficient [25]. Moreover, O diffusion during growth was also observed [24]. Following defect reactions are possible between vacancies (V^{0}/V^{+}) and interstitials (O^{0}/O^{-}), as calculated in [11], at the high temperatures during the growth:

$$O^{0} + V^{0} \Rightarrow O^{-} + V^{+} \quad (1)$$

$$O^{-} + V^{+} \Rightarrow O^{--} + V^{++} \quad (2)$$

As PDA at 700 °C took place during the fabrication of our devices, which was subject to the conventional CMOS process flow, it is quite reasonable to expect that such charged vacancies are present in our films. As such, the equilibrium in the numbers of charged vacancies and interstitials, i.e., the charge neutrality is maintained in the fresh devices.

It was reported in [26] that PDA at 700 °C/60 s in NH_3 ambient does not significantly increase N and simultaneously reduce O in Hf-silicate films as does PDA at higher temperature (e.g. 900 °C/15 s) in the same ambient. Hence, O vacancies are less in number under the former anneal condition [26], which in turn reduces electron trapping and leakage, and, thus, improves electrical performance.

Atomic N concentration was ~10% in Hf-silicate films [26] after 700 °C/60 s PDA in NH_3 ambient. One of the plausible reactions for NH_3 dissociation is $NH_3 \Rightarrow (NH_2)^{-} + H^{+}$, which was calculated to be occurring within 1–2 ps of PDA at $T > 330$ °C [8]. Therefore, H incorporation into the film can be expected to be at the order of that of N. Interfacial layer (IL) is chemically grown SiO_2 in our devices [4]. H passivates interface states after PDA and D_{it} is in range of 10^{12} cm^2 ev^{-1} in our type of devices [2,3]. Considering reduction of O at higher temperatures and NH_3 dissociation starting above 330 °C, we believe, PDA at 700 °C/60 s is probably optimized.

V^{++} shows the *negative-U* behavior [13,14], which is characterized by the relaxation of the defect state from the shallow to deeper levels after capturing electrons due to the strong electron lattice interaction. Calculations show that V^{++} occupies an energy level ~0.3 eV below the high-κ conduction edge [13]. Hence, it is filled with electrons injected from E_c^{Si} under positive gate bias. After capturing an electron ($V^{++} + e \rightarrow V^{+}$), V^{+} relaxes by ~1 eV to ~1.3 eV below the conduction edge. After capturing another electron ($V^{+} + e \rightarrow V^{0}$), V^{0} further relaxes by ~0.3 eV to ~1.6 eV below the conduction edge. The capture of electrons by V^{++}/V^{+} puts an end to the charge neutrality discussed above and the film becomes negatively charged [13]. Detrapping occurs in the reverse order. It may be immediately mentioned that considering Hf-silicate/Si conduction edge band offset to be ~1.5 eV [21], E_T'' lies ~1.6 eV below the high-κ conduction edge in our films. Therefore, it affirms our assumption regarding the presence of O vacancy defects in our bulk high-κ films. Furthermore, V^{0} level lies within Si bandgap range, i.e., it induces deep defect level and gives rise to the slow transient trapping.

3.2. SHE stress applied on n^{+}-ringed nMOS-C

SHE stress was applied on n^{+}-ringed nMOS-C using the arrangement shown in Fig. 4. SHE injection was realized by keeping the gate voltage (V_g) and substrate voltage (V_s) at low positive and high negative bias respectively, while the ring voltage (V_{ring}) was kept grounded. V_{inj} is the bias applied on n^{+}-ring of the adjacent capacitor located around 10 μm away, which forms a p/n^{+} junction and acts as an electron injector. For low gate bias ($V_g = 0.75$ V), the gate current during SHE injection increases by one order of magnitude compared to the cold carrier case [20]. Therefore, during SHE stress, gate current comprises mostly of hot electrons injected into the oxide. In addition, gate current, that is, hot electron injection, increases when the injector bias is increased for a given V_s.

SHE stress was applied on n^{+}-ringed nMOS-C with $V_s = -4$ V, -6 V, -8 V, -9 V and -10 V for ~4000 s. For $V_s = -10$ V, significant electron trapping occurred as 1 MHz C–V plots shift to the right in the flatband region as shown in Fig. 5. High-κ defects are highly ionic [1], i.e., electrically active. Charged defects contribute to the total bulk oxide charge and affect ΔV_{FB}. Electrons remain trapped at the stress-induced deep bulk defects even after SHE stress is removed because of the their energy level in the context of MOS band diagram and physical location within the gate stack. They may act as the fixed oxide charge and affect ΔV_{FB} provided they are near to IL/high-κ interface. Peaks of 10 KHz G–V plots shift to the right due to electron trapping. However, no change in the magnitude of the peaks is observed as the interface states generation was negligible [27] and trapping occurred mostly within the bulk high-κ. It is further observed that 18 h of detrapping at 'no bias' condition achieved only a partial ΔV_{FB} recovery.

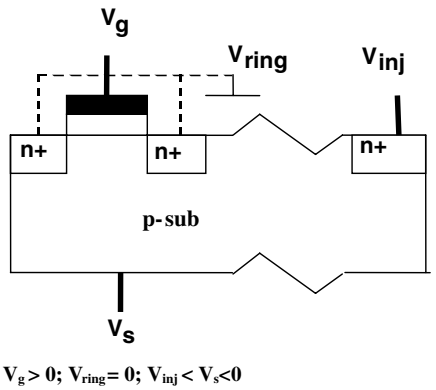

Fig. 4. Arrangement of n^{+}-ringed nMOS-C with n^{+}/p diode injector for SHE injection.

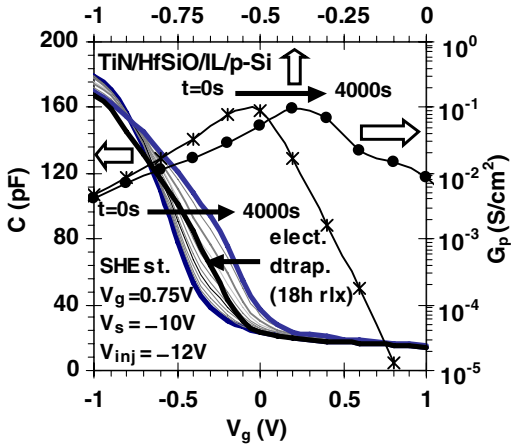

Fig. 5. For 3.5 nm Hf-silicate/IL, 1 MHz C–V plots before stress, after ~4000 s of SHE stress with $V_g = 0.75$ V, $V_s = -10$ V and $V_{inj} = -12$ V, and after 18 h of relaxation at 'no bias' condition. 10 KHz G–V plots before and after SHE stress.

In order to understand the effects of both the spatial location and the energy level of the deep bulk traps on the detrapping time to the substrate, the following modified Shockley–Read–Hall (SRH) model of carrier emission rate, $e_{n/p}$ can be used [9,28]:

$$e_{n/p} \propto \exp(-E_a/KT) \times T_{n/p} \quad (3)$$

$$T_{n/p} \propto \exp(-\Phi_B \times d_T) \quad (4)$$

Here, E_a is the activation energy of the deep bulk high-κ trap with energy level lying within Si bandgap range and is measured from Si band edge, K is Boltzman's constant, $T_{n/p}$ is the tunneling transparency, Φ_B is the barrier height seen by the trapped carriers and d_T is the distance of the trap location from the IL/high-κ interface provided IL is less than 2 nm to accommodate the direct tunneling to/from the bulk high-κ traps.

For traps near the substrate, detrapping time, which is the inverse of the emission rate, is thermally activated for the deep defects with constant E_a under 'no bias' condition. Hence, it is slow at room temperature. It is further understood that for an electron trap level above E_c^{Si} or a hole trap level below E_v^{Si} within the bulk high-κ, detrapping time primarily depends on the tunneling transparency. Therefore, it is considerably fast, and does not depend on temperature under 'no-bias' condition.

On the other hand, the lateral distribution of trapping (high d_T) is possible for stress with long periods of time. For the shallow traps with high d_T, the fast detrapping to the high-κ band edges occurs under a 'low bias' condition. But, for the deep traps with similar spatial distribution detrapping is considerably slow because of the tunneling transparency factor.

Therefore, time dependent post-stress ΔV_{FB} recovery characteristics need to be studied under both 'no bias' and 'low bias' conditions to correctly understand the trapping level (shallow/deep). However, re-stressing may occur for the latter, which limits the conclusions drawn from the observations of the detrapping characteristics.

Fig. 6 depicts ΔV_{FB} during SHE stress with $V_s = -9$ V, post-stress ΔV_{FB} recovery at different reverse gate biases and post-stress relaxation at 'no bias' conditions. Detrapping at -1 V recovers ΔV_{FB} by almost 30% very quickly (~1 s), but later it saturates. It shows that the shallow trapping at the conduction edge traps located away from the substrate occurs during the stress. This is consistent with our earlier observations under substrate injection as reported elsewhere [29]. On the other hand, detrapping at -1.5 V and -2 V shows comparatively slow reduction followed by saturation, which can be attributed to the trapping at the deep defects with lateral distribution. Relaxation at 'no bias' condition for 54 h, however, shows that hole trapping is partly responsible for the observed decrease in ΔV_{FB} under the negative gate bias. In our previous work [20], we also observed significant hole trapping at the deep defects for constant voltage stress applied on nMOS-C with the negative gate bias.

The slow ΔV_{FB} recovery time under 'no bias' condition, observed in Fig. 6, therefore, shows that ΔV_{FB} is due to both the fast and slow transient trapping. However, the latter dominates and is the focus of our investigations in this work. This is why the effect of the fast trapping on ΔV_{FB} needs to be eliminated to study the trapping at the deep defects. But, longer detrapping time under 'non-zero' bias conditions initiates re-stressing. Hence, after each period of SHE stress -1 V of reverse bias was applied for 1 s before ΔV_{FB} is measured in the following experiments. Stress/detrapping cycles were repeated for several times in Fig. 7. Steady increase in the pre-stress and the post stress ΔV_{FB} (>0) is observed, which shows that the traps are generated during the stress.

ΔV_{FB}, corrected for the conduction edge trapping, is plotted as a function of the stress time in log–log scale

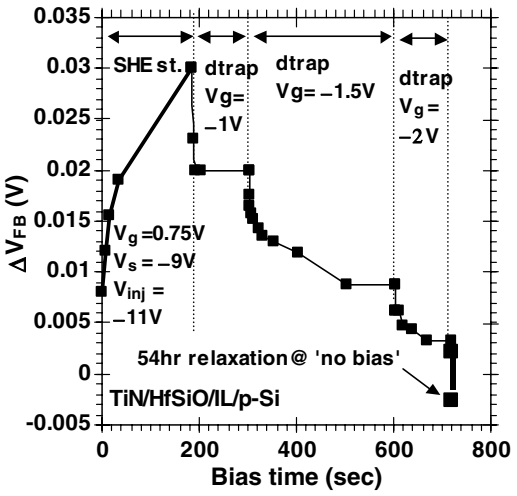

Fig. 6. For 3.5 nm Hf-silicate/IL, ΔV_{FB} during SHE stress, during post-stress detrapping under different reverse bias conditions, and after relaxation at 'no bias' condition.

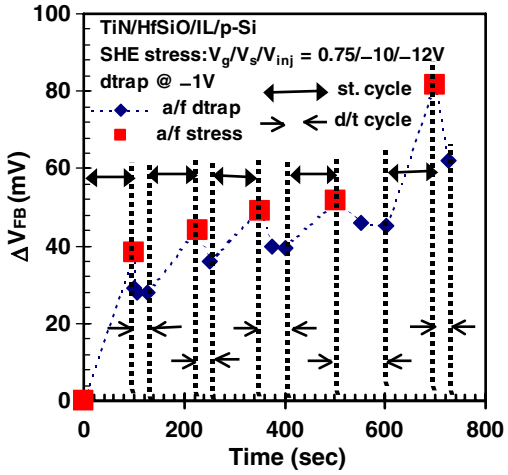

Fig. 7. For 2 nm Hf-silicate/IL, ΔV_{FB} during SHE stress/detrap cycles. SHE stress was applied with $V_g/V_s/V_{inj} = 0.75/-10/-12$ V. During detrapping cycle, $V_s = -1$ V.

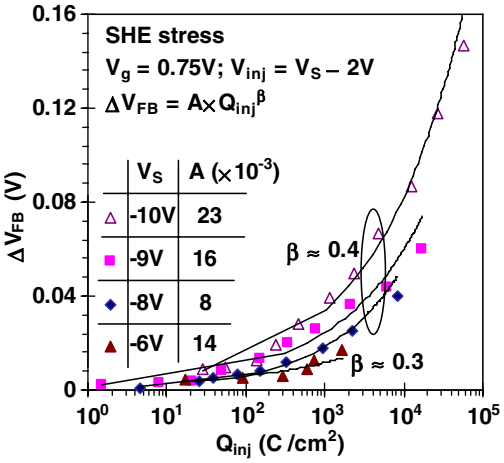

Fig. 9. For 3.5 nm Hf-silicate/IL, ΔV_{FB} vs. Q_{inj} under SHE stress at different $V_s(V_{inj} = V_s - 2$ V) bias conditions. (Inset) Table showing the value of the coefficient A for different V_s.

for different stress levels in Fig. 8. Power law fits clearly show that t^n dependence dominates for all stress levels due to the generation of the deep bulk defects. Fig. 9 shows ΔV_{FB} vs. injected charge, Q_{inj} for different stress levels. It is obvious from the power law fits of $A \times Q_{inj}^{\beta}$ that the deep bulk defect generation increases with the stress level for a given Q_{inj}. It may be noticed that for $V_s = -8$ V to -10 V, the exponents n and $\beta \approx 0.4$ whereas, they are ≈ 0.3 for $V_s = -6$ V. This disparity may be due to the difference in the defect generation mechanisms. This anomaly is also visible from the values of coefficient A, shown in the inset of Fig. 9. The value of A increases with stress level for $V_s = -8$ V to -10 V, which suggest similar defect generation mechanism. But, this trend is not seen for $V_s = -6$ V. This further supports our earlier assumption.

Change in the leakage $\Delta J_g(t) = J_g(t) - J_g(0)$ vs. stress time in Fig. 10 shows that it also follows t^n power law dependence. The bulk defect generation is responsible for

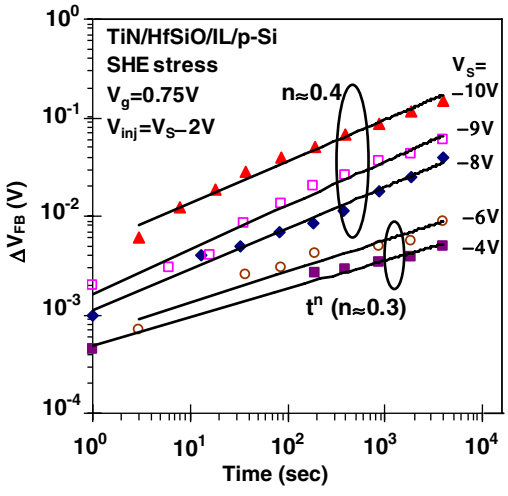

Fig. 8. For 3.5 nm Hf-silicate/IL, ΔV_{FB} vs. stress time in log–log scale under SHE stress at different $V_s(V_{inj} = V_s - 2$ V) conditions.

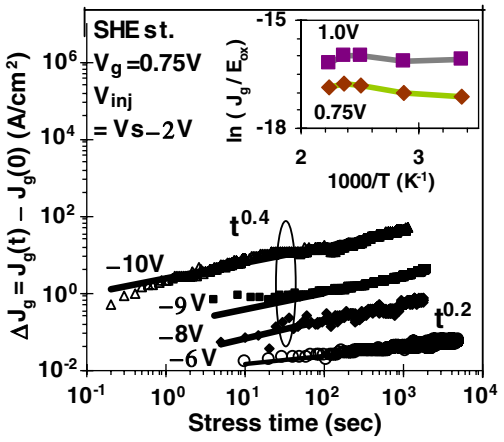

Fig. 10. For 3.5 nm Hf-silicate/IL, $\Delta J_g(t)$ vs. stress time in log–log scale under SHE stress at different $V_s(V_{inj} = V_s - 2$ V) bias conditions. (Inset) Arrhenius plot of $\ln(J_g/E_{ox})$ for different V_g.

the enhanced trap-assisted tunneling induced increase in the leakage especially at low V_g [30]. Another reason for increase in $\Delta J_g(t)$ may be due to the positive charge build-up near the substrate [16,30]. The release of the energy of plasmons at the metal/high-κ interface induces the energetic anodic hole injection [31], which initiates the positive charge build-up. But, the most obvious signature of this process is the interface state generation [16,30,31], which is not observed in our case. This is why, the latter option can be ruled out. Therefore, the stress induced defects, responsible for the enhanced slow transient trapping and trap-assisted tunneling, may be the same as they show the same value of n, especially for $V_s = -8$ V to -10 V. The value of n, however, does not follow this trend for $V_s = -6$ V, which is expected from our previous discussion.

The inset of Fig. 10 shows Arrhenius plot of $\ln(-J_g/E_{OX})$ for n^+-ringed nMOS-C under substrate injection at low gate bias and high temperature conditions. It is

obvious that a thermally and field activated conduction mechanism (e.g. Poole–Frenkel-type) is absent for $V_g = 0.75$ V and 1 V in our gate stacks as Arrhenius plots do not show a straight-line behavior [32]. Here, resultant electric field, $E_{OX} = E_{HK} + E_{IL} = V_{HK}/t_{HK} + V_{IL}/t_{IL}$, where, E_{HK} and E_{IL} are the electric field at the high-κ and interfacial layer respectively. In our case, EOT is ~2 nm and physical thickness of the bulk and interfacial layers are 3.5 and 1 nm respectively. Hence, $V_{HK}/V_{IL} = (t_{HK}/t_{IL}) \times (\kappa_{IL}/\kappa_{HK}) \approx (3.5/1) \times (1/3.5) \approx 1$. Furthermore, $V_{HK} = V_{IL} = V_{OX}/2 = (V_g - V_{FB} - \Psi_s)/2$. Therefore, $E_{OX} \approx V_{OX}/0.15 = (V_g - V_{FB} - \Psi_s)/0.15$ (MV/cm). Moreover, the change of the leakage with temperature is negligible, which is suggested by our earlier assumption that the trap-assisted tunneling dominates during SHE injection [32]. The shortage of the minority carriers did not occur under the substrate injection, as n^+-ring was kept grounded during the leakage measurements. It may be mentioned here that if trapping had occurred mostly at the shallow levels, which are resonant with electrons injected during SHE stress at low V_g, the fast transient trapping would have dominated. The following discussions will explain why it did not happen; rather significant slow transient trapping occurred.

Incident carrier energy during SHE stress, $E_{inc} \approx q|V_s|$, where q is the charge of an electron [16]. As stated earlier, $E_{inc} \approx 4$ eV is known as the threshold for the defect generation in Hf-based dielectrics. But, O vacancy formation energy was calculated to be ~7 eV under equilibrium conditions [10,12]. Such defect generation is possible if the incident carrier energy during SHE stress is increased to above 7 eV. We observed the enhanced slow transient trapping due to the deep bulk defect generation for $V_s = -8$ V to -10 V, and its mechanism is shown to be different from that for $V_s < -7$ V.

In this work, we mostly observed the deep trap generation and subsequent trapping in them. Hence, ΔV_{FB} is due to the amount of trapped charge in stress-induced defects. Detrapping under post-stress reverse bias condition further supports this observation (see Figs. 5–7). The amount of trapped charge, $\Delta Q_{trapped}$ ($= \Delta V_{FB} \times C'_{ox}$; C'_{ox}: oxide capacitance per unit area) is plotted in Fig. 11 for different V_s under SHE stress. Here, we consider that the charge centroid is located near the substrate. The number of the generated traps, $N_{trap,gen}$ is also shown as the secondary axis in the same plot. Initially, the pre-existing traps are filled. Hence, $N_{trap,gen}$ does not show much difference for low V_s conditions.

A convincing answer to the question whether the trap generation predominantly occurs within the IL or high-κ layer may be obtained by applying SHE stress on the gate stacks with the same IL but different high-κ layers. Our original gate stack was TiN/3.5 nm $HfSi_xO_y$/1 nm IL/ p-Si. To clarify the above stand, we applied SHE stress under the same conditions on TiN/2 nm $HfSi_xO_y$/1 nm IL/p-Si gate stacks. ΔV_{FB} and $\Delta J_g(t) = J_g(t) - J_g(0)$ vs. stress time in Fig. 12 show the strikingly different characteristics. For 2 nm Hf-silicate, the mixed degradation due to both electron and hole trapping dominates. This is in sharp contrast to 3.5 nm Hf-silicates (see Figs. 8–11), where the monotonously increasing electron trapping dominates. We may, therefore, conclude that the stress-induced defects are located mostly within the high-κ layer in TiN/3.5 nm $HfSi_xO_y$/1 nm IL gate stacks.

Energy levels of the defects, generated within IL, needs to be resonant with the conduction band of the substrate and the bulk high-κ (3.5 nm thick) trap levels to participate in trap-assisted tunneling across the oxide [8]. However, strong correlation observed in between increase in stress induced leakage and ΔV_{FB} (see Figs. 8 and 10) suggests that bulk trap generation, which dominates under high V_s conditions, is mostly responsible for both electron trapping and trap-assisted tunneling.

A plausible and coherent phenomenon during SHE stress at a high V_s and a low V_g conditions, which is consistent with our experimental observations, is depicted in

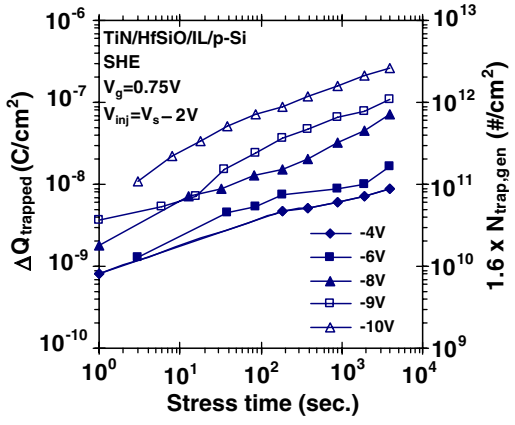

Fig. 11. For 3.5 nm Hf-silicate/IL, amount of stress induced trapped charge, $\Delta Q_{trapped}$ and number of stress induced traps, $N_{trap,gen}$ as a function os stress time for different V_s conditions under SHE stress.

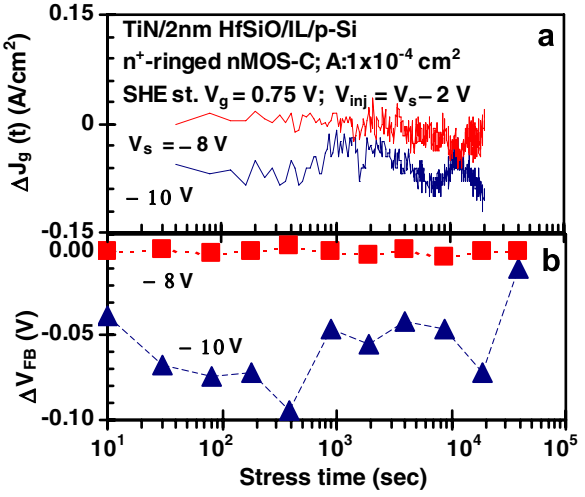

Fig. 12. For 2 nm Hf-silicate/IL, (a) $\Delta J_g(t)$ and (b) ΔV_{FB} vs. stress time under SHE stress with $V_s = -8$ and -10 V conditions.

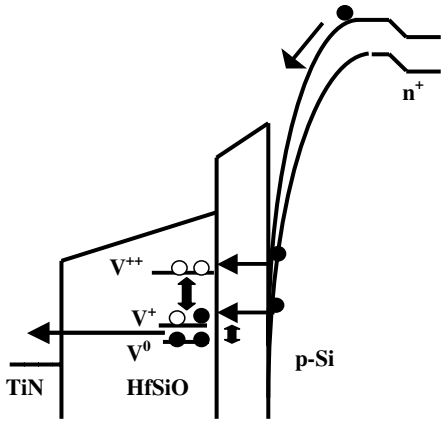

Fig. 13. For 3.5 nm Hf-silicate/IL, band diagram of the MOS structure showing the *negative-U* behavior of the stress induced charged O vacancy defects during SHE stress.

Fig. 13. Electrons impinge on Si/IL interface with high E_{inc} and generate V^{++} defects, which act as the *negative-U* centers. The relaxation to V^{+} and V^{0} levels due to the trapping, and subsequent tunneling from them toward the gate increases the leakage. Defect levels other than V^{++}/V^{+} are also possibly resonant with the injected electrons as far as the band bending at low V_g is concerned. Hence, the fast transient trapping at the shallow levels is observed; however, it is found to be partially responsible for ΔV_{FB}. A small fraction of the injected electrons ($\approx 1 \times 10^{-10}$) remains trapped at the stress induced V^{0} level and gives rise to the significant slow transient trapping.

Based on results and discussion it may be inferred that O vacancy generation most probably took place, which explains the simultaneous occurrences of the enhanced slow transient trapping and increased trap-assisted tunneling during SHE injection with high E_{inc}. We may further deduce that the slow transient trapping occurred at the deep defect levels observed from the low temperature measurements in our Hf-silicate films.

4. Conclusion

Low temperature techniques have been used to find the deep defect levels, which are responsible for the slow transient trapping in TiN/$HfSi_xO_y$ based gate stacks with the thick high-κ layer. An excellent match between the calculated deep defect level, which is induced by the relaxation of the charged O vacancy (V^{++}/V^{+}), and one of the observed electron trap levels is found. For the gate stacks with the thin high-κ layer and the same IL, negligible trapping is observed as temperature is lowered. This suggests that the deep defect levels are located within the high-κ layer. They are not, however, observed in the thin high-κ layers as very fast detrapping from them occur due to very short tunneling distances. For thick high-κ layer, ΔV_{FB}, due to electron trapping at the stress induced deep defect levels, is observed to follow t^n and $A \times Q_{inj}^{\beta}$ power law dependence under SHE stress applied on n^+-ringed nMOS-C. The disparity in the values of the exponents and coefficients clearly indicates that the defect generation mechanism changes as the incident carrier energy (E_{inc}) increases above the calculated O vacancy formation threshold. For E_{inc} above the threshold, ΔV_{FB} and $\Delta J_g(t)$ are found to increase with the same value of the exponent. Hence, the same defects are likely responsible for the simultaneous occurrences of the enhanced slow transient trapping and increased trap-assisted tunneling. The *negative-U* behavior of the stress induced defects, which is a signature of the charged O vacancies, is shown to coherently explain these observations. For thin high-κ layer, however, mixed degradation dominates. Therefore, it may be concluded that the generation of the charged O vacancies within the bulk high-κ and subsequent trapping in them are possibly responsible for the slow transient trapping observed under SHE injection with high E_{inc} in our thick Hf-silicate films.

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