Asynchronous Communication for Wireless Sensors Using Ultra Wideband Impulse Radio

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***Abstract*— This paper addresses simulations and design of an asynchronous integrated ultra wideband impulse radio transmitter and receiver suitable for low-power miniaturized wireless sensors. This paper first presents software simulations for asynchronous transmission over noisy channels using FSK-OOK modulation, which demonstrates that the proposed architecture is capable to communicate reliably at moderate signal-to-noise ratios and that the main errors are due to deletions of received noisy transmit pulses. Then, we address a hardware chip implementation of the integrated UWB transmitter and receiver, which is fabricated using an IBM 0.18μm CMOS process. This implementation provides a low peak power consumption, i.e., 10.8 mW for the transmitter and 5.4 mW for the receiver, respectively. The measured maximum baseband data rate of the proposed radio is 2.3 Mb/s.**

***Index Terms*—Asynchronous Communication, Ultra Wideband Impulse Radio, Low Power Wireless Sensors, Integrated Circuits.**

I. Introduction

In recent years there has been a growing demand of low-power small-size wireless sensors in many applications such as environmental observation [1], biomedical signal monitoring [2], and security surveillance systems [3]. Since such applications require a wireless sensor operating in "always-on" mode, the increased data rate and limited power constraint of the sensor become significant design challenges. For example, the battery of a surveillance wireless image sensor [3] needs to be replaced every two days. This power-and-speed trade-off limits such sensors to be deployed in the wild. Therefore, there is a critical need for low-complexity low-power sensor architectures capable of providing reliable high data-rate transmission over a noisy communication link.

Asynchronous sensing becomes attractive to solve the above problems [4]. In most of the "always-on" monitoring applications, the input signal is sparse or pulse-based, while only the rapid variation of the signal is of interest. A conventional architecture with a constant sampling rate generates a large amount of null data and wastes considerable energy when sensing a sparse signal. In contrast, asynchronous sensing generates a trigger pulse only when the input amplitude crosses a set of predefined thresholds and therefore converts the analog input signal into asynchronous digital pulse sequences. Many asynchronous sensing systems have been proposed [5]–[7] and some applications have been investigated [8].

In order to implement wireless sensing, sensors and radios must be seamless combined. Nonetheless, current prevalent synchronous wireless communication devices cannot match the asynchronous sensing front-end, since synchronous digital radio interfaces require clocked data packets and thus must be redesigned to enable an asynchronous operation. Although some techniques such as sleep-mode or wake-up circuitry are proposed to solve the problem, these methods typically apply a larger amount of circuitry which increases the hardware complexity. Furthermore, asynchronous radios require wideband carriers which are not well suited for narrow-band radio applications.

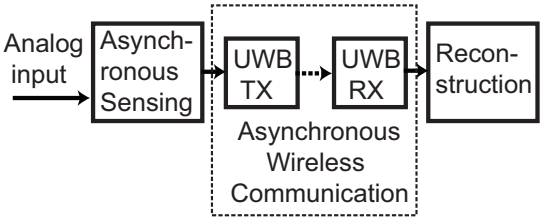

Fig. 1. Asynchronous wireless sensing system, where an ultra wideband (UWB) impulse radio is used for asynchronous communication.

Ultra wideband impulse radio (UWB-IR) is a competitive candidate for asynchronous radio, which has been already demonstrated in asynchronous data communication [9]. An overview about the proposed asynchronous communication system is shown in Fig. 1, where the analog input signal is converted to asynchronous pulses and transmitted by asynchronous radio using UWB-IR. We first provide a numerical simulation of the whole system for transmission over a noisy communication channel, where the obtained performance results provide guidelines for the design of the hardware implementation. As one of the main results we observe that the proposed system mainly suffers from errors due to the deletion of received pulses at low signal-to-noise ratios. Based on these results we then propose both a low complexity UWB receiver and transmitter hardware implementation, fabricated using an IBM 0.18μm CMOS process.

II. Asynchronous Communication System

A. Computer simulation setup

In this section, we provide numerical simulation results for the proposed asynchronous communication system. The asynchronous sampling stage for converting the analog waveform signal into discrete-time samples is shown in Fig. 2. Here, the waveform signal is sampled with equidistantly spaced decision levels, where the number of employed thresholds is given

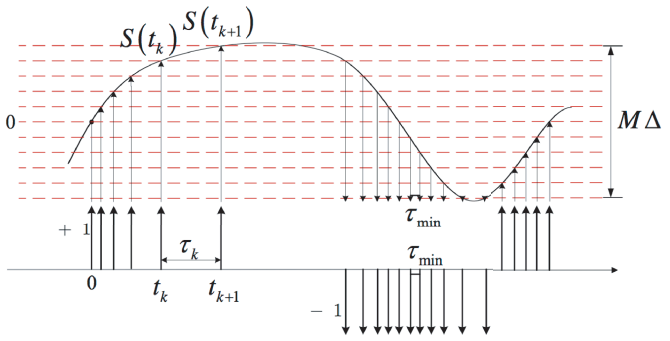

Fig. 2. Asynchronous sampling operation

by M. Further, $S(t)$ denotes the amplitude of the signal, t_k the timing information of the samples, and τ_k the interval between t_k and t_{k+1}, respectively. The quantization interval Δ is defined as

$$\Delta \triangleq \frac{2\max(|S(t)|)}{M}, \tag{1}$$

A "+1" (positive) sample is placed whenever a decision level of an integer multiple of Δ is exceeded by the waveform signal in the direction of increasing amplitude, otherwise a "-1" (negative) sample is placed.

After sampling, the samples are modulated by frequency shift keying (FSK) modulation, where the carrier pulses are given as [10]

$$C_{f_n}(t) = \begin{cases} \sqrt{\frac{E}{T}}\left(\frac{\sin(\pi t/2T)}{\pi t/2T}\right)\cos\left((n+0.5)\frac{\pi t}{T}\right), t \in \left[-\frac{\tau_k}{2}, \frac{\tau_k}{2}\right], \\ 0 \quad \text{otherwise}, \end{cases} \tag{2}$$

where $\frac{3T}{2n+1}$ denotes the time interval from zero to the first zero crossing of the pulse for $n \in \{1, 2\}$, E is the pulse energy, and τ_k the time difference between two samples at time k. Every pulse is bandlimited to the frequency range $\left[\frac{n}{2T}, \frac{n+1}{2T}\right]$. The positive and negative pulses obtained from the sampling stage are multiplied by $C_{f_1}(t)$ and $C_{f_2}(t)$, respectively. We define the smallest possible sampling interval, which is a function of the source waveform signal, M, and Δ as $\tau_{\min}$ (see Fig. 2). In order to avoid carrier interferences due to overlapping FSK pulses, the length of the pulses τ_k is fixed to $\tau_{\min}$.

The received signal $r(t)$ is composed of pulses of frequencies f_1 and f_2 plus additive noise $n(t)$, which is given as

$$r(t) = \sum_{i=1}^{p} C_{f_1}(t - t_i^{f_1}) + \sum_{j=1}^{q} C_{f_2}(t - t_j^{f_2}) + n(t), \tag{3}$$

where p and q represent the number of pulses with frequency f_1 and f_2, respectively. A block diagram of the corresponding receiver is shown in Fig. 3, where we use two matched filters $C_{f_1}(-t)$ and $C_{f_2}(-t)$ to recover the samples. After smoothing the matched filter output energies $E_{1/2}(t)$ with a suitable time window, we perform a threshold decision on the filtered energies $E'_{1/2}(t)$ with a suitably selected threshold.

B. Results

The employed waveform source signal consists of a heart beat signal from a mouse, recorded via an electrocardiogram with a sampling frequency of 20 kHz. In order to simulate a quasi continuous-time signal and to mimic a proper sampling operation we interpolate 10,000 points between all the adjacent samples of this signal.

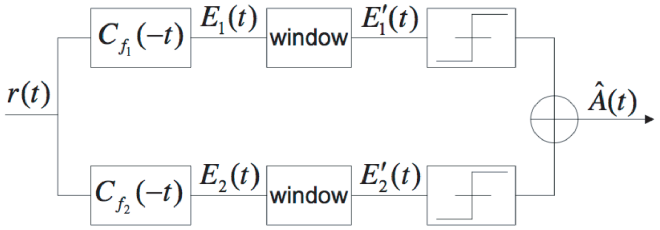

Fig. 3. Receiver block diagram

The bandwidth of the baseband FSK pulses is chosen as $\frac{1}{2T} = 10\,\text{MHz}$, thus the carrier frequencies are given as $f_1 = 15\,\text{MHz}$ and $f_2 = 25\,\text{MHz}$. Further, we use $E = 1$ in (2), and we consider an additive white Gaussian noise (AWGN) channel. Fig. 4(b) shows error probabilities for the different error types occurring in the system, namely insertion, deletion, and shift errors, and the total error probability over the bandlimited signal-to-noise ratio (SNR) on the AWGN channel. The results have been obtained by averaging 400 simulated transmissions over the AWGN channel for 10 ms of the source waveform signal.

The shift errors shown in Fig. 4(b) are generated by time position shifts of the reconstructed pulses due to small changes of the shape of the energy waveforms $E'_{1/2}(t)$ under channel noise. We define the shift error probability as

$$P_e \triangleq \Pr(\{|(t_i - d_1) - \hat{t}_i| > \tau_{\text{tol}}\}), \tag{4}$$

where t_i and $\hat{t}_i$ are the time positions of the i-th original and reconstructed sample, resp., and d_1 is a small offset to align both the original and recovered signal at time zero. If the time difference exceeds the value of τ_{tol}, which is a prescribed tolerance parameter, we declare a shift error. In Fig. 4(b), τ_{tol} is chosen as $\tau_{\text{tol}} = 0.3\,\text{ms}$ without loss of generality. Insertion errors are obtained in the low SNR regime due to the noise-induced signal fluctuations at the output of the windowed matched filter as for a fixed decision threshold in this case a new pulse may be detected which is not present in the original signal. Similarly, if an original pulse is not detected due to the channel noise, we obtain a deletion error. We can observe from Fig. 4(b) that the deletion errors are small when the SNR is low, since in this regime we naturally have more insertions than deletions.

Fig. 4(a) shows the distortion D for different numbers of quantization thresholds M versus the SNR on the AWGN channel, where D is defined as

$$D \triangleq \frac{1}{T_d}\int_0^{T_d} |S(t - d_1) - \hat{S}(t)|^2 dt, \tag{5}$$

with T_d denoting the overall duration of the waveform signal. As expected, the distortion decreases with increasing SNR and eventually reaches a constant level. This constant level is only determined by M and corresponds to the noiseless reconstruction distortion. Note that for $M = 7$ the average sampling rate amounts to 4.3 kHz, which is a reduction by

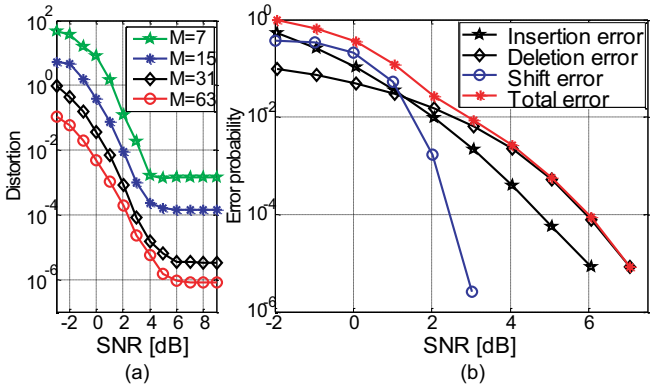

Fig. 4. (a) Distortion for different numbers of quantization thresholds M versus the SNR on the AWGN channel, (b) error probability versus SNR on the AWGN channel for different types of errors.

78.5% compared to the original synchronous sampling rate of 20 kHz.

III. Asynchronous Radio Circuit Design

The asynchronous radio transmitter and receiver are designed based on the specifications of an implantable biomedical application [2], which may require a data rate as high as 50 Mb/s. Since in asynchronous sensing each sample can be represented by using only 2 bits (positive or negative), savings of roughly 80% of the data rate can be obtained compared to a traditional system that requires 10 bits to represent one sample. By applying the result from Section II of a 78.5% sampling rate reduction, the minimal target data rate of the asynchronous radio is given as $50\cdot(1-0.785)\cdot(1-0.8)=2.15$ Mb/s, which is a significant reduction compared to the synchronous case. We choose the sub-GHz UWB frequency band for the radio because of the high tissue absorption of high frequency signals (>1 GHz) in implantable applications [2]. The proposed asynchronous radio applies frequency-shift-keying on-off-keying (FSK-OOK) modulation.

A. Transmitter Design

The proposed asynchronous radio uses two separate transmitters with FSK-OOK modulation for positive and negative pulses. Each transmitter consists of a ring oscillator with an input stage, a multiplexer chain, and a power amplifier. The baseband data is sent to the input stage, which performs OOK. The ring oscillator generates the RF carriers for the impulse modulation. The frequency of the RF carrier is controlled by a multiplexer chain, which performs FSK. The RF impulse is delivered to a power amplifier which drives the transmitter antenna. The simplified schematic of the transmitter is shown in Fig. 5.

OOK is realized at the input stage, which is implemented as a special inverter in the inverter-based ring oscillator with an enable signal as the data input. As shown in Fig. 5, when the input is logic low, the input stage is disabled. This cuts off the oscillation in the whole ring oscillator. On the other hand, when the input is logic high, the input stage is enabled, and the ring oscillator starts oscillating. Thus, the input data is modulated through the ring oscillator via OOK.

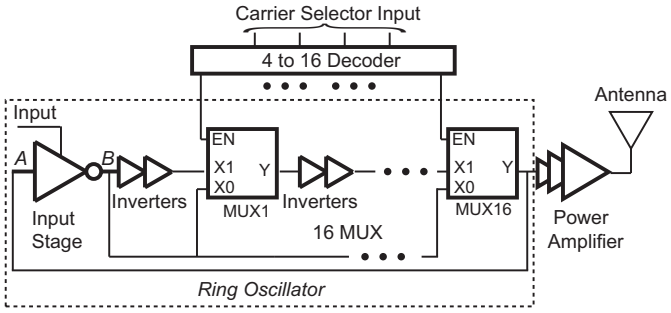

Fig. 5. FSK-OOK transmitter structure.

FSK is implemented by controlling the multiplexers in the ring oscillator. As shown in Fig. 5, each multiplexer has an enable signal *EN*. When the *EN* signal is logic high, the multiplexer passes the input *X1* to the output *Y*, otherwise it passes the input *X0* to the output *Y*. The difference between *X1* and *X0* is that the path of *X1* contains more inverters than the path of *X0*. Thus, selecting *X1* introduces more delay to the ring oscillator and lowers the oscillation frequency. In this design there are 16 multiplexers in the ring oscillator. By controlling the *EN* signals of the multiplexers, the frequency of the oscillator is adjusted. The total of 16 frequencies are selected by using a 4-to-16 decoder, which translates a 4 bit binary code to a 16 bit thermometer code for the multiplexers.

The power amplifier is made up of an inverter chain where the size of the inverter is increased at each stage. Further, it is able to drive the antenna up to the maximum carrier frequency.

B. Receiver Design

A non-coherent detection is utilized by the two receivers to detect positive and negative received pulses separately as shown in Fig. 3. Each receiver consists of a front-end filter, a low noise amplifier, a gain stage, a level shifter, an envelope detector, and a comparator. The receiver block diagram is shown in Fig. 6.

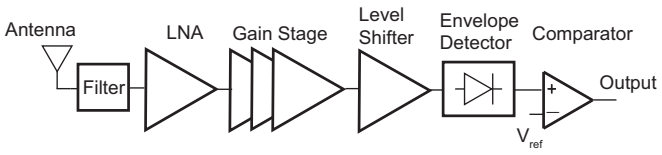

Fig. 6. Non-coherent receiver structure.

The first stage of the receiver is an off-chip bandpass filter to separate the positive and negative carriers. Then on the chip, a sub-mW UWB CMOS LNA [11] is implemented followed by the RF gain stages. Next, a level shifter shifts the DC value of the amplified RF signal from *VDD*/2 to *GND*. After that, an envelope detector is used to recover the baseband signal. The envelope detector is designed using a diode connected MOSFET followed by a capacitor in parallel with a discharging resistor. Both capacitor and resistor determine the time-constant for the charging and discharging paths, which is designed based on the carrier frequency and the baseband data rate. The detected envelope of the RF signal is digitized by

using a level-crossing comparator. The comparator is designed with hysteresis to avoid noise at the level crossing boundary [12]. An external DC signal serves as the reference voltage for the comparator. A multi-stage digital buffer follows the comparator to further enhance the output fanout of the receiver. Simulated waveforms at different positions in the receiver are displayed in Fig. 7.

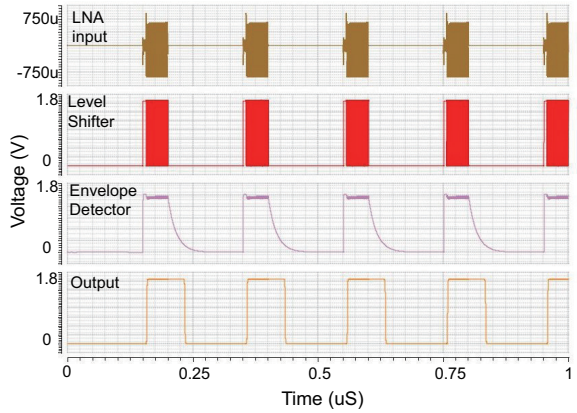

Fig. 7. Simulation result of the receiver at different nodes.

The transmitter and receiver circuits were designed and fabricated using an IBM 7RF 0.18μm CMOS technology. The power supply for both chips is 1.8V. The core sizes of the transmitter and receiver are 276μm x 114μm and 200μm x 86μm, respectively. The transmitter is designed to transmit pulses with a frequency range from 240 to 960 MHz. The frequency range of the receiver is between 200 MHz and 1 GHz. In a simple test setup monopole antennas are used for both transmitter and receiver. The maximum measured baseband data rate between the transmitter and receiver is 2.3 Mb/s, which is higher than the design specification target of 2.15 Mb/s. At this rate, the peak power consumption of the transmitter is 10.8 mW, whereas the receiver's power consumption is 5.4 mW. In our setup, the transmission distance between the transmitter antenna and receiver antenna is 15 cm.

IV. Conclusion

Transmitters	ISLPED2010 [13]	TVLSI2012 [3]	This Work
Process	90nm CMOS	0.5μm CMOS	0.18μm CMOS
Bandwidth	3∼5GHz	0∼3GHz	240∼960MHz
Data Rate	5Mbit/sec	1.3Mbit/sec	5Mbit/sec
Power	0.145mW	15mW	10.8 mW
Receivers	RFIT2012 [14]	RFIC2012 [15]	This Work
Process	65nm CMOS	65nm CMOS	0.18μm CMOS
Bandwidth	3.5∼4GHz	3∼5GHz	200MHz∼1GHz
Datarate	100kbit/sec	1Mbit/sec	2.3Mbit/sec
Power	3.8mW	0.45mW	5.4mW

TABLE I
Comparison of the proposed transmitter/receiver chip with existing work

We have presented an asynchronous wireless sensor architecture. Software simulations show that the system can communicate reliably at moderate SNR values, in low SNR the predominant type of errors are pulse deletions at the receiver. Transmitter and receiver chips have been designed and tested where the results from the software simulation were incorporated into the design process. Table I compares important design parameters between this work and recently published results and shows that the proposed asynchronous wireless sensing architecture is competitive compared with other approaches.

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